**ECE 4250/ 7250: VHDL and Programmable Logic Devices**

**Laboratory**

**Lab #: 07**

**Lab Title: BCD Converter**

**Group #: 5**

**Names: John Kelly | Zach Rump**

**Teaching Assistant Use Only:**

**Points Earned Reasons for Deduction**

**Pre-lab:**

**Post Lab report**:

**Demonstration:**

**Final Lab Grade:**

**Comments to students:**

**Objective**

The objective of Lab 07 is to implement BCD to Binary and Binary to BCD converters on Spartan-3 FPGA using the technique of separating data path and control section. The system will take a 16-bit input (loaded twice from the 8 switches) and display the conversion result as hex digits on the seven segment displays.

**Implementation**

The implementation is split into three categories: The code to drive the seven segment displays, the conversion implementations, and the test bench. The file Dec\_7seg.vhd describes which signals need to be sent to the 7-segment display for a given hexadecimal digit. The AnodeControl.vhd file cycles through the different seven segments and enables them by toggling the Anode. The test bench, Lab7Bench.vhd is used in conjunction with the Lab7Bench.ucf file in order to interface with the hardware. The end result is that the Spartan-3 hardware drives test bench which drives the BCD2BIN and BIN2BCD components. Finally, the LEDDisplay.vhd module is used as a component in the test bench, and ties all the modules together.

BCD2BIN

BIN2BCD

**Conclusion**

The main challenge with this lab was understanding the algorithm to actually perform the conversion.

**What troubles did we encounter how did we overcome them.**

**- How did this lab contribute to VHDL knowledge.**