CS4110 : COMPUTER SYSTEMS DESIGN LAB

Assignment #4

Deadline : 27th Oct. 11:55PM

This assignment is about simulating the cache coherence protocols

Specifications of the processor & memory :

- Bus-based shared memory two processor system
- private cache - 1KB/cache
- main memory - 32KB
- block size - 32B
- data bus-width - 32bit

Each processor performs only two operations: *read* and *write*. Each processor randomly picks a block, i.e., select a block out of 1024 blocks in the main memory, and read the data word by word from beginning to the end of the block. When the entire block is read by the processor, it then writes to a random word location in the block. This process is repeated again and again. When both the processors try to access the bus only one will be given the access permission to place its transaction on the bus. The main memory can serve only one request from the processor at a time.

One way to minimize the number of coherence transaction, and main memory accesses is to modify the MESI protocol by considering an additional state, Owned(O). The new protocol is called MOESI protocol. This requires direct cache to cache data transfer to be possible. Suppose a processor(C1) requests to write in block B, and it was not present the cache of procesor(C2). Then C2 requests to read the data,instead of writing it back to the main memory, the state of the block in C1 is changed to Owned(O) and is in state shared(S) in C2. On write hit from C1, the state is changed from O to M. And state O is invalidated only when C2 wants to write to B. The owned state contains the dirty data, and is responsible to reply for snoop request on the bus. This way it avoids the need to write back the modified data back to the memory before sharing.

Simulate the above memory access pattern and record the frequency of state changes and the number of coherence protocol places on the bus for both MESI an MOESI protocols.