OPCODE TABLE

SR. NO	OPCODE	INSTRUCTION	NO. OF ARGUMENTS	OPERAND 1	OPERAND 2	SIZE	MOD R/M	+RD	NO. OF BYTES
1	89 /r	mov reg32,reg32	2	reg	reg	2	Y	N	
2	B8+ rd id	mov reg32, imm32	2	reg	imm	5	N	Y	
3	8B /r	mov reg32,[mem]	2	reg	[mem]	6	Y	N	
4	C7 /0 id	mov [mem], imm	2	[mem]	imm	10	Y	N	
5	89 /r	mov [mem],reg32	2	[mem]	reg	6	Y	N	
6	01 /r	add reg32,reg32	2	reg	reg	2	Y	N	
7	81 /0 id	add reg32, imm32	2	reg	imm	3	Y	N	4
8	03 /r	add reg32,[mem]	2	reg	[mem]	6	Y	N	
9	81 /0 id	add [mem], imm32	2	[mem]	imm	10	Y	N	4
10	01 /r	add [mem],reg32	2	[mem]	reg	6	Y	N	
11	83 /0 ib	add reg32, imm8	2	reg	imm	3	Y	N	1
12	83 /0 id	add [mem], imm8	2	[mem]	imm	7	Y	N	1
13	29 /r	sub reg32,reg32	2	reg	reg	2	Y	N	
14	81 /5 id	sub reg32, imm32	2	reg	imm	3	Y	N	4
15	2B /r	sub reg32,[mem]	2	reg	[mem]	6	Y	N	
16	81 /5 id	sub [mem],imm32	2	[mem]	imm	10	Y	N	4
17	29 /r	sub [mem],reg32	2	[mem]	reg	6	Y	N	
18	81 /5 ib	sub reg32, imm8	2	reg	imm	3	Y	N	1
19	81 /5 id	sub [mem],imm8	2	[mem]	imm	7	Y	N	1
20	F7 /4	mul reg32	1	reg		2	Y	N	
21	F7 /4	mul [mem]	1	[mem]		6	Y	N	
22	F7 /6	div reg32	1	reg		2	Y	N	
23	F7 /6	div [mem]	1	[mem]		6	Y	N	
24	40+ rd	inc reg32	1	reg		1	N	Y	
25	FF /0	inc[mem]	1	[mem]		6	Y		
26	48+rd	dec reg32	1	reg		1	N	Y	
27	FF /1	dec[mem]	1	[mem]		6	Y	N	
28	31 /r	xor reg32,reg32	2	reg	reg	2	Y	N	
29	81 /6 id	xor reg32,imm32	2	reg	imm	6	Y	N	4
30	33 /r	xor reg32,[mem]	2	reg	[mem]	6	Y	N	
31	81 /6 id	xor [mem],imm32	2	[mem]	imm	10	Y	N	4
32	31 /r	xor [mem],reg32	2	[mem]	reg	6	Y	N	
33	81 /6 ib	xor reg32,imm8	2	reg	imm	3	Y	N	1

34	83 /6 ib	xor [mem],imm8	2	[mem]	imm	7	Y	N	1
35	39 /r	cmp reg32,reg32	2	reg	reg	2	Y	N	
36	81 /7 id	cmp reg32,imm	2	reg	imm	3	Y	N	
37	3B /r	cmp reg32,[mem]	2	reg	[mem]	6	Y	N	
38	81 /7 id	cmp [mem],imm	2	[mem]	imm	7	Y	N	
39	39 /r	cmp [mem],reg32	2	[mem]	reg	6	Y	N	
40	83 /7 ib	cmp reg32,imm8	2	reg	imm	3	Y	N	1
41	83 /7 ib	cmp [mem],imm8	2	[mem]	imm	7	Y	N	1
42	FF /4	jmp reg32	1	reg		2	Y		
43	FF /4	jmp [mem]	1	[mem]		6	Y		
44	0F 84 cd	jz [mem]	1	[mem]		2	N	N	
45	0F 85 cd	jnz [mem]	1	[mem]		2	N	N	