

DDCO Project

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Implementing Left Shift and Right Shift operations for existing register array

Code:

```
module shift_reg #(parameter MSB=8) ( input d, input clk, input en, input dir, input rstn, output reg [MSB-1:0] out);  
  always @ (posedge clk)  
  if (!rstn)  
    out <= 0;  
  else begin  
    if (en)  
      case (dir)  
        0 : out <= {out[MSB-2:0], d};  
        1 : out <= {d, out[MSB-1:1]};  
      endcase  
    else  
      out <= out;  
    end  
  end  
endmodule
```

Testbench file:

```

module tb_sr;
  parameter MSB = 16;
  reg data;
  reg clk;
  reg en;
  reg dir;
  reg rstn;
  wire [MSB-1:0] out;

  shift_reg #(MSB) sr0 ( .d (data),
                        .clk (clk),
                        .en (en),
                        .dir (dir),
                        .rstn (rstn),
                        .out (out));

  always #10 clk = ~clk;
  initial begin
    clk <= 0;
    en <= 0;
    dir <= 0;
    rstn <= 0;
    data <= 'h1;
  end
  rstn <= 0;
  #20 rstn <= 1;
  en <= 1;
  repeat (7) @ (posedge clk)
    data <= ~data;
  #10 dir <= 1;
  repeat (7) @ (posedge clk)
    data <= ~data;
  repeat (7) @ (posedge clk);
  $finish;
end
initial
begin
  $monitor ("rstn=%0b data=%b, en=%0b, dir=%0b, out=%b", rstn, data, en, dir, out);
  $dumpfile("tb_p1.vcd");
  $dumpvars(0,tb_sr);
end
endmodule

```

CMD:

```
C:\iverilog\bin>iverilog -o proj tb_p1.v p1.v

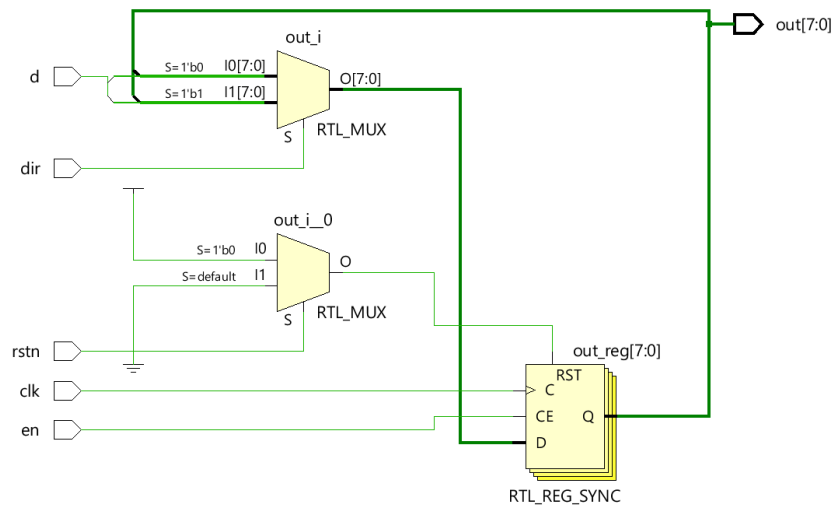
C:\iverilog\bin>vvp proj
VCD info: dumpfile tb_p1.vcd opened for output.
rstn=0 data=1, en=0, dir=0, out=xxxxxxxxxxxxxxxx
rstn=0 data=1, en=0, dir=0, out=0000000000000000
rstn=1 data=1, en=1, dir=0, out=0000000000000000
rstn=1 data=0, en=1, dir=0, out=0000000000000001
rstn=1 data=1, en=1, dir=0, out=0000000000000010
rstn=1 data=0, en=1, dir=0, out=0000000000000101
rstn=1 data=1, en=1, dir=0, out=0000000000001010
rstn=1 data=0, en=1, dir=0, out=0000000000010101
rstn=1 data=1, en=1, dir=0, out=000000000101010
rstn=1 data=0, en=1, dir=0, out=0000000001010101
rstn=1 data=0, en=1, dir=1, out=0000000001010101
rstn=1 data=1, en=1, dir=1, out=000000000101010
rstn=1 data=0, en=1, dir=1, out=1000000000010101
rstn=1 data=1, en=1, dir=1, out=010000000001010
rstn=1 data=0, en=1, dir=1, out=1010000000000101
rstn=1 data=1, en=1, dir=1, out=0101000000000010
rstn=1 data=0, en=1, dir=1, out=1010100000000001
rstn=1 data=1, en=1, dir=1, out=0101010000000000
rstn=1 data=1, en=1, dir=1, out=1010101000000000
rstn=1 data=1, en=1, dir=1, out=1101010100000000
rstn=1 data=1, en=1, dir=1, out=1110101010000000
rstn=1 data=1, en=1, dir=1, out=1111010101000000
rstn=1 data=1, en=1, dir=1, out=1111101010100000
rstn=1 data=1, en=1, dir=1, out=1111110101010000
tb_p1.v:52: $finish called at 430 (1s)
rstn=1 data=1, en=1, dir=1, out=1111111010101000

C:\iverilog\bin>gtkwave tb_p1.vcd
```

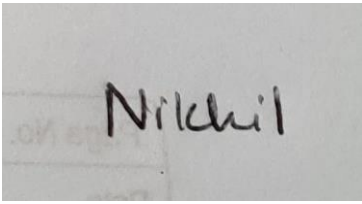
GTKWAVE:



Circuit Diagram:



Signatures:

A handwritten signature in black ink that reads "Nikhil". The letters are slightly slanted and connected.

Nikhil Girish

A handwritten signature in black ink that reads "Nive". The signature is enclosed within a hand-drawn circle.

P Niveditha

A handwritten signature in blue ink that reads "Charan". The signature is written in a cursive style with a long horizontal stroke at the end.

P Sai Charan

A handwritten signature in blue ink. It appears to be the name "Onkar" with a large "X" or cross drawn over it. There are also some additional strokes below the main signature.

Onkar Suhasrao Pampattiwar