**Microprocessor and Computer Architecture Laboratory**

**UE19CS256**

**4th Semester, Academic Year 2020-21**

Date: 24/03/23

| Name: Nikhil Girish | SRN: PES2UG21CS334 | Section: F |
|---|---|---|

Week#____8_____ Number: ____1__

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes.

a)Find Number of bits in tag, index and offset.

- Tag = 6 bits
- Index = 2 bits
- Offset = 2 bits

b)The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

| 0000 | 00 | 01 |
|---|---|---|
| 4 bit | 2 bit | 2 bit |

ii) Screenshot showing the Cache Table

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 0001 | BLOCK 4 WORD 0 - 3 | 0 |
| 1 | 1 | 0000 | BLOCK 1 WORD 0 - 3 | 0 |
| 2 | 1 | 0000 | BLOCK 2 WORD 0 - 3 | 0 |
| 3 | 0 | - | 0 | 0 |

iii) Screenshot showing hit and miss rates

**Statistics**

**Hit Rate :** **38%**

**Miss Rate :** **63%**

**List of Previous Instructions :**

- **Load 1 [Miss]**
- **Load 4 [Miss]**
- **Load 8 [Miss]**
- **Load 5 [Hit]**
- **Load 14 [Miss]**
- **Load 11 [Miss]**
- **Load 13 [Hit]**
- **Load 38 [Miss]**
- **Load 9 [Miss]**
- **Load B [Hit]**
- **Load 4 [Miss]**
- **Load 2B [Miss]**
- **Load 5 [Hit]**
- **Load 6 [Hit]**
- **Load 9 [Miss]**
- **Load 11 [Hit]**

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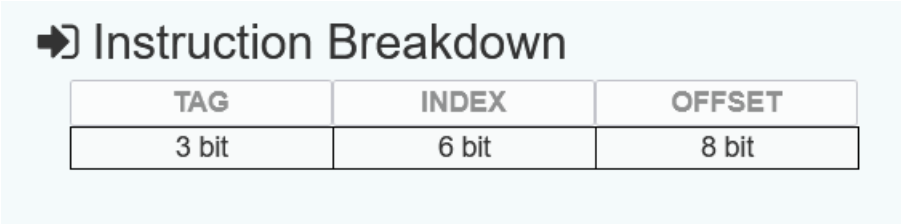
Week#____8_____ Number: ____2__

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



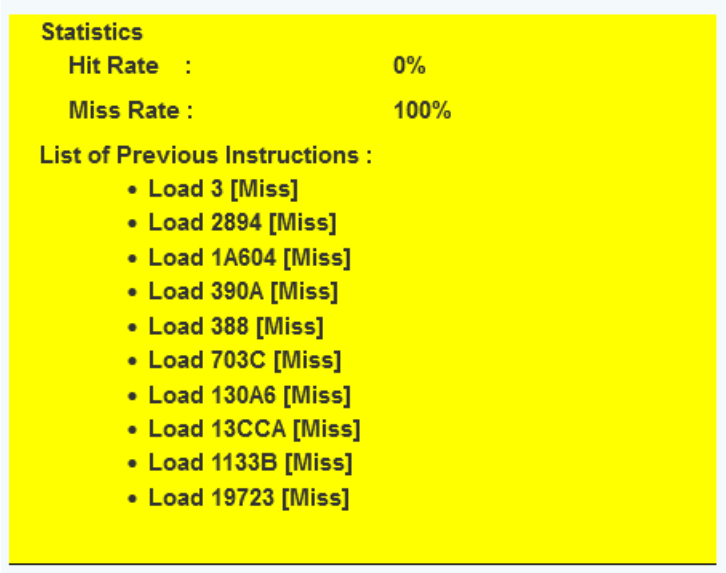

b) Screenshot showing the Cache Table

## Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 000 | BLOCK 0 WORD 0 - 255 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 1 | 000 | BLOCK 3 WORD 0 - 255 | 0 |
| 4 | 0 | - | 0 | 0 |
| 5 | 0 | - | 0 | 0 |
| 6 | 0 | - | 0 | 0 |
| 7 | 0 | - | 0 | 0 |
| 8 | 0 | - | 0 | 0 |
| 9 | 0 | - | 0 | 0 |
| 10 | 0 | - | 0 | 0 |
| 11 | 0 | - | 0 | 0 |
| 12 | 0 | - | 0 | 0 |
| 13 | 0 | - | 0 | 0 |
| 14 | 0 | - | 0 | 0 |
| 15 | 0 | - | 0 | 0 |
| 16 | 0 | - | 0 | 0 |
| 17 | 0 | - | 0 | 0 |
| 18 | 0 | - | 0 | 0 |
| 19 | 1 | 100 | BLOCK 113 WORD 0 - 255 | 0 |
| 20 | 0 | - | 0 | 0 |
| 21 | 0 | - | 0 | 0 |
| 22 | 0 | - | 0 | 0 |
| 23 | 1 | 110 | BLOCK 197 WORD 0 - 255 | 0 |
| 24 | 0 | - | 0 | 0 |
| 25 | 0 | - | 0 | 0 |
| 26 | 0 | - | 0 | 0 |
| 27 | 0 | - | 0 | 0 |
| 28 | 0 | - | 0 | 0 |
| 29 | 0 | - | 0 | 0 |
| 30 | 0 | - | 0 | 0 |
| 31 | 0 | - | 0 | 0 |
| 32 | 0 | - | 0 | 0 |
| 33 | 0 | - | 0 | 0 |
| 34 | 0 | - | 0 | 0 |
| 35 | 0 | - | 0 | 0 |
| 36 | 0 | - | 0 | 0 |
| 37 | 0 | - | 0 | 0 |
| 38 | 1 | 110 | BLOCK 1A6 WORD 0 - 255 | 0 |
| 39 | 0 | - | 0 | 0 |
| 40 | 1 | 000 | BLOCK 28 WORD 0 - 255 | 0 |
| 41 | 0 | - | 0 | 0 |
| 42 | 0 | - | 0 | 0 |
| 43 | 0 | - | 0 | 0 |
| 44 | 0 | - | 0 | 0 |
| 45 | 0 | - | 0 | 0 |
| 46 | 0 | - | 0 | 0 |
| 47 | 0 | - | 0 | 0 |
| 48 | 1 | 100 | BLOCK 130 WORD 0 - 255 | 0 |
| 49 | 0 | - | 0 | 0 |
| 50 | 0 | - | 0 | 0 |
| 51 | 0 | - | 0 | 0 |
| 52 | 0 | - | 0 | 0 |

| | | | | |
|---|---|---|---|---|
| 53 | 0 | - | 0 | 0 |
| 54 | 0 | - | 0 | 0 |
| 55 | 0 | - | 0 | 0 |
| 56 | 0 | - | 0 | 0 |
| 57 | 1 | 000 | BLOCK 39 WORD 0 - 255 | 0 |
| 58 | 0 | - | 0 | 0 |
| 59 | 0 | - | 0 | 0 |
| 60 | 1 | 100 | BLOCK 13C WORD 0 - 255 | 0 |
| 61 | 0 | - | 0 | 0 |
| 62 | 0 | - | 0 | 0 |
| 63 | 0 | - | 0 | 0 |

c) Screenshot showing hit and miss rates



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|---|---|---|

Week#____8_____ Number: ____3__

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 5 bit | 5 bit | 6 bit |

(b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

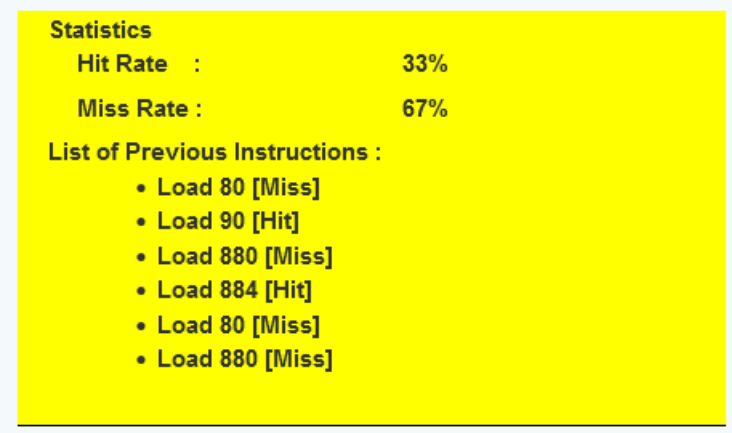
a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 5 bit | 5 bit | 6 bit |

b) Screenshot showing the Cache Table

c) Screenshot showing hit and miss rates

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|---|---|---|

Week#____8_____ Number: ___4__

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number

of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

### Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 4 bit | 5 bit | 8 bit |

b) Screenshot showing the Cache Table

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 1 | d | B. 1A2 W. 0 - 255 | 0 |
| 3 | 1 | e | B. 1C3 W. 0 - 255 | 0 |
| 4 | 1 | c | B. 184 W. 0 - 255 | 0 |
| 5 | 0 | - | 0 | 0 |
| 6 | 0 | - | 0 | 0 |
| 7 | 0 | - | 0 | 0 |
| 8 | 1 | 0 | B. 8 W. 0 - 255 | 0 |
| 9 | 0 | - | 0 | 0 |
| 10 | 0 | - | 0 | 0 |
| 11 | 0 | - | 0 | 0 |
| 12 | 0 | - | 0 | 0 |
| 13 | 0 | - | 0 | 0 |
| 14 | 0 | - | 0 | 0 |
| 15 | 0 | - | 0 | 0 |
| 16 | 0 | - | 0 | 0 |
| 17 | 1 | 5 | B. B1 W. 0 - 255 | 0 |
| 18 | 1 | 4 | B. 92 W. 0 - 255 | 0 |
| 19 | 0 | - | 0 | 0 |
| 20 | 1 | 6 | B. D4 W. 0 - 255 | 0 |
| 21 | 0 | - | 0 | 0 |
| 22 | 0 | - | 0 | 0 |
| 23 | 1 | b | B. 177 W. 0 - 255 | 0 |
| 24 | 1 | 7 | B. F8 W. 0 - 255 | 0 |
| 25 | 0 | - | 0 | 0 |
| 26 | 0 | - | 0 | 0 |
| 27 | 0 | - | 0 | 0 |
| 28 | 0 | - | 0 | 0 |
| 29 | 0 | - | 0 | 0 |
| 30 | 0 | - | 0 | 0 |
| 31 | 0 | - | 0 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 0 | - | 0 | 0 |
| 1 | 0 | - | 0 | 0 |
| 2 | 0 | - | 0 | 0 |
| 3 | 1 | b | BLOCK 163 WORD 0 - 255 | 0 |
| 4 | 0 | - | 0 | 0 |
| 5 | 0 | - | 0 | 0 |
| 6 | 0 | - | 0 | 0 |
| 7 | 0 | - | 0 | 0 |
| 8 | 0 | - | 0 | 0 |
| 9 | 0 | - | 0 | 0 |
| 10 | 0 | - | 0 | 0 |
| 11 | 0 | - | 0 | 0 |
| 12 | 0 | - | 0 | 0 |
| 13 | 0 | - | 0 | 0 |
| 14 | 0 | - | 0 | 0 |
| 15 | 0 | - | 0 | 0 |
| 16 | 0 | - | 0 | 0 |
| 17 | 0 | - | 0 | 0 |
| 18 | 0 | - | 0 | 0 |
| 19 | 0 | - | 0 | 0 |
| 20 | 0 | - | 0 | 0 |
| 21 | 0 | - | 0 | 0 |
| 22 | 0 | - | 0 | 0 |
| 23 | 0 | - | 0 | 0 |
| 24 | 0 | - | 0 | 0 |
| 25 | 0 | - | 0 | 0 |
| 26 | 0 | - | 0 | 0 |
| 27 | 0 | - | 0 | 0 |
| 28 | 0 | - | 0 | 0 |
| 29 | 0 | - | 0 | 0 |
| 30 | 0 | - | 0 | 0 |
| 31 | 0 | - | 0 | 0 |

c) Screenshot showing hit and miss rates

**Statistics**

**Hit Rate :** 0%

**Miss Rate :** 100%

**List of Previous Instructions :**

- Load 1C323 [Miss]
- Load 920C [Miss]
- Load 8E5 [Miss]
- Load F837 [Miss]
- Load D41A [Miss]
- Load 17781 [Miss]
- Load 1A24F [Miss]
- Load B1A9 [Miss]
- Load 18462 [Miss]
- Load 163E5 [Miss]

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|---|---|---|

Week#____8_____ Number: ___5__

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines

Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.

The cache is mapped as

a) Direct Mapped

Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 3 bit | 2 bit | 1 bit |

Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 0 | - | 0 | 0 |
| 1 | 1 | 101 | BLOCK 15 WORD 0 - 1 | 0 |
| 2 | 1 | 001 | BLOCK 6 WORD 0 - 1 | 0 |
| 3 | 1 | 101 | BLOCK 17 WORD 0 - 1 | 0 |

**Statistics**

**Hit Rate : 0%**

**Miss Rate : 100%**

**List of Previous Instructions :**

- **Load 3C [Miss]**
- **Load 1F [Miss]**
- **Load 34 [Miss]**
- **Load 17 [Miss]**
- **Load 37 [Miss]**
- **Load 22 [Miss]**
- **Load 26 [Miss]**
- **Load C [Miss]**
- **Load 2E [Miss]**
- **Load 2B [Miss]**

b) Two way set Associative

## Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 4 bit | 1 bit | 1 bit |

### Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 3 | BLOCK 6 WORD 0 - 1 | 0 |
| 1 | 1 | a | BLOCK 15 WORD 0 - 1 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | d | BLOCK 1A WORD 0 - 1 | 0 |
| 1 | 1 | b | BLOCK 17 WORD 0 - 1 | 0 |

**Statistics**

**Hit Rate :** **0%**

**Miss Rate :** **100%**

**List of Previous Instructions :**

- **Load 3C [Miss]**
- **Load 1F [Miss]**
- **Load 34 [Miss]**
- **Load 17 [Miss]**
- **Load 37 [Miss]**
- **Load 22 [Miss]**
- **Load 26 [Miss]**
- **Load C [Miss]**
- **Load 2E [Miss]**
- **Load 2B [Miss]**

c) Four Way Set associative

## Instruction Breakdown

| TAG | INDEX | OFFSET |
|---|---|---|
| 5 bit | 0 bit | 1 bit |

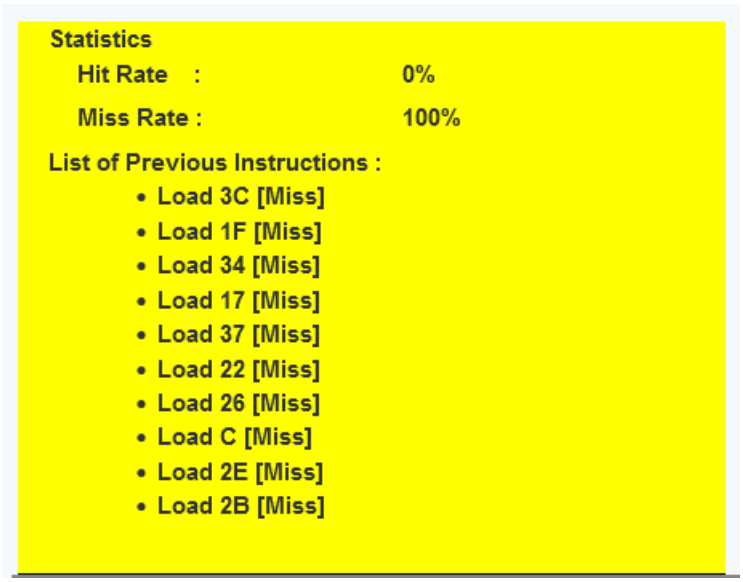
### Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 17 | B. 17 W. 0 - 1 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 15 | B. 15 W. 0 - 1 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 13 | B. 13 W. 0 - 1 | 0 |

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 6 | B. 6 W. 0 - 1 | 0 |




d) Fully Associative

## Instruction Breakdown

| BLOCK | OFFSET |
|---|---|
| 5 bit | 1 bit |

## Cache Table

| Index | Valid | Tag | Data (Hex) | Dirty Bit |
|---|---|---|---|---|
| 0 | 1 | 10111 | BLOCK 17 WORD 0 - 1 | 0 |
| 1 | 1 | 10101 | BLOCK 15 WORD 0 - 1 | 0 |
| 2 | 1 | 10011 | BLOCK 13 WORD 0 - 1 | 0 |
| 3 | 1 | 00110 | BLOCK 6 WORD 0 - 1 | 0 |

**Statistics**

**Hit Rate :** 0%

**Miss Rate :** 100%

**List of Previous Instructions :**

- Load 3C [Miss]
- Load 1F [Miss]
- Load 34 [Miss]
- Load 17 [Miss]
- Load 37 [Miss]
- Load 22 [Miss]
- Load 26 [Miss]
- Load C [Miss]
- Load 2E [Miss]
- Load 2B [Miss]

**Next Index:** 2

**Last Index:** 1

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

b) Screenshot showing the Cache Table

c) Screenshot showing hit and miss rates

**Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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