

# Microprocessor and Computer Architecture

UE21CS251B

4th Semester, Academic Year 2022-23

Date: 20/01/23

|                     |                       |               |
|---------------------|-----------------------|---------------|
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|---------------------|-----------------------|---------------|

Week# \_\_\_\_1\_\_\_\_ Program Number: \_\_\_\_1\_\_\_\_

Title of the Program

**Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0**

I. ARM Assembly Code:

```
.text
LDR R0,=a
LDR R0,[R0]
ANDS R1,R0,#1
BEQ even
BNE odd
even:
    MOV R2,#0
    B end
odd:
    MOV R2,#255
    B end
end:
.data
a: .word 20
.end
```

II. Output Screen Shot (Two):

RegistersView

General Purpose

Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000  
R1 : 00000000  
R2 : 00000000  
R3 : 00000000  
R4 : 00000000  
R5 : 00000000  
R6 : 00000000  
R7 : 00000000  
R8 : 00000000  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00011400  
-----  
CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 0  
Overflow (V) : 0  
IRQ Disable : 1  
FIQ Disable : 1  
Thumb (T) : 0  
CPU Mode : System  
-----

CodeView

P1.o

```

.text
00001000:E59F001C LDR R0,=a
00001004:E5900000 LDR R0, [R0]
00001008:E2101001 ANDS R1,R0,#1
0000100C:0A000000 BEQ even
00001010:1A000001 BNE odd
even:
00001014:E3A02000 MOV R2,#0
00001018:EA000001 B end
odd:
0000101C:E3A020FF MOV R2, #255
00001020:EAF00000 B end
end:
.data
00001028:00000014 a: .word 20
.end...

```

RegistersView

General Purpose

Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 :00000015  
R1 :00000001  
R2 :000000ff  
R3 :00000000  
R4 :00000000  
R5 :00000000  
R6 :00000000  
R7 :00000000  
R8 :00000000  
R9 :00000000  
R10 (s1) :00000000  
R11 (fp) :00000000  
R12 (ip) :00000000  
R13 (sp) :00011400  
R14 (lr) :00000000  
R15 (pc) :00011400

CPSR Register

Negative (N) :0

Zero (Z) :0

Carry (C) :0

Overflow (V) :0

IRQ Disable:1

FIQ Disable:1

Thumb (T) :0

CPU Mode :System

CodeView

P1.o

```

.text
00001000:E59F001C LDR R0,=a
00001004:E5900000 LDR R0, [R0]
00001008:E2101001 ANDS R1,R0,#1
0000100C:0A000000 BEQ even
00001010:1A000001 BNE odd
even:
00001014:E3A02000 MOV R2,#0
00001018:EA000001 B end
odd:
0000101C:E3A020FF MOV R2, #255
00001020:EAF00000 B end
end:
.data
a: .word 21
.end...
00001028:00000015

```

The output should be verified for both even and odd numbers.

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Week# \_\_\_\_1\_\_\_\_ Program Number: \_\_\_\_2\_\_\_\_

Title of the Program

**Write an ALP to compare the value of R0 and R1, add if R0  
= R1, else subtract**

I.ARM Assembly Code:

```
.text
LDR R0, =a
LDR R1, =b
LDR R0, [R0]
LDR R1, [R1]
CMP R0, R1
ADDEQ R2, R1, R0
SUBNE R2, R1, R0

.data
a: .word 20
b: .word 20
.end
```

II. Output Screen Shot (Two):

RegistersView

General Purpose

Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000  
R1 : 00000000  
R2 : 00000028  
R3 : 00000000  
R4 : 00000000  
R5 : 00000000  
R6 : 00000000  
R7 : 00000000  
R8 : 00000000  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00011400  


---

CPSR Register  
Negative (N) : 0  
Zero (Z) : 1  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable: 1  
FIQ Disable: 1  
Thumb (T) : 0  
CPU Mode : System

CodeView

P2.o

```

.text
00001000:E59F0014 LDR R0, =a
00001004:E59F1014 LDR R1, =b
00001008:E5900000 LDR R0, [R0]
0000100C:E5911000 LDR R1, [R1]
00001010:E1500001 CMP R0,R1
00001014:00812000 ADDEQ R2,R1,R0
00001018:10412000 SUBNE R2,R1,R0

.data
00001024:00000014 a: .word 20
00001028:00000014 b: .word 20
.end...

```

RegistersView

General Purpose

Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000014  
R1 : 0000000a  
R2 : ffffffff6  
R3 : 00000000  
R4 : 00000000  
R5 : 00000000  
R6 : 00000000  
R7 : 00000000  
R8 : 0000005a  
R9 : 00000000  
R10 (s1) : 00000000  
R11 (fp) : 00000000  
R12 (ip) : 00000000  
R13 (sp) : 00011400  
R14 (lr) : 00000000  
R15 (pc) : 00011400  


---

CPSR Register  
Negative (N) : 0  
Zero (Z) : 0  
Carry (C) : 1  
Overflow (V) : 0  
IRQ Disable: 1  
FIQ Disable: 1  
Thumb (T) : 0  
CPU Mode : System

CodeView

P2.o

```

.text
00001000:E59F0014 LDR R0, =a
00001004:E59F1014 LDR R1, =b
00001008:E5900000 LDR R0, [R0]
0000100C:E5911000 LDR R1, [R1]
00001010:E1500001 CMP R0,R1
00001014:00812000 ADDEQ R2,R1,R0
00001018:10412000 SUBNE R2,R1,R0

.data
00001024:00000014 a: .word 20
00001028:0000000A b: .word 10
.end...

```

The output should be verified for both equal and nor equal values

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|---------------------|-----------------------|------------|

Week# \_\_\_\_1\_\_\_\_

Program Number: \_\_\_\_3\_\_\_\_

Title of the Program

**Based on the value of the number in R0, Write an ALP to store 1 in R1 if R0 is zero, Store 2 in R1 if R0 is positive, Store 3 in R1 if R0 is negative. (Program shown in class)**

I.ARM Assembly Code:

```
.text
LDR R0, =a
LDR R0, [R0]
CMP R0, #0

ZERO:
    BNE NEGATIVE
    MOV R1, #1
    B end

NEGATIVE:
    BPL POS
    MOV R1, #3
    B end

POS:
    MOV R1, #2
```

```
end:  
.data  
a: .word -2  
  
.end
```

## II. Output Screen Shot (Three):

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000000

R1 : 00000001

R2 : 00000000

R3 : 00000000

R4 : 00000000

R5 : 00000000

R6 : 00000000

R7 : 00000000

R8 : 00000000

R9 : 00000000

R10 (s1) : 00000000

R11 (fp) : 00000000

R12 (ip) : 00000000

R13 (sp) : 00011400

R14 (lr) : 00000000

R15 (pc) : 00001014

CPSR Register

Negative (N) : 0

Zero (Z) : 1

Carry (C) : 1

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : System

CodeView

P2.o

.text

00001000:E59F0020 LDR R0, =a

00001004:E5900000 LDR R0, [R0]

00001008:E3500000 CMP R0, #0

ZERO:

0000100C:1A000001 BNE NEGATIVE

00001010:E3A01001 MOV R1, #1

00001014:EA000003 B end

NEGATIVE:

00001018:5A000001 BPL POS

0000101C:E3A01003 MOV R1, #3

00001020:EA000000 B end

POS:

00001024:E3A01002 MOV R1, #2

end:

.data

0000102C:00000000 a: .word 0

.end

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00000004

R1 : 00000002

R2 : 00000000

R3 : 00000000

R4 : 00000000

R5 : 00000000

R6 : 00000000

R7 : 00000000

R8 : 00000012

R9 : 00000000

R10 (s1) : 00000000

R11 (fp) : 00000000

R12 (ip) : 00000000

R13 (sp) : 00011400

R14 (lr) : 00000000

R15 (pc) : 00011400

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 1

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : System

CodeView

P2.o

.text

00001000:E59F0020 LDR R0, =a

00001004:E5900000 LDR R0, [R0]

00001008:E3500000 CMP R0, #0

ZERO:

0000100C:1A000001 BNE NEGATIVE

00001010:E3A01001 MOV R1, #1

00001014:EA000003 B end

NEGATIVE:

00001018:5A000001 BPL POS

0000101C:E3A01003 MOV R1, #3

00001020:EA000000 B end

POS:

00001024:E3A01002 MOV R1, #2

end:

.data

0000102C:00000004 a: .word 4

.end



RegistersView

General Purpose

Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : ffffffff

R1 : 00000003

R2 : 00000000

R3 : 00000000

R4 : 00000000

R5 : 00000000

R6 : 00000000

R7 : 00000000

R8 : 00000000

R9 : 00000000

R10 (s1) : 00000000

R11 (fp) : 00000000

R12 (ip) : 00000000

R13 (sp) : 00011400

R14 (lr) : 00001031

R15 (pc) : 0000202e

CPSR Register

Negative (N) : 1

Zero (Z) : 0

Carry (C) : 1

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 1

CPU Mode : System

CodeView

P2.o

.text

00001000:E59F0020 LDR R0, =a

00001004:E5900000 LDR R0, [R0]

00001008:E3500000 CMP R0, #0

ZERO:

0000100C:1A000001 BNE NEGATIVE

00001010:E3A01001 MOV R1, #1

00001014:EA000003 B end

NEGATIVE:

00001018:5A000001 BPL POS

0000101C:E3A01003 MOV R1, #3

00001020:EA000000 B end

POS:

00001024:E3A01002 MOV R1, #2

end:

.data

a: .word -2

.end

The output should be verified for zero, positive and negative cases.

### Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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