Assignment 4 - Pipelined CPU

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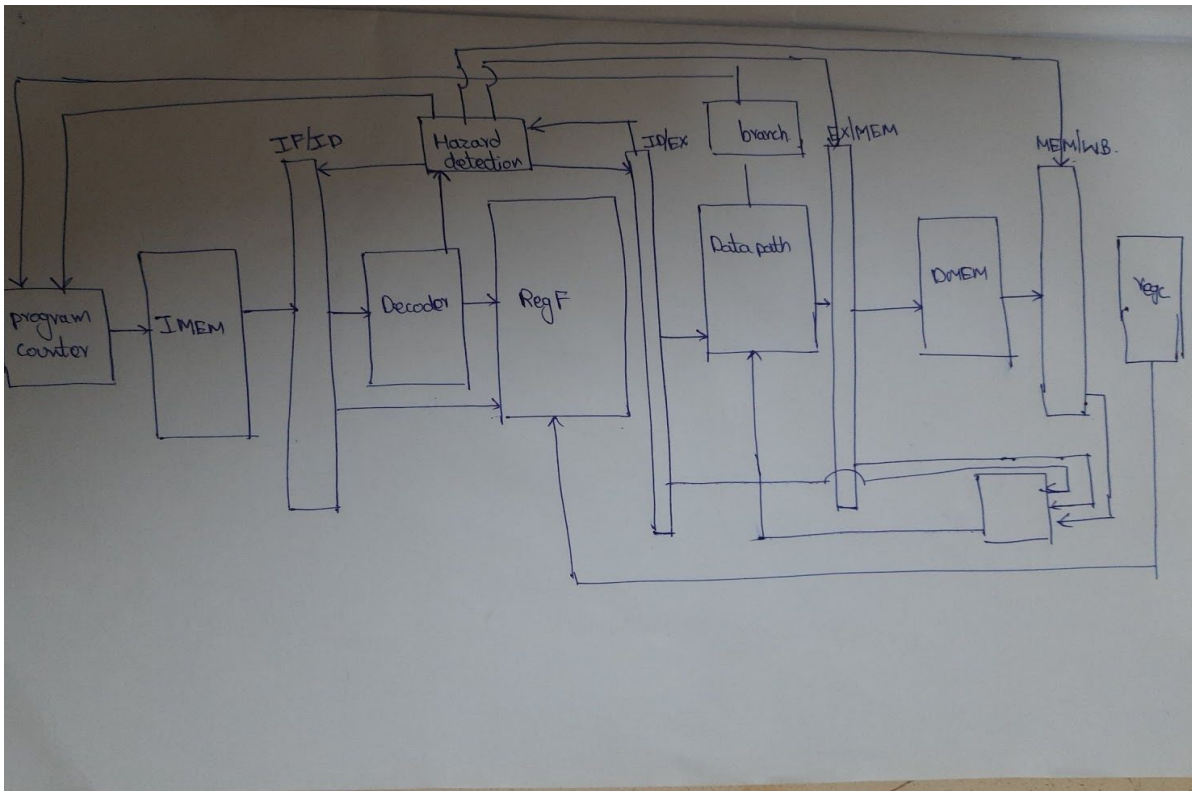
Work Division

For this assignment base code for all the modules is taken from Nikhil and reviewed by Kushal for the proper splitting of modules for which he made some changes accordingly. Then we both discussed the possible implementation methods and came with a code without any forwarding, hazard detection or branch stalling. To solve control and data hazards we used methods discussed in Patterson and Hennessy's book and implemented them with some minor changes



Block diagram of pipelined CPU showing modules used in the assignment