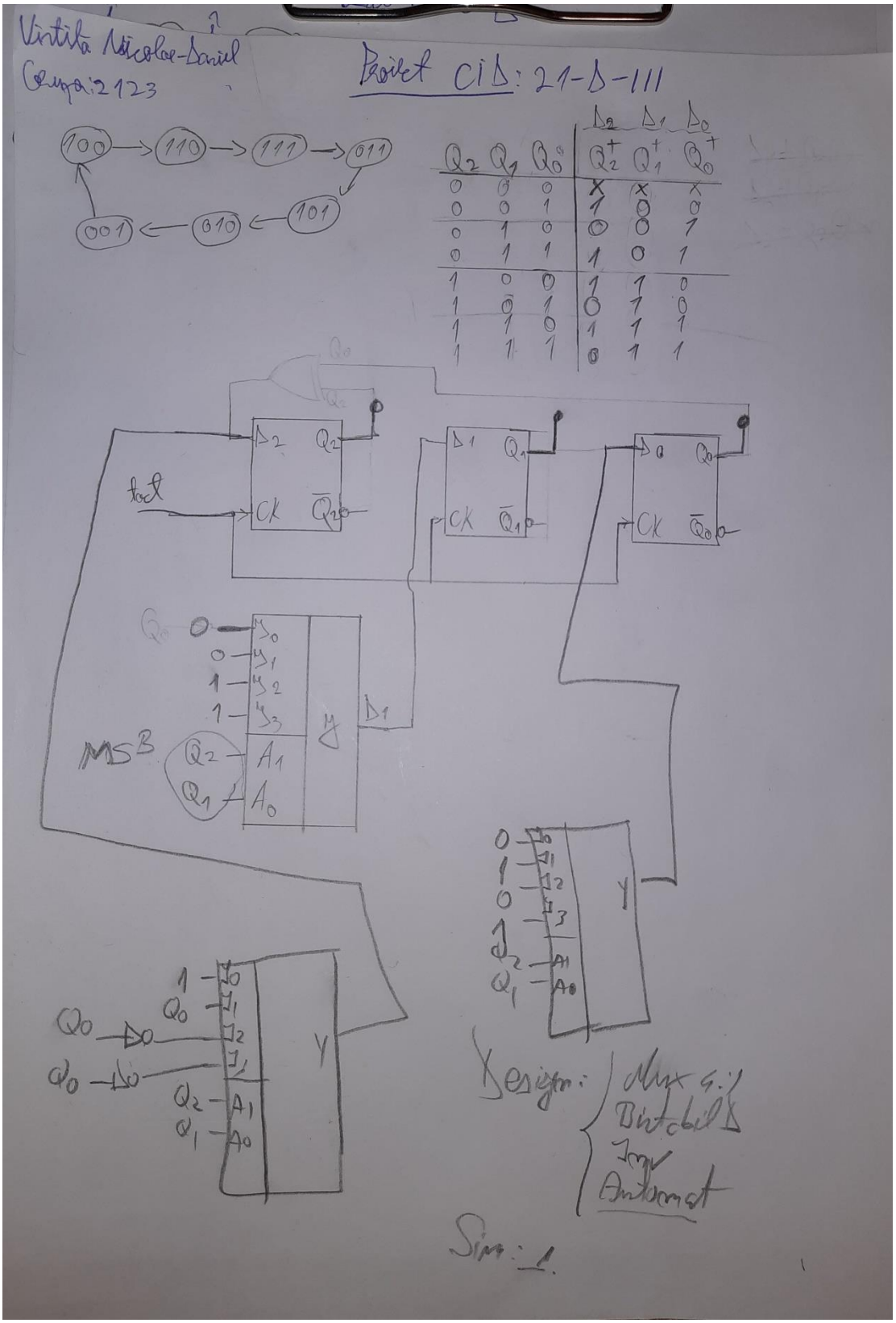
Proiect CID
Automat Bistabile

Vintila Nicolae-Daniel

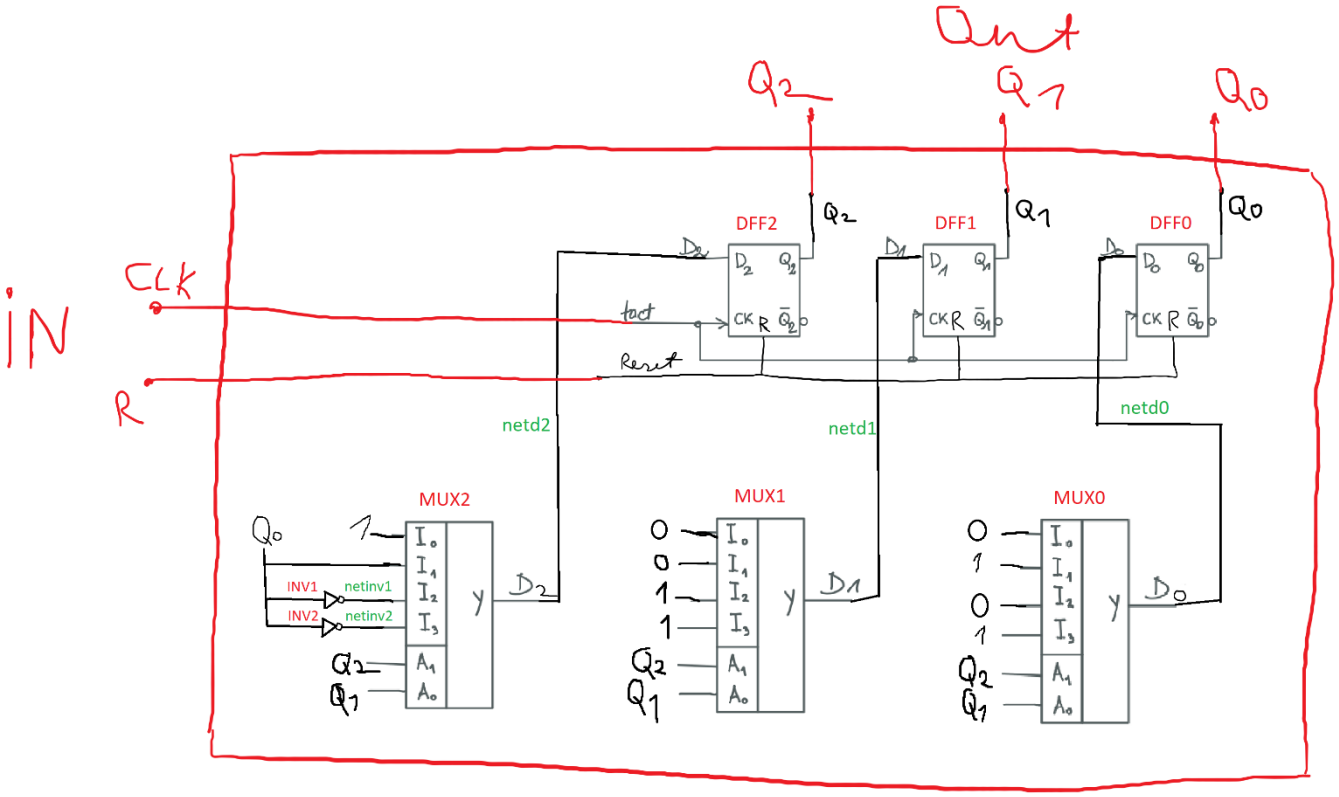
Grupa: 2123

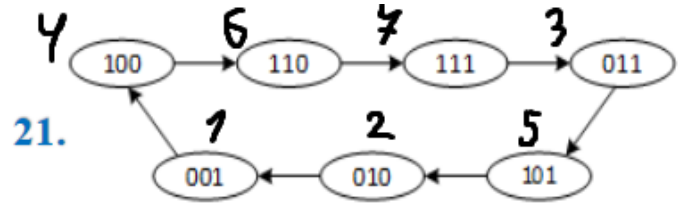
Proiect: 21-D-III

1) Rezolvarea pe hartie a temei de proiect



2) Circuitul pentru implementarea in Vivado si tabelul de adevar





21.

D.

r	clk	Action
1	x	Reset
0	↑	$Q^+ = D$
otherwise		Wait

III. MUX 4:1 și porți logice

3) Implementarea componentelor (Bistabilul D, MUX, Poarta inversor)

DFF.vhd | INV.vhd | MUX4.vhd | automat.vhd

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity DFF is
5      Port ( d : in STD_LOGIC;
6             clk : in STD_LOGIC;
7             r : in STD_LOGIC;
8             q : out STD_LOGIC;
9             qn : out STD_LOGIC);
10 end DFF;
11
12 architecture Behavioral of DFF is
13 begin
14
15 process(clk, r)
16 begin
17     if r='1' then
18             q <= '0';
19             qn <= '1';
20
21    elsif falling_edge(clk) then
22             q <= d;
23             qn <= not d;
24    end if;
25
26 end process;
27
28 end Behavioral;
```

DFF.vhd | INV.vhd | MUX4.vhd | aut

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity INV is
5      Port ( a : in STD_LOGIC;
6             y : out STD_LOGIC);
7  end INV;
8
9  architecture Behavioral of INV is
10
11 begin
12
13 y <= not a;
14
15 end Behavioral;
```

DFF.vhd | INV.vhd | MUX4.vhd | automat.vhd

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity MUX4 is
5      Port ( i0 : in STD_LOGIC;
6             i1 : in STD_LOGIC;
7             i2 : in STD_LOGIC;
8             i3 : in STD_LOGIC;
9             a1 : in STD_LOGIC;
10            a0 : in STD_LOGIC;
11            y : out STD_LOGIC);
12 end MUX4;
13
14 architecture Behavioral of MUX4 is
15
16 signal a: std_logic_vector (1 downto 0);
17 begin
18
19 a <= a1 & a0;
20
21 with a  select
22 y <= i0 when "00",
23      i1 when "01",
24      i2 when "10",
25      i3 when "11",
26      i0 when others;
27
28
29 end Behavioral;
30
```

4) Implementarea sursei automatului

DFF.vhd | INV.vhd | MUX4.vhd | **automat.vhd** | Test_aut

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity automat is
5      Port ( clk : in STD_LOGIC;
6             r : in STD_LOGIC;
7             q : out STD_LOGIC_VECTOR (2 downto 0));
8  end automat;
9
10 architecture Behavioral of automat is
11
12 component  DFF is
13     Port ( d : in STD_LOGIC;
14            clk : in STD_LOGIC;
15            r : in STD_LOGIC;
16            q : out STD_LOGIC;
17            qn : out STD_LOGIC);
18 end component DFF;
19
20 component MUX4 is
21     Port ( i0 : in STD_LOGIC;
22            i1 : in STD_LOGIC;
23            i2 : in STD_LOGIC;
24            i3 : in STD_LOGIC;
25            a1 : in STD_LOGIC;
26            a0 : in STD_LOGIC;
27            y : out STD_LOGIC);
28 end component MUX4;
29
30 component INV is
31     Port ( a : in STD_LOGIC;
32            y : out STD_LOGIC);
33 end component INV;
34
35 signal netd0, netd1, netd2, netinv1, netinv2:std_logic;
36 signal qint:std_logic_vector(2 downto 0);
37
38 begin
39 q <= qint;
40
41 DFF0: DFF port map( clk => clk,
42                     r => r,
43                     d => netd0,
44                     q => qint(0));
```

DFF.vhd | INV.vhd | MUX4.vhd | automat

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```
44                      q => qint(0));
45
46 DFF1: DFF port map ( clk => clk,
47                      r => r,
48                      d => netd1,
49                      q => qint(1));
50
51 DFF2: DFF port map ( clk => clk,
52                      r => r,
53                      d => netd2,
54                      q => qint(2));
55
56 MUX0: MUX4 port map (i0 => '0',
57                      i1 => '1',
58                      i2 => '0',
59                      i3 => '1',
60                      a1 => qint(2),
61                      a0 => qint(1),
62                      y => netd0);
63
64 MUX1: MUX4 port map (i0 => '0',
65                      i1 => '0',
66                      i2 => '1',
67                      i3 => '1',
68                      a1 => qint(2),
69                      a0 => qint(1),
70                      y => netd1);
71
72 MUX2: MUX4  port map (i0 => '1',
73                       i1 => qint(0),
74                       i2 => netinv1,
75                       i3 => netinv2,
76                       a1 => qint(2),
77                       a0 => qint(1),
78                       y => netd2);
79
80 INV1: INV port map (a => qint(0),
81                     y => netinv1);
82
83 INV2: INV port map (a => qint(0),
84                     y => netinv2);
85
86 end Behavioral;
87
```

5) Implementarea sursei de simulare a automatului

Test_automat.vhd | DFF.vhd | INV.vhd | MUX4.vhd

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```
1
2   library IEEE;
3   use IEEE.STD_LOGIC_1164.ALL;
4
5   entity Test_automat is
6   --  Port ( );
7   end Test_automat;
8
9   architecture Behavioral of Test_automat is
10
11  component automat is
12      Port ( clk : in STD_LOGIC;
13             r : in STD_LOGIC;
14             q : out STD_LOGIC_VECTOR (2 downto 0));
15  end component automat;
16
17  signal clk, r:std_logic;
18  signal q: std_logic_vector (2 downto 0);
19  begin
20
21  UUT: automat port map(clk, r, q);
22
23  process
24  begin
25     clk <= '0'; wait for 1 ns;
26     clk <= '1'; wait for 1 ns;
27  end process;
28
29  r <= '1' after 0 ns, '0' after 2.2 ns;
30
31  end Behavioral;
32
```

6) Implementarea sursei de simulare a bistabilului si portii inversoare

Test_BIST_D.vhd * | Test_MUX4.vhd | Test_inv.vhd

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity Test_BIST_D is
5  --  Port ( );
6  end Test_BIST_D;
7
8  architecture Behavioral of Test_BIST_D is
9
10 component DFF is
11     Port ( d : in STD_LOGIC;
12            clk : in STD_LOGIC;
13            r : in STD_LOGIC;
14            q : out STD_LOGIC;
15            qn : out STD_LOGIC);
16 end component DFF;
17
18 signal d, clk, r, q, qn:std_logic;
19
20 begin
21
22 UUT: DFF port map(d, clk, r, q, qn);
23
24 process
25 begin
26 clk <= '0'; wait for 1 ns;
27 clk <= '1'; wait for 1 ns;
28 end process;
29
30 process
31 begin
32 d <= '0'; wait for 3.8 ns;
33 d <= '1'; wait for 3.8 ns;
34 end process;
35
36 r <= '1' after 0 ns, '0' after 2.3 ns;
37
38 end Behavioral;
```

Test_BIST_D.vhd | Test_inv.vhd | Test_MUX4

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```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity Test_inv is
5  --  Port ( );
6  end Test_inv;
7
8  architecture Behavioral of Test_inv is
9
10 component  INV is
11     Port ( a : in STD_LOGIC;
12            y : out STD_LOGIC);
13 end component INV;
14
15 signal a, y:std_logic;
16
17 begin
18
19 UT: INV port map (a, y);
20
21 process
22 begin
23 a <= '0'; wait for 2 ns;
24 a <= '1'; wait for 2 ns;
25 end process;
26
27 end Behavioral;
```

7) Implementarea sursei de simulare a multiplexorului 4:1

Test_BIST_D.vhd | **Test_MUX4.vhd** | Test_inv.vhd

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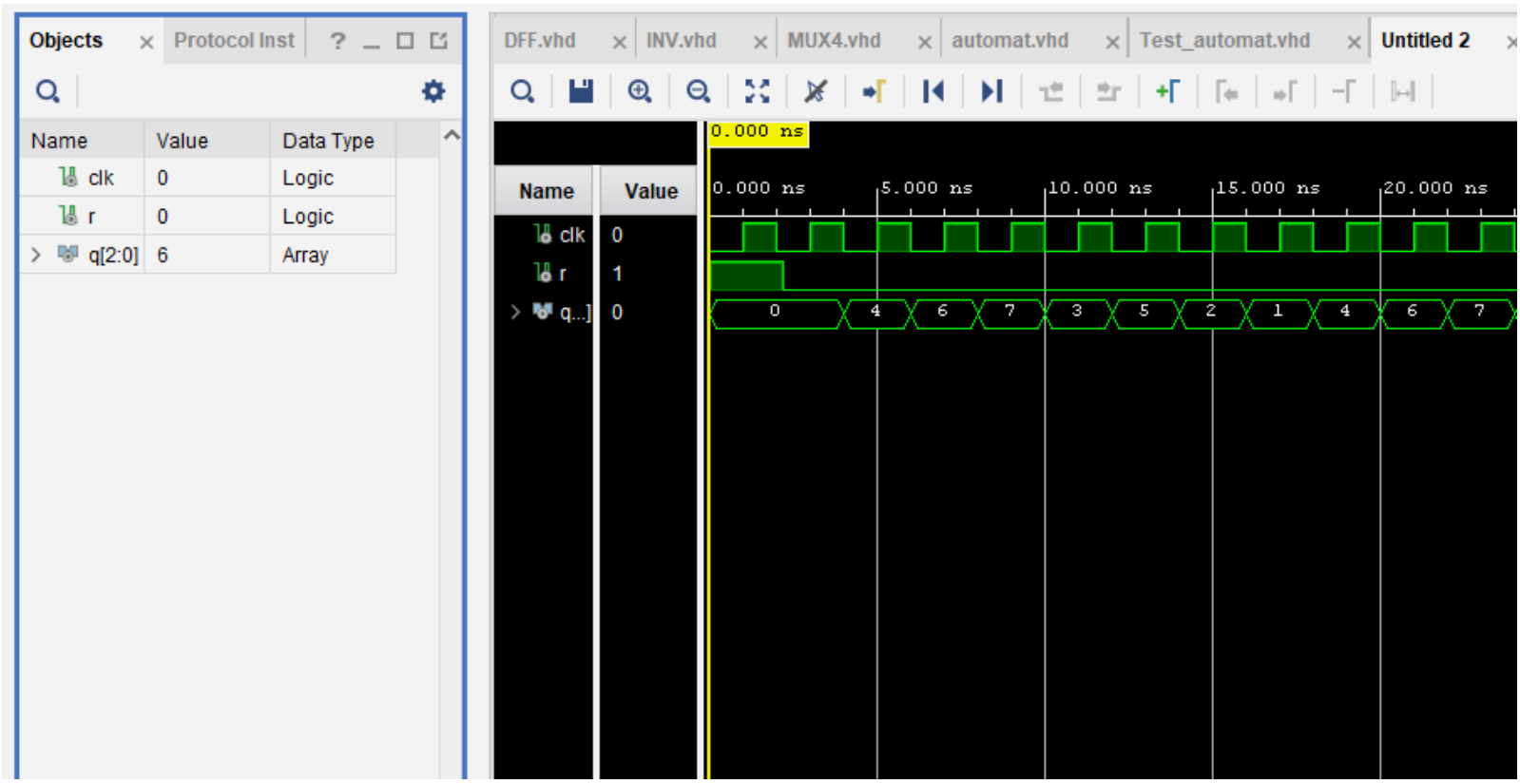
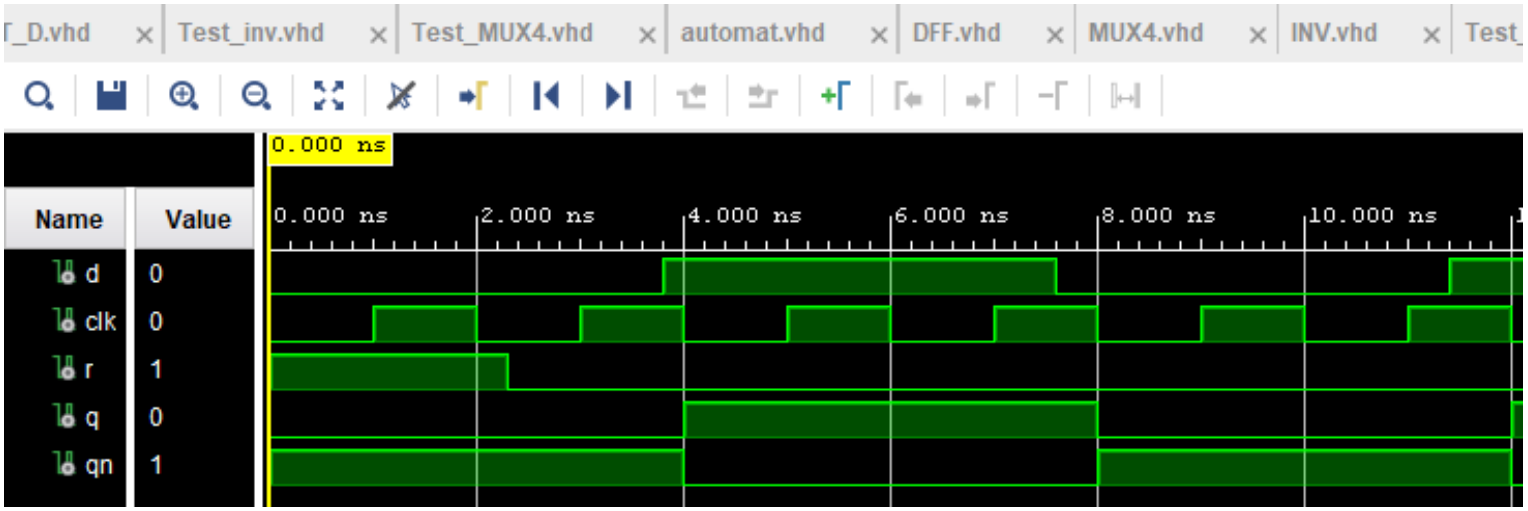
```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity Test_MUX4 is
5  --  Port ( );
6  end Test_MUX4;
7
8  architecture Behavioral of Test_MUX4 is
9
10 component  MUX4 is
11     Port ( i0 : in STD_LOGIC;
12            i1 : in STD_LOGIC;
13            i2 : in STD_LOGIC;
14            i3 : in STD_LOGIC;
15            a1 : in STD_LOGIC;
16            a0 : in STD_LOGIC;
17            y : out STD_LOGIC);
18 end component MUX4;
19
20 signal i0, i1, i2, i3, a1, a0, y: std_logic;
21
22 begin
23 UT: MUX4 port map(i0, i1, i2, i3, a1, a0, y);
24
25 process
26 begin
27 a0 <= '0'; wait for 2 ns;
28 a0 <= '1'; wait for 2 ns;
29 end process;
30
31 process
32 begin
33 a1 <= '0'; wait for 3 ns;
34 a1 <= '1'; wait for 3 ns;
35 end process;
36
37 process
38 begin
39 i0 <= '0'; wait for 4 ns;
40 i0 <= '1'; wait for 4 ns;
41 end process;
42
43 process
44 begin
45 i1 <= '0'; wait for 5 ns;
46 i1 <= '1'; wait for 5 ns;
47 end process;
48
49 process
50 begin
51 i2 <= '0'; wait for 6 ns;
52 i2 <= '1'; wait for 6 ns;
53 end process;
54
55 process
56 begin
57 i3 <= '0'; wait for 7 ns;
58 i3 <= '1'; wait for 7 ns;
59 end process;
60
61 end Behavioral;
62
```

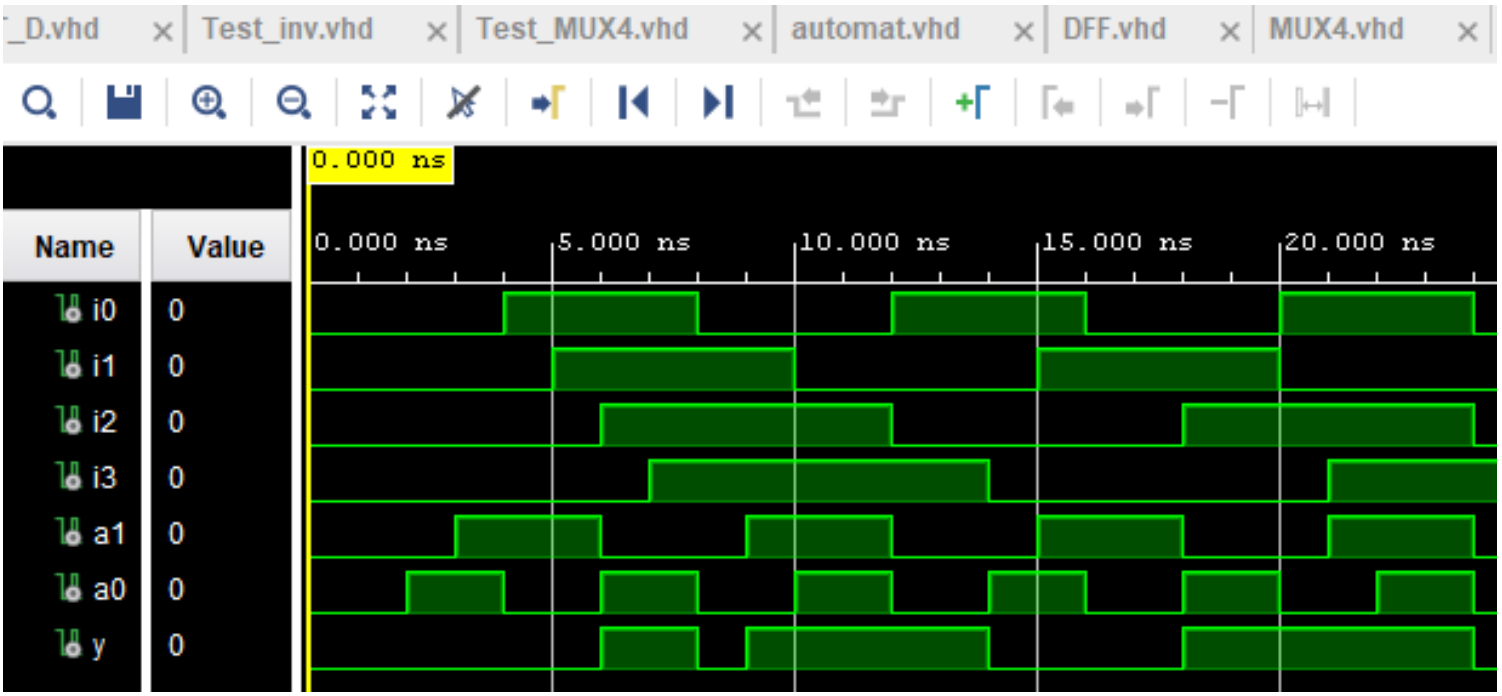
8) Simulare propriu-zisa a automatului



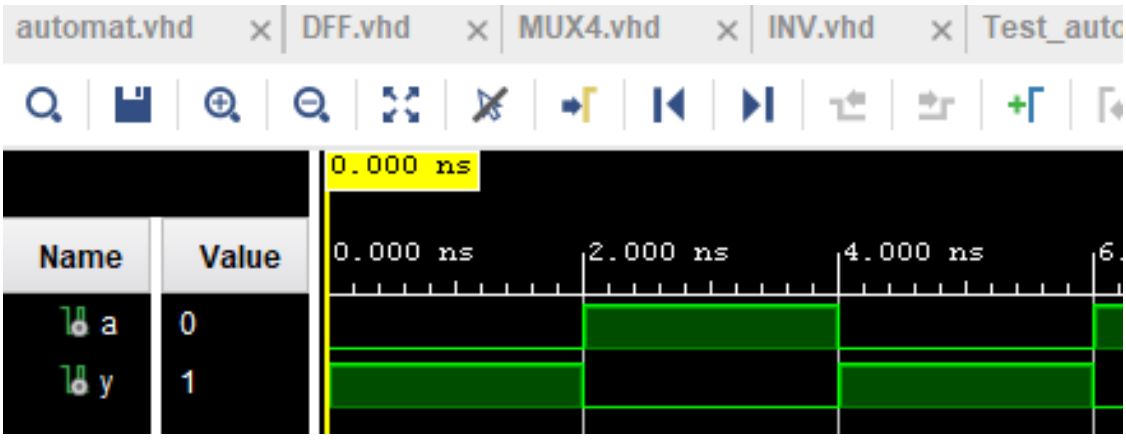
9) Simularea Bistabilului D



10) Simularea multiplexorului 4:1



11) Simularea portii inversoare



Multumesc de atentie!

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Proiect: 21-D-III