A High Gain 0.0831µV/mA Load Regulated Capacitorless LDO With Fast Loop and Nested Miller Compensation (NMC)

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***Abstract*— In recent years, there has been a spike in demand for wearable devices. Low dropout regulators are an integral part of these devices, owing to their high Power Supply Rejection (PSR) and stable output. This paper proposes a high gain, low quiescent current (10.298µA), Output Capacitorless Low Dropout Regulator (OCL-LDO) with a fast local loop and unity feedback. Nested Miller frequency Compensation (NMC) technique is used to stabilize the system. The proposed circuit can operate with a load current ranging from 20µA to 20mA. The design encompasses three gain stages with a total open loop gain of 132 dB resulting in enhanced load regulation (0.0831 µV/mA) and line regulation (0.6917 mV/V). The proposed LDO has been simulated in gpdk 90nm CMOS technology using Cadence Virtuoso. The simulation results demonstrate a PSR of -61.03 dB and -41.17 dB at 1kHz and 10kHz respectively.**

***Index Terms*—Output Capless Low-dropout regulator (OCL-LDO), high gain, fast loop, Nested Miller Compensation (NMC).**

I. Introduction

Most modern electronic devices consist of many high performance and sensitive analog blocks which require a clean supply voltage. These include biomedical implants [1], energy-harvesting systems [2] and wearable devices [3]. Hence, the rippled voltage supplied by switched DC-DC converters and batteries is given to a crucial analog block, the Low Dropout Regulator (LDO), to generate a low ripple output. A conventional LDO consists of an error amplifier, a pass transistor and a resistive feedback network to maintain its output at a certain reference voltage. The pass transistor could be an NMOS switch [4] or a PMOS switch. Although an NMOS pass transistor has a better regulation and transient response, it requires a higher dropout voltage to function which is not preferable for most wearable devices.

Traditional PMOS LDOs (capped) [5], [6] consists of a large capacitor (~1µF) at the output to obtain excellent transient response and stability. Such high capacitors cannot be integrated on-chip, making them bulky off chip components. Portable and wearable devices often have an area limitation, which calls for the design of output capacitorless LDOs (OCL-LDO). Working without a bulky capacitor requires additional fast-loops and advanced compensation techniques to achieve low undershoot-overshoot and good stability. Another key parameter in designing an LDO is the quiescent current, which determines the current efficiency of the block. Low quiescent current gives better current efficiency. The output of the LDO is also provided to ADCs and DACs as their supply voltage which demand sufficient load regulation in order to the maintain conversion accuracy. However, gain of the error amplifier often limits the regulation of the output. This paper presents a high gain capless LDO with a second non-inverting gain stage to overcome this limitation which also poses as a fast loop to improve the overall transient response of the system.

The architectures proposed in [7], [8], [9], [10] and [11] showcase different ways of implementing fast loops that account for better transient response. The commonality among them is that they are all capacitorless designs. The bottleneck of these designs is the high value of quiescent current (>30uA) which is overcome by the proposed LDO architecture without degrading the transient response.

Traditionally, while going from low-to-high load, the undershoot value increases, causing spikes in voltage hence inducing distortion in the system. Having a fast loop poses as an ailment for this drawback. Although the fast loop in [12] provides some fix to the transient response, the proposed LDO design further reduces the undershoot value significantly, thereby providing a better response.

The brief is organized as follows. Section II explains the proposed OCL-LDO architecture along with stability analysis. In Section III, experimental and simulation results are demonstrated. Finally, a conclusion is drawn in Section IV.

II. Proposed LDO with Fast-Loop and NMC

Conventionally, in a two stage LDO, as shown in Fig. 1, a sudden change in the load changes the output voltage V_{OUT}, which is fed back to the Error Amplifier (EA) and the output of the EA is fed to the gate of the pass transistor. This changes the amount of current flowing through the pass branch and regulates the output voltage back to the desired value.

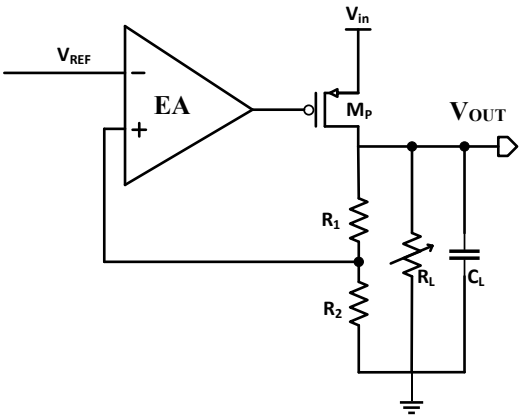

Fig. 1. Conventional PMOS LDO

However, the functionality of this is limited by the gain bandwidth of the EA. One solution is to introduce a fast loop between the EA and the pass transistor, resulting in a three stage LDO.

Fig. 2 shows the structure of the proposed LDO with a fast loop and Nested Miller Compensation (NMC) which consists of an EA, a fast loop and a pass transistor. The proposed structure poses an advantage of using a unity feedback network instead of a conventional resistive feedback network. C_L is the effective on-chip load capacitance, C_2 and C_3 are the capacitors used for Nested Miller Compensation to improve the stability of the system. C_1 is a feedforward capacitor used to enhance the transient response and extend the Unity Gain Bandwidth (UGB) of the system.

The first stage is an n-input folded cascode amplifier consisting of transistors M_0-M_{11} with M_{16} and M_{17} forming the biasing branches with currents of 500nA (I_{B2}) and 1µA (I_{B3}) respectively. The second stage is a non-inverting gain stage consisting of transistors M_{12}-M_{15}. The pass transistor M_p forms the third stage. When there is a sudden change in the load current I_L, the value of V_{OUT} changes. This change is coupled by the capacitor C_2 to M_{12} which changes the V_{gs} of M_{12}. This accounts for the change in current I_3 and the same current is copied to M_{15}. Thus, the node voltage V_X varies and is fed to the pass transistor M_p which thereby alters the current in the pass branch based on the active load, regulating the output voltage back to the desired value. In steady state, the high driving capability of the pass transistor M_p charges the output node rapidly, provided it is properly driven by the previous stage. This way, the second stage acts as a fast loop whenever there is a sudden change in the load current, reducing the undershoot and overshoot of the OCL-LDO.

A. Small Signal Analysis

The small signal analysis of the proposed design in Fig. 3 consists of three gain stages.

The first stage gain is as shown in (1).

$$A_{v1} = g_{m_1} \times (g_{m_7} r_{o_7}(r_{o_1} || r_{o_5}) || g_{m_9} r_{o_9} r_{o_{11}}) \quad (1)$$

The second stage consists of two single stage common source amplifier structures. (2) illustrates the gain provided by this stage.

$$A_{v2} = \frac{g_{m_{12}}}{g_{m_{13}}} \times g_{m_{15}}(r_{o_{15}} || r_{o_{14}}) \quad (2)$$

The third and final stage of the design contributes a gain as expressed in (3).

$$A_{v3} = g_{m_P}(r_{o_P} || R_L) \quad (3)$$

As shown in (1), the cascode structure provides a high single stage gain of 66 dB. The second stage with a gain of 38 dB, further enhances the system gain to 103 dB. Finally, the pass transistor stage provides a gain of 28 dB providing a full system gain of 132 dB. The design incorporates two compensation capacitors connected in nested miller architecture and one feedforward capacitor across the driver MOSFET for stability.

B. Stability Analysis

The small signal modelling of the proposed OCL-LDO as shown in Fig. 3 demonstrates a three-pole system. The output node of the folded cascode amplifier forms the dominant pole. The high resistance due to the cascode structure of the error amplifier along with the miller capacitor C_2 ensures the dominancy of this pole.

The capacitor C_2 connected across second and third gain stages has an effective capacitance as depicted in (4).

$$C_c = C_2 \times \left(\frac{g_{m_{12}}}{g_{m_{13}}} \times g_{m_{15}}(r_{o_{15}} || r_{o_{14}}) \times g_{m_P}(r_{o_P} || R_L) \right) \quad (4)$$

The dominant pole created at the folded cascode output node is shown in (5).

Once the dominant pole is hit, the capacitor C_2 gets shorted, connecting the output of the LDO directly to the input of the second stage. The structure (Fig. 2) now resembles a common source configuration with a gain stage in its negative feedback between the nodes V_{OUT} and V_X. The negative feedback strives to match V_X to V_{OUT} which virtually diode connects the pass transistor, making the miller effect of capacitor C_3 insignificant and giving the non-dominant pole in (6).

$$\omega_{ND} = \frac{1}{2\pi(r_{o_{14}} || r_{o_{15}})(C_3)} \quad (6)$$

Finally, the second non-dominant pole at the output node is given in (7).

$$\omega_{out} = \frac{g_{m_p}}{2\pi C_L} \quad (7)$$

The UGB of the system is evaluated by the equation (8).

$$\omega_{UGB} = \frac{g_{m_1}}{2\pi C_2} \quad (8)$$

$$\omega_{-3dB} = \frac{1}{2\pi(g_{m_7} r_{o_7}(r_{o_1} || r_{o_5}) || g_{m_9} r_{o_9} r_{o_{11}}) \left(C_2 \times \left(\frac{g_{m_{12}}}{g_{m_{13}}} \times g_{m_{15}}(r_{o_{15}} || r_{o_{14}}) \times g_{m_P} r_{o_P} \right) \right)} \quad (5)$$

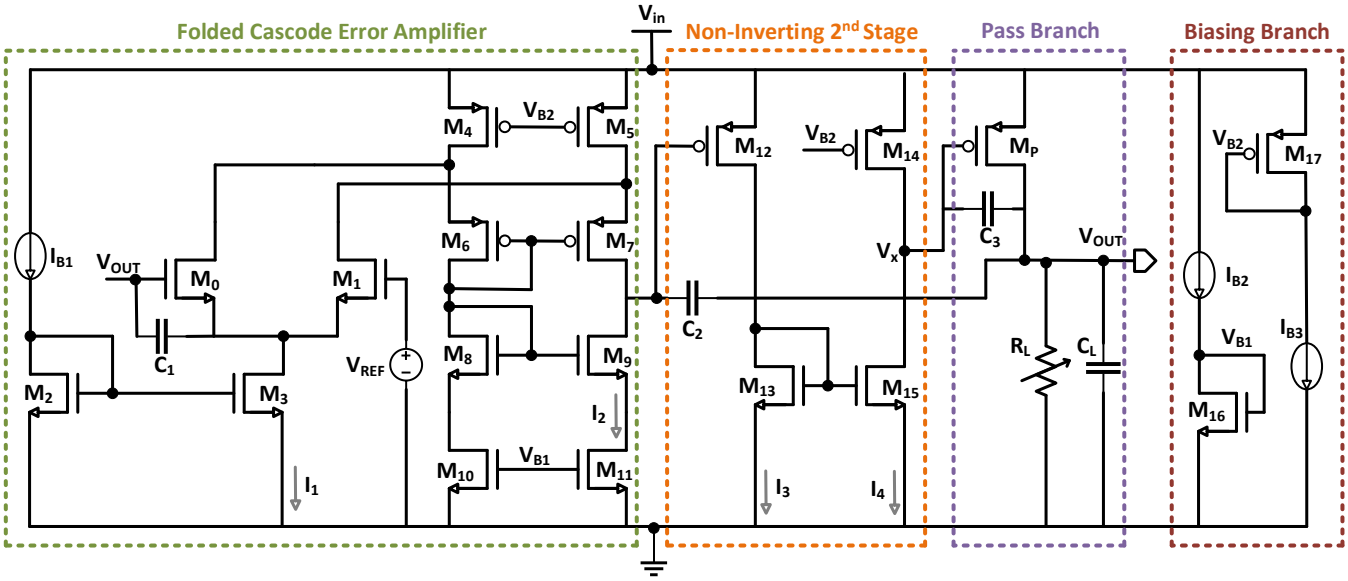

Fig. 2. Schematic of Proposed OCL-LDO with fast loop and NMC

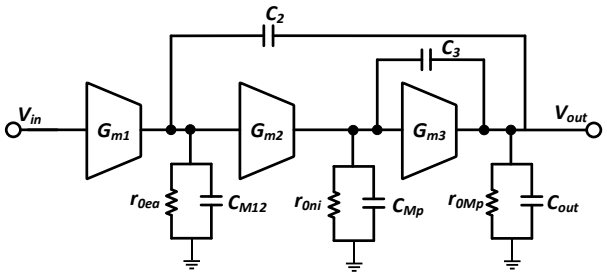

Fig. 3. Small signal model of proposed OCL-LDO

The phase margin of the proposed three pole OCL-LDO is given by the equation (9).

$$PM = 180° - \tan^{-1}\frac{\omega_{UGB}}{\omega_{-3dB}} - \tan^{-1}\frac{\omega_{UGB}}{\omega_{ND}} - \tan^{-1}\frac{\omega_{UGB}}{\omega_{out}} \quad (9)$$

Considering the equations above, the proposed OCL-LDO has been designed for a capacitor C_2 with a value of 2.2pF to push the dominant pole to 277mHz and a UGB of 1MHz. Furthermore, capacitor C_3 from the nested miller structure is designed for 50fF to obtain a non-dominant pole at 7.1MHz, which is considerably away from the UGB and hence does not affect the stability of the system.

The design also consists of a 6pF feedforward capacitor to enhance the transient response of the system. Lastly, the 10pF output capacitor introduces an output pole at 10MHz which is exactly one decade away from ω_{UGB} and does not affect the stability of the system.

The nested miller structure discussed in the proposed OCL-LDO introduces two RHP zeroes which are decades away from the UGB and do not hinder the stability of the system.

Fig. 4 illustrates the corner analysis of gain and phase plots for the proposed OCL-LDO. The design has been verified across the process corners of SS, NN and FF with temperatures ranging from −40℃ to 100℃ with a nominal value of 27 ℃ and a 10% variation in supply voltage sweeping across the voltages 1.62V, 1.8V and 1.98V for a load sweeping across the voltages 1.62V, 1.8V and 1.98V for a load current of 20µA and load capacitance of 10pF. Through these PVT variations, the design exhibits a worst-case phase margin of 61.5°, a worst-case gain of 125 dB and a worst-case UGB of 802kHz.

III. Experimental results

The proposed LDO is simulated in 90 nm CMOS technology using Cadence Virtuoso. The supply voltage given to the LDO is 1.8V and the output is 1.4V with a dropout of 0.4V. The load current varies from 20µA to 20mA with a load capacitance range of 10pF to 100pF. The circuit consumes a maximum quiescent current I_Q of 10.298µA at 20mA load condition and has a maximum current efficiency of 99.94%.

Corner analysis is performed to evaluate the robustness of the proposed design against process, voltage and temperature variations. Fig. 5 shows the gain and phase for a range of currents and it can be observed that the gain is approximately constant throughout the variation and the phase margin is greater than 60° for all currents which implies that the proposed design is a stable system.

Fig. 6 shows the transient response of the proposed LDO when load current changes from 20µA to 20mA with an edge time of 1µs. The undershoot is 102mV while the overshoot is 199mV with a settling time of 2.35µs. As shown in Fig. 7, the undershoot and overshoot of the proposed design is considerably low compared to that of a design without a fast loop.

As shown in Fig. 8 there is no significant variation in output voltage across different currents. The measured load regulation of the system is 0.0831 µV/mA with load current ranging from 20µA to 20mA and V_{OUT} decreasing by 1.66µV approximately, whereas the line regulation with supply voltage varying from 1.62V to 1.98V is 0.6917 mV/V. Fig. 9 shows the line regulation of the system for different input voltages. Both load and line regulation verify the proposed LDO's notable DC characteristics, particularly its high loop gain. Fig. 10 shows the PSR for different currents. The measured PSR is -60.93 dB @ 1kHz for I_L=20µA and -61.03

dB for I_L=20mA, -41.12 dB @ 10kHz for I_L=20µA and -41.17 dB for I_L=20mA, -20.29 dB @ 100kHz for I_L=20µA and -20.35 dB for I_L=20mA. PSR at DC is -75.88 dB at 20mA.

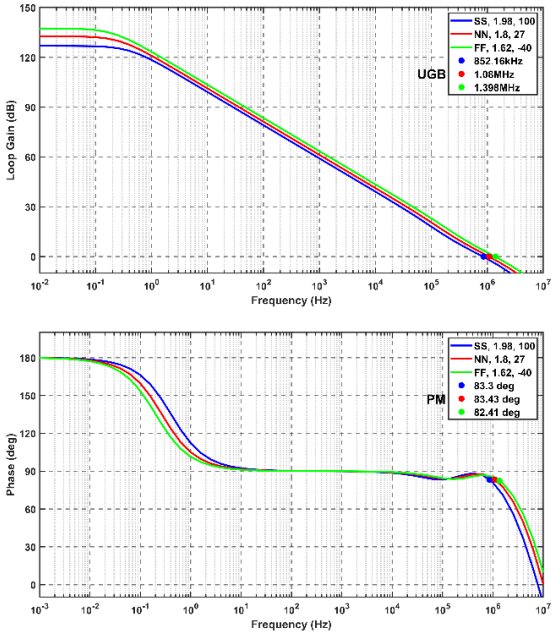

Fig. 4. Gain and Phase plots for corner analysis

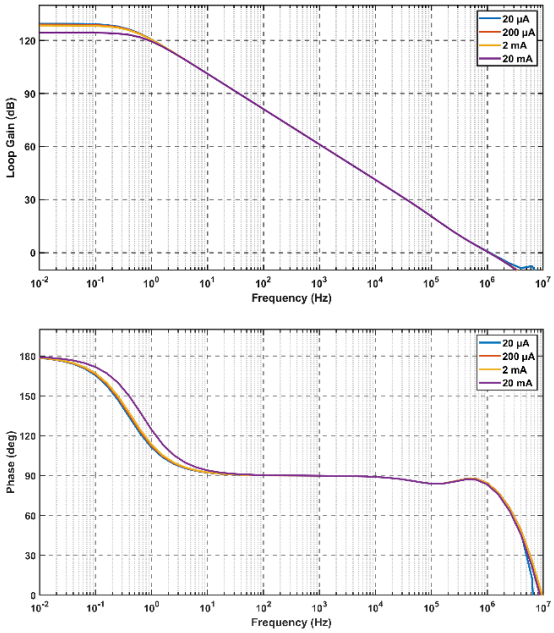

Fig. 5. Gain and Phase plots across load currents

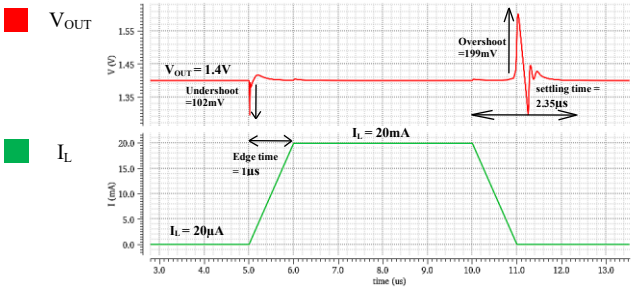

Fig. 6. Transient response of proposed LDO with V_{IN}= 1.8V, C_L= 10pF and I_L = 20µA to 20mA

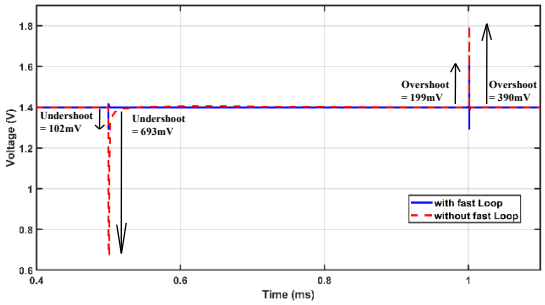

Fig. 7. Transient response of LDO with and without fast loop

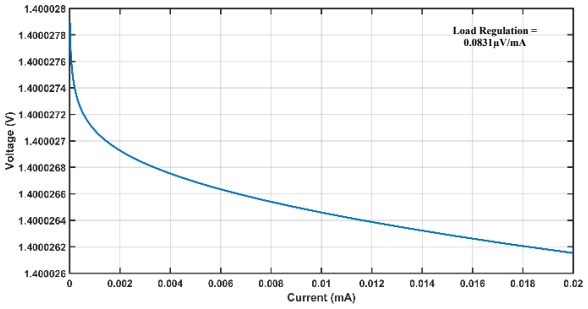

Fig. 8. Load regulation of proposed LDO

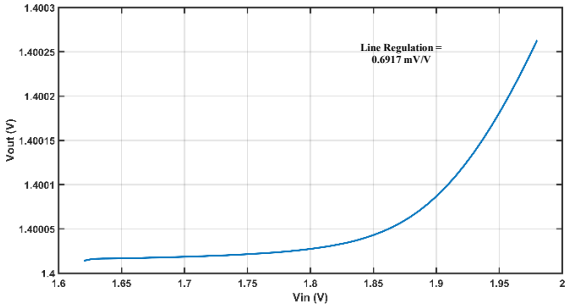

Fig. 9. Line regulation of proposed LDO

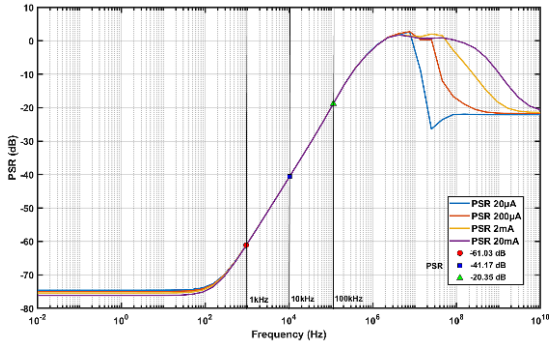

Fig. 10. PSR of proposed LDO for different load currents

Table. I shows the summary of the simulation results in comparison to other state-of-the-art LDOs, which highlights the advantages of the proposed LDO. The suggested LDO offers excellent load and line regulation, as well as PSR even at high frequencies. Furthermore, the quiescent current consumption of the proposed design is roughly constant regardless of the load current unlike [13], [14], [15] where I_Q depends on I_L to some extent.

IV. Conclusion

A high gain output capacitorless Low Dropout Regulator comprising a fast loop and unity gain feedback is presented in this study. The non-inverting gain stage yields notable load and line regulation while improving the transient response of

TABLE. I
PERFORMANCE SUMMARY OF PROPOSED LDO AND COMPARISON WITH STATE-OF-THE-ART LDO

Parameters	[16]	[17]	[18]	[19]	[20]	This work
Year	2018	2020	2022	2024	2024	**2024**
Technology (nm)	500	65	350	65	28	**90**
V_{IN} (V)	2.7	1.05	2.7-3.3	2	0.9	**1.8**
V_{OUT} (V)	2.6	0.9	2.5-3.1	1.8	0.85	**1.4**
Dropout Voltage (mV)	100	150	200	118	50	**400**
I_Q (µA)	107	65	66	110	33	**10.298**
I_{OUT} (min) (µA)	50	100	10	200	0	**20**
I_{OUT} (max) (mA)	100	20	100	50	20	**20**
On-chip Capacitance (pF)	20	1.4	14	10	36	**8.7**
Line Reg. (mV/V)	0.08	NA	0.8	NA	17.5	**0.6912**
Load Reg. (µV/mA)	6	NA	0.06	NA	260	**0.0831**
Overshoot (mV)	200	200	170	128	64	**199**
Undershoot (mV)	296	380	255	96	176	**102**
PSR @ 1kHz	-67.8	-52	-51	-91	NA	**-60.93**
PSR @ 10kHz	NA	-52	-41	NA	NA	**-41.12**
PSR @ 100kHz	NA	-45	-25.7	NA	-30	**-20.29**
Settling time (t_s) (µs)	0.06	0.1	0.7	0.4	0.22	**2.5**

the system by coupling the change in the output hence acting like a fast loop. Subsequently, the proposed design can handle a load current up to 20mA with a current efficiency of 99.94%. The design consumes a total quiescent current of 10.298µA with a notable PSR of -61.03 dB at 1kHz and with overshoot and undershoot values less than 200mV. The achieved specifications are best suited for wearable devices where consumption of low quiescent current is crucial.

REFERENCES

[1] A Low-Power High-Precision Low-Dropout Regulator For Biomedical Implants," 2022 30th International Conference on Electrical Engineering (ICEE), Tehran, Iran, Islamic Republic of, 2022, pp. 857-863. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.

[2] S. -Y. Moon, S. C. Chandrarathna, A. Shafique and J. -W. Lee, "A Compact DC-DC Converter With Pulse-Counting MPPT and Fast One-Path Self-Startup for Thermal Energy Harvesting," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 5, pp. 2457-2470, May 2024 .

[3] T. -H. Chou, S. Yu, S. Bose, J. Cook, J. Park and M. L. Johnston, "Wireless, Multi-Sensor System-on-Chip for pH and Amperometry Powered by Body Heat," in IEEE Transactions on Biomedical Circuits and Systems, vol. 17, no. 4, pp. 782-794, Aug. 2023.

[4] H. Park, W. Jung, M. Kim and H. -M. Lee, "A Wide-Load-Range and High-Slew Capacitor-Less NMOS LDO With Adaptive-Gain Nested Miller Compensation and Pre-Emphasis Inverse Biasing," in IEEE Journal of Solid-State Circuits, vol. 58, no. 10, pp. 2696-2708, Oct. 2023.

[5] The Design of An LDO Regulator [The Analog Mind]," in IEEE Solid State Circuits Magazine, vol. 14, no. 2, pp. 7-17, Spring 2022.

[6] B. Razavi, "The Low Dropout Regulator [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 11, no. 2, pp. 8-13, Spring 2019.

[7] G. Li, H. Qian, J. Guo, B. Mo, Y. Lu, and D. Chen, "Dual Active Feedback Frequency Compensation for Output-Capacitorless LDO With Transient and Stability Enhancement in 65-nm CMOS," IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 415-426, Jan. 2020.

[8] N. Liu and D. Chen, "A Transient-Enhanced Output-Capacitorless LDO With Fast Local Loop and Overshoot Detection," IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 67, no. 10, pp. 3945-3956, Oct. 2020.

[9] X. Ming et al., "A Capacitor-less LDO With Fast-transient Error Amplifier and Push-pull Differentiator," IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018.

[10] A. N. Deleuran, N. Lindbjerg, M. K. Pedersen, P. L. Muntal and I. H. H. Jørgensen, "A capacitor-free, fast transient response linear voltage regulator in a 180nm CMOS," Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), Oslo, Norway, 2015.

[11] R. Wang, J. J. Liou, W. Fan and Y. Wang, "Design of A Fast Transient Response Capacitor-Less LDO with Dual Loop," 10th International Symposium on Next-Generation Electronics (ISNE), Wuxi, China, 2023.

[12] H. Kim, S. S. Kwak and Y. S. Kim, "LDO Regulator Optimized on Power Efficiency and Load Transient Response with Voltage Damper and Body Loop Feedback," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2022.

[13] Y. Huang, Y. Lu, F. Maloberti, and R. P. Martins, “Nano-ampere low dropout regulator designs for IoT devices,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 11, pp. 4017–4026, Nov. 2018.

[14] N. Adorni, S. Stanzione, and A. Boni, “A 10-mA LDO with 16-nA IQ and operating from 800-mV supply,” IEEE J. Solid-State Circuits, vol. 55, no. 2, pp. 404–413, Feb. 2020.

[15] J. Li et al., “An adaptively biased LDO regulator with 11nA quiescent current and 50mA available load,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2021.

[16] X. Ming et al., "A Capacitor-less LDO With Fast-transient Error Amplifier and Push-pull Differentiator," IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018.

[17] N. Liu and D. Chen, "A Transient-Enhanced Output-Capacitorless LDO With Fast Local Loop and Overshoot Detection," IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 67, no. 10, pp. 3945-3956, Oct. 2020.

[18] X. Ming et al., "A Fast-Transient Capacitorless LDO With Dual Paths Active-Frequency Compensation Scheme," in IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 10332-10347, Sept. 2022.

[19] X. Cheng et al., "A Fast Transient Response Capless LDO Regulator Achieving -78 dB of PSR Up to 2 MHz," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, 2024.

[20] X. Ma, Y. Lu, and Q. Li, "A Fully Integrated LDO With 50-mV Dropout for Power Efficiency Optimization," IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 67, no. 4, pp. 725-729, Apr. 2020.