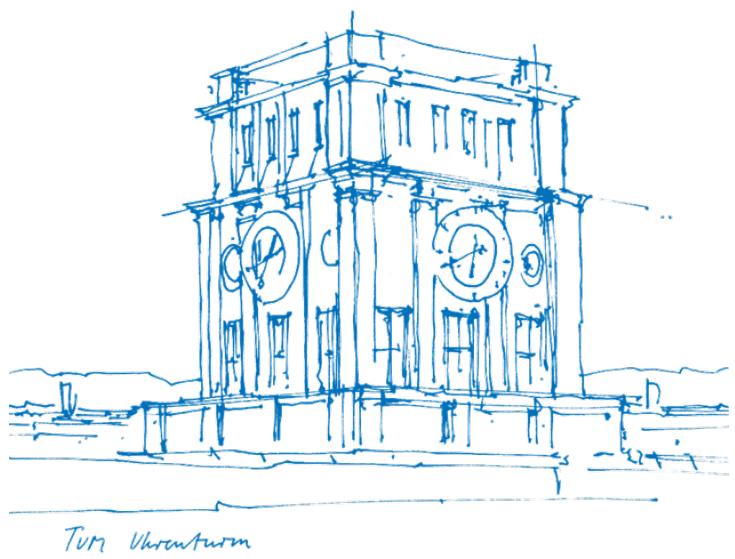


# A Capacitor-less Low-Dropout Voltage Regulator Design

Weiqing Lou





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Weiqing Lou

Thesis for the attainment of the academic degree

**Master of Science (M.Sc.)**

at the TUM School of Computation, Information and Technology of the Technical University of Munich.

**Examiner:**

Prof. Dr. -Ing. Ralf Brederlow

**Supervisor:**

Dr. Pengcheng Xu

**Submitted:**

Munich, 01.06.2025



I hereby declare that this thesis is entirely the result of my own work except where otherwise indicated. I have only used the resources given in the list of references.



# Abstract

The relentless advancement of integrated circuit technology has heightened the importance of efficient power management solutions, with Low Dropout Regulators (LDOs) emerging as a cornerstone in modern circuit design. Renowned for their straightforward architecture, LDOs deliver stable output voltage, minimal noise, low ripple, and cost-effectiveness, making them indispensable in applications spanning digital circuits, medical electronics, analog systems, and radio frequency (RF) chips. By providing reliable voltage regulation to internal modules, LDOs facilitate seamless integration into System-on-Chip (SoC) designs, supporting the growing complexity of compact, high-performance electronics.

As the industry prioritizes smaller, more efficient chip designs, traditional capacitor-based LDOs face challenges due to their suboptimal area efficiency, as external compensation capacitors consume valuable chip real estate. Capacitor-less LDOs address this limitation by eliminating the need for external capacitors, significantly reducing chip area and overall system costs while maintaining performance. This paper investigates the fundamental operating principles of capacitor-less LDOs and presents the design of eight distinct LDO variants implemented in a 22 nm process node. Through comprehensive experimental analysis, the study compares the performance of these LDOs, evaluating variations in capacitor types, pass devices, and feedback resistors. Additionally, it contrasts voltage-mode and current-mode LDO architectures to elucidate their respective advantages and trade-offs. The findings offer valuable insights into optimizing capacitor-less LDO designs for next-generation integrated circuits, balancing performance, area efficiency, and cost in compact SoC applications.



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# 1 Introduction

## 1.1 Research Background

Power management integrated circuits (PMICs) are fundamental to modern electronic systems, providing efficient power conversion, regulation, and distribution to ensure reliable and optimized device performance. These chips deliver precise voltage and current levels to diverse integrated components, incorporating essential functions such as voltage regulation, power sequencing, battery management, and thermal control within compact, highly integrated packages [1]. This integration streamlines circuit design reduces system costs and enhances reliability, making PMICs indispensable across a wide range of applications.

The rapid evolution of consumer electronics, automotive systems, industrial automation, and Internet of Things (IoT) technologies has driven unprecedented demand for advanced power management solutions. According to market forecasts, the global PMIC market is projected to grow at a compound annual growth rate (CAGR) of approximately 6.8% through the next decade, reflecting the increasing reliance on efficient power management in diverse sectors [2]. In consumer electronics, devices such as smartphones, tablets, and wearables require sophisticated PMICs to maximize battery life, enhance performance, and support compact form factors. In automotive applications, robust power management is critical for the safe and reliable operation of advanced driver-assistance systems (ADAS), electric vehicle (EV) powertrains, and infotainment platforms. Industrial automation relies on PMICs to ensure consistent performance of control systems, sensors, and actuators in harsh environments. Similarly, IoT devices and wireless sensor networks demand ultra-low-power designs to extend operational lifespans, particularly for battery-powered or energy-harvesting systems.

The relentless push toward miniaturization, coupled with the growing complexity of electronic systems, underscores the need for continuous innovation in power management technologies. Modern systems require PMICs that balance high efficiency, compact size, and robust performance while addressing challenges such as thermal dissipation and electromagnetic interference. Power supplies typically operate in direct current (DC) or alternating current (AC) configurations, with this paper focusing on DC-based designs due to their prevalence in integrated circuits. Key DC power management solutions include LDO linear regulators, charge pump voltage converters, and inductor-based switching DC-DC converters. LDOs are valued for their simplicity, low noise, and stable output, making them ideal for applications requiring precise voltage regulation. This paper explores these technologies in detail, with a focus on the design and optimization of LDOs, particularly capacitor-less variants, to meet the demands of next-generation integrated circuits.

### 1.1.1 Linear Regulator

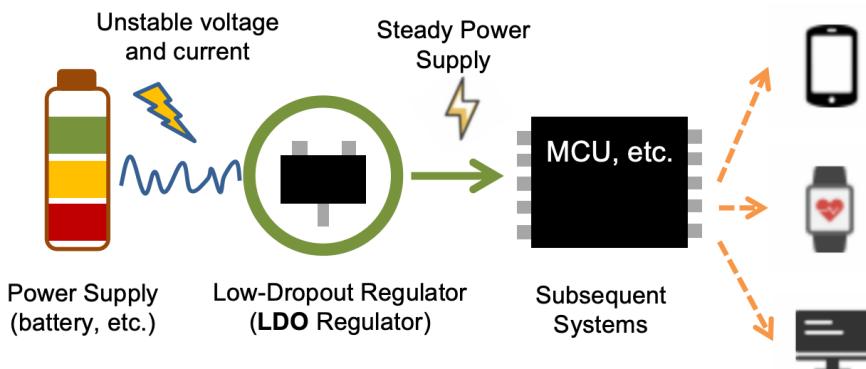
Linear regulators are essential components in power management systems, designed to provide a stable output voltage despite fluctuations in input voltage or load current. Operating in the linear region of a pass transistor, these regulators dissipate excess power as heat to maintain precise voltage regulation. Their simplicity, low output noise, and fast transient response make them ideal for noise-sensitive applications, such as analog circuits, RF systems, and precision instrumentation, where clean and stable power is critical [1].

The evolution of LDO linear regulators has been driven by the demand for efficient, compact, and low-noise power management in modern electronics. Introduced by Robert C. Dobkin in the 1970s, early linear regulators required significant input-output voltage differentials, which limited their efficiency in low-voltage applications [3]. The advent of LDOs addressed this constraint by enabling operation with minimal voltage

headroom, typically below 1 V, making them well-suited for battery-powered devices, such as smartphones, wearables, and IoT nodes, where power efficiency and compactness are paramount [4].

In the 1980s, advancements in CMOS technology enabled the integration of LDOs into monolithic circuits, reducing size, cost, and external component requirements while improving performance metrics like power supply rejection ratio (PSRR) and quiescent current. These developments made LDOs a cornerstone of analog and mixed-signal circuits [4]. The 1990s saw further innovations spurred by the rise of portable electronics, including mobile phones and laptops, with designs focusing on enhanced PSRR, lower quiescent current, and improved transient response to extend battery life and support dynamic loads.

The 2000s introduced significant refinements, with research emphasizing adaptive biasing, dynamic compensation, and integration with power management integrated circuits (PMICs) to enhance efficiency and stability under varying load conditions [5]. Modern LDOs, leveraging advanced process nodes (e.g., 22 nm and below), achieve ultra-low dropout voltages, high current densities, and robust performance, catering to diverse applications, including automotive advanced driver-assistance systems (ADAS), medical devices, and ultra-low-power IoT sensors. Recent advancements have explored digitally controlled LDOs, hybrid analog-digital architectures, and capacitor-less designs to address area efficiency and scalability challenges in System-on-Chip (SoC) integration.



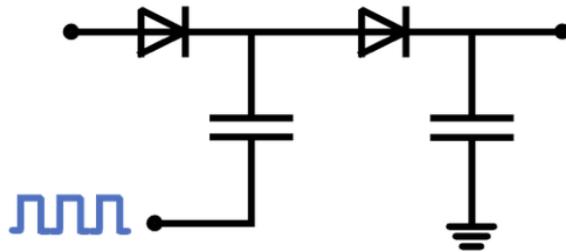
**Figure 1.1** Usage of a Low Dropout Regulator

As shown in Figure 1.1, linear regulators continue to play a vital role in battery-powered devices, audio systems, and high-precision applications, where their low noise and rapid transient response outweigh efficiency trade-offs. Ongoing research focuses on enhancing LDO performance through techniques such as adaptive voltage scaling, integrated compensation, and capacitor-less architectures to meet the stringent demands of next-generation electronics, including 5G infrastructure, edge computing, and energy-harvesting systems [5]. These advancements position LDOs as a key enabler of efficient and reliable power management in increasingly compact and power-constrained designs.

### 1.1.2 Charge Pump

Charge pumps are specialized power management circuits that generate output voltages higher or lower than the input voltage without the use of inductors, offering a compact and cost-effective solution for integrated circuit applications. By transferring charge between capacitors through controlled switching, charge pumps enable voltage doubling, inversion, or stepping, making them ideal for low-power systems where space and simplicity are critical [6]. Their inductor-less design minimizes electromagnetic interference (EMI), reduces external component count, and facilitates seamless integration into space-constrained devices, such as mobile phones, smart cards, and wearable electronics.

As shown in Figure 1.2, the operation of a charge pump relies on a two-phase switching mechanism driven by a clock signal. During the first phase, a flying capacitor is charged from the input voltage source. In the second phase, the charged capacitor is reconfigured to transfer its charge to an output capacitor, effectively modifying the output voltage relative to the input [7]. Common configurations include the Dickson



**Figure 1.2** Schematic Design of a Charge Pump

charge pump, which excels in voltage step-up applications, and cross-coupled designs, which improve efficiency in low-voltage scenarios by reducing transistor switching losses [8]. Despite their advantages, charge pumps are limited by low output current capability, efficiency losses from parasitic capacitances, and switching inefficiencies, which can constrain their use in high-power applications.

Charge pumps have been pivotal in applications requiring compact voltage conversion, such as EEPROM and flash memory programming, LCD and OLED display drivers, and low-current analog and RF circuits [7]. Since their introduction by John F. Dickson in the 1970s, charge pumps have evolved significantly. Early designs focused on basic voltage multiplication for memory circuits, but advancements in CMOS technology during the 1980s and 1990s enabled higher efficiency and integration into monolithic power management integrated circuits (PMICs) [6]. The 2000s saw further refinements, including the development of adaptive switching techniques and low-voltage architectures to support portable electronics and battery-powered devices.

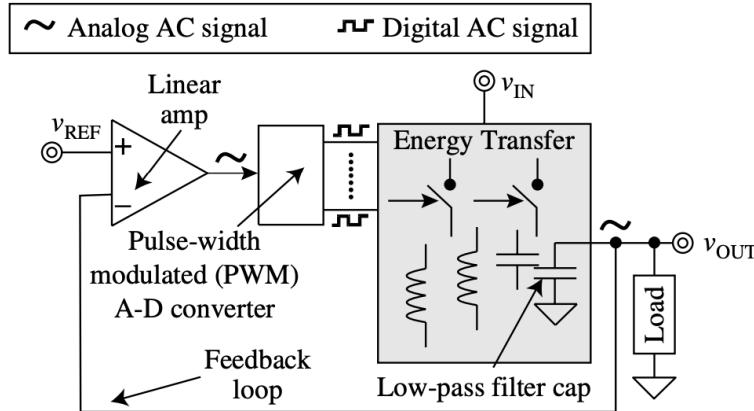
Modern charge pumps, benefiting from advanced process nodes (e.g., 22 nm and below), achieve improved power efficiency and support applications in IoT devices, medical implants, and energy-harvesting systems. Recent research has focused on enhancing performance through innovations such as adaptive switching frequencies, which optimize efficiency across varying loads, and hybrid architectures that combine charge pumps with linear regulators or switching converters to balance efficiency and noise performance [9]. Additionally, efforts to mitigate parasitic losses and improve output current capacity have led to the exploration of multi-phase charge pumps and integrated control loops for dynamic performance optimization.

The core strengths of charge pumps lie in their simplicity, small footprint, and EMI-friendly design, making them a preferred choice for low-power, area-constrained applications. However, their efficiency and output current limitations necessitate careful design considerations, particularly when compared to inductor-based switching converters. As the demand for compact and efficient power management grows in 5G infrastructure, edge computing, and ultra-low-power IoT systems, charge pumps continue to evolve, with ongoing research exploring digitally controlled designs and integration with SoC platforms to meet the needs of next-generation electronics.

### 1.1.3 DC-DC Converter

DC-DC converters are critical power management circuits that transform a DC input voltage to a different DC output voltage, enabling efficient and flexible power delivery in electronic systems. Unlike linear regulators, which dissipate excess power as heat, DC-DC converters employ high-frequency switching techniques to minimize power losses, achieving efficiencies often exceeding 90% [10]. By utilizing energy storage elements such as inductors and capacitors, these converters provide compact, high-performance solutions for applications ranging from portable electronics and automotive systems to renewable energy systems and data centers.

The operation of an inductive switching DC-DC converter relies on an inductor as the primary energy storage element, leveraging its property of resisting sudden voltage changes to store and release energy. Controlled by high-frequency switching, typically through pulse-width modulation (PWM) or pulse-



**Figure 1.3** Schematic of a Switching DC-DC Converter [1]

frequency modulation (PFM), the converter samples the output voltage and generates a feedback control signal to adjust the duty cycle of switching elements (e.g., MOSFETs). This feedback mechanism ensures a stable output voltage despite variations in input voltage or load conditions [11]. DC-DC converters are classified into several topologies, including buck (step-down), boost (step-up), and buck-boost (step-up/down), each tailored to specific voltage conversion requirements [12]. The combination of inductors, filter capacitors, and switching elements enables precise voltage regulation and efficient power transfer.

Since their widespread adoption in the 1980s, driven by advancements in power electronics and CMOS technology, DC-DC converters have become indispensable in modern systems. Their high efficiency under large loads and wide voltage differentials makes them superior to linear regulators for applications requiring significant power conversion, such as automotive electronics (e.g., electric vehicle powertrains), communication infrastructure (e.g., 5G base stations), computer power supplies, and LED drivers [13]. For example, buck converters are commonly used in battery-powered devices to step down voltages for microprocessors, while boost converters are critical in renewable energy systems to elevate voltages from solar panels or batteries [10].

Despite their efficiency advantages, DC-DC converters introduce challenges due to high-frequency switching, including output voltage ripple and electromagnetic interference (EMI). These issues necessitate additional design considerations, such as low-pass filters, shielding, and careful layout to minimize noise and ensure clean output [14]. Furthermore, switching losses and inductor size can impact performance in ultra-compact or high-frequency applications, prompting innovations to address these trade-offs. DC-DC converters strike a balance between efficiency, size, and cost, making them a cornerstone of power management in battery-powered electronics, automotive systems, renewable energy applications, and high-performance computing.

#### 1.1.4 Comparison

Linear regulators, charge pumps, and DC-DC converters are key power supply technologies, each offering distinct advantages and trade-offs in power management applications. Understanding these trade-offs is essential for effective power supply chip selection.

The choice between linear regulators, charge pumps, and DC-DC converters depends on application requirements. Linear regulators prioritize simplicity and low noise but sacrifice efficiency. Charge pumps offer a compact, inductor-less solution for specific voltage conversions with moderate efficiency. DC-DC converters provide superior efficiency and flexibility for a wide range of voltages and currents but introduce complexity and noise. A typical comparison of the main functions, features, advantages and disadvantages of the three types is summarized in Table 1.1.

Parameters	LDO Regulator	Switching DC-DC Converter	Charge Pump DC-DC Converter
<b>Function</b>	Buck	Buck, Boost, Buck-Boost	Boost, Buck, or Invert
<b>Efficiency</b>	Medium	High (typically >90%)	Medium
<b>Ripple</b>	Low	High (filtering required)	Medium
<b>Noise</b>	Low	High	High
<b>Complexity</b>	Simple; Few components	Complex; Needs inductors, capacitors	Complex; Capacitor based
<b>Peripheral Device</b>	Few	Inductors, Capacitors, etc.	Capacitors
<b>Size</b>	Small	Large	Large
<b>Cost</b>	Low	High	Medium
<b>Applications</b>	Battery-powered devices, RF/analog circuits	Automotive, consumer electronics, CPU power rails	LCD drivers, memory biasing, low-power systems

Table 1.1 Comparison of DC Conversion Regulators

## 1.2 Problem Statement

Traditional LDO designs rely on large external capacitors to ensure stability, suppress transient voltage fluctuations, and maintain low noise under varying load conditions. However, these capacitors increase system size, elevate bill-of-materials (BoM) costs, and complicate integration, posing significant challenges as electronic devices trend toward miniaturization and higher levels of SoC integration [1]. The need for fully integrated power management solutions has driven research into capacitor-less LDO regulators, which eliminate the need for external capacitors, thereby reducing footprint, simplifying design, and lowering costs while maintaining performance comparable to traditional LDOs.

This paper defines the problem of designing a capacitor-less LDO that addresses these challenges while meeting the demands of next-generation integrated systems. The development of capacitor-less LDOs addresses growing demands for cost-effective and reliable power management in consumer electronics, automotive systems, and IoT applications, where minimal external components and high reliability are critical [7]. However, designing capacitor-less LDOs introduces significant challenges, particularly in achieving stability and low noise without external capacitors. The absence of these capacitors increases the risk of instability, especially at high load currents or under dynamic operating conditions, and exacerbates sensitivity to process, voltage, and temperature (PVT) variations, particularly in advanced process nodes like 22 nm FDX-Plus. These challenges necessitate innovative design strategies to ensure robust performance across diverse operating conditions.

Another critical issue is ensuring reliable operation in advanced CMOS technologies, where scaling to 22 nm nodes introduces stringent requirements for voltage regulation, current handling, and silicon area efficiency. For instance, designing an LDO capable of stepping down a 1.5 V input to a 0.8 V output while supporting a wide load current range (e.g., 10  $\mu$ A to 100 mA) is essential for powering modern integrated circuits, such as low-power microcontrollers, RF transceivers, and analog front-ends. The lack of an ex-

ternal capacitor complicates transient response and noise suppression, requiring advanced compensation techniques, adaptive biasing, and optimized feedback mechanisms to achieve stability and efficiency.

### 1.3 Motivation

In the context of advanced CMOS technologies, such as the 22 nm FDX-Plus process node, the design of capacitor-less LDOs presents both opportunities and challenges. This paper aims to develop an LDO capable of converting a 1.5 V input voltage to a 0.8 V output while supporting a wide load current range from 10  $\mu$ A to 100 mA, meeting the stringent requirements of low-power microcontrollers, analog front-ends, and RF transceivers in modern SoCs. The project systematically compares eight distinct LDO architectures, exploring trade-offs between NMOS and PMOS pass elements, capacitor-based and capacitor-less designs, and voltage-mode and current-mode control schemes. These comparisons provide critical insights into optimizing stability, transient response, and integration potential for diverse application demands, from ultra-low-power IoT sensors to high-performance automotive electronics.

The primary motivation for this work is to achieve high reliability and stability across a broad operating range while minimizing reliance on external components. Capacitor-less LDOs must overcome significant challenges, including susceptibility to oscillations and degraded transient performance in the absence of external capacitors, particularly under dynamic load conditions or process, voltage, and temperature variations inherent in 22 nm nodes. To address these issues, the proposed designs incorporate internal compensation techniques, such as adaptive biasing, Miller compensation, and pole-zero cancellation, to ensure robust stability and fast transient response. Furthermore, these LDOs are optimized for high PSRR and low quiescent currents to improve overall efficiency.

The significance of this research lies in its potential to advance fully integrated power management solutions for next-generation electronics. By developing and analyzing eight capacitor-less LDO configurations, this study aims to identify optimal architectural choices that balance performance, reliability, and area efficiency in advanced semiconductor processes. The findings will contribute to the design of power-efficient, compact SoCs for emerging applications, including 5G infrastructure, edge computing, medical implants, and energy-harvesting systems. Ultimately, this work seeks to pave the way for scalable, cost-effective power management solutions that meet the evolving demands of high-performance, miniaturized electronic systems.

### 1.4 Structure of this Thesis

This thesis is organized into six chapters.

Chapter 1 introduces the background and motivation for this work. It reviews different voltage regulation methods, including linear regulators, charge pumps, and DC-DC converters, and provides a comparative analysis. The problem statement and motivation for developing high-performance LDOs are also outlined.

Chapter 2 discusses the basic principles and structural characteristics of LDOs. It introduces the general architecture, classifications of pass devices and capacitors, and evaluates key performance metrics such as dropout voltage, quiescent current, regulation capability, PSRR, and efficiency. It also analyzes the location and impact of poles and zeros in the system.

Chapter 3 presents the circuit-level analysis and compensation strategies. Loop gain behavior and frequency response are discussed in detail, followed by various compensation techniques including resistor-based, feed-forward, Miller, and buffer-assisted methods.

Chapter 4 describes the implementation of key sub-circuits. It includes the design of pass devices, operational transconductance amplifiers (OTAs), and bandgap reference circuits. A source-follower-based pre-filter is also introduced to enhance PSRR performance.

Chapter 5 details the experimental designs and simulation results. Several LDO architectures are implemented, including capacitor-based, capacitor-less, and current-mode configurations. Their performance

is compared in terms of dropout voltage, loop stability, PSRR, load and line regulation, and transient response.

Chapter 6 concludes the thesis with a summary and insights into possible future research directions.



## 2 Basic Principle and Structure Analysis

Low Dropout (LDO) regulators are critical for delivering stable, low-noise power supplies in modern electronic systems, particularly in applications requiring precise voltage regulation with minimal input-output voltage differential. The core principle of an LDO lies in its ability to maintain a constant output voltage by dynamically adjusting the resistance of a pass device, compensating for fluctuations in input voltage or load current. The architecture and compensation strategy of an LDO vary significantly depending on the target application, with key distinctions between capacitor-based and capacitor-less designs, as well as between different pass element types (e.g., PMOS vs. NMOS). Understanding these architectural variations is essential for evaluating trade-offs in stability, dropout voltage, transient response, noise performance, and integration feasibility in advanced process nodes like 22 nm FDX-Plus.

### 2.1 LDO Architecture Overview

The fundamental structure of an LDO regulator, as illustrated in Figure 2.1, comprises four key components: a startup circuit, a reference voltage generator, an error amplifier (EA), and a pass device, working in tandem to regulate the output voltage  $V_{OUT}$  despite variations in input voltage  $V_{IN}$  and load conditions. The startup circuit ensures proper initialization of the LDO, particularly in low-power or battery-powered systems, by providing initial biasing to prevent latch-up or instability during power-up. The reference voltage generator produces a stable, temperature-independent reference voltage  $V_{REF}$ , typically derived from a bandgap reference, which serves as the target for output regulation [1].

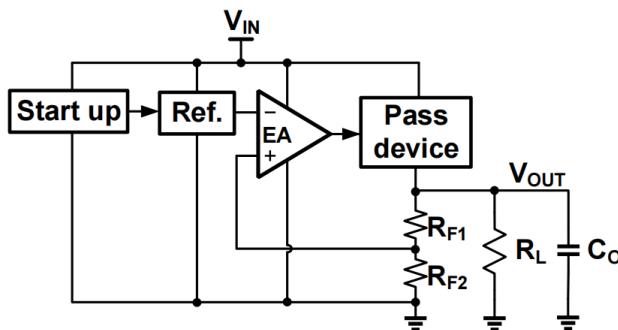


Figure 2.1 LDO Block Diagram

The error amplifier compares  $V_{REF}$  to a fraction of  $V_{OUT}$ , obtained through a resistive feedback network formed by resistors  $R_{F1}$  and  $R_{F2}$ . The feedback voltage is given by:

$$V_{FB} = V_{OUT} \cdot \frac{R_{F2}}{R_{F1} + R_{F2}} \quad (2.1)$$

The error amplifier amplifies the difference between  $V_{REF}$  and  $V_{FB}$ , generating a control signal that adjusts the gate voltage of the pass device, typically a PMOS or NMOS transistor, to regulate  $V_{OUT}$ . The choice of pass device significantly impacts performance: PMOS transistors offer lower dropout voltages and simpler gate drive requirements but may require larger silicon area, while NMOS transistors provide faster transient response and better load regulation but necessitate a charge pump or higher gate drive voltage [4].

The output node is loaded by a load resistor  $R_L$  and, in traditional designs, an output capacitor  $C_O$ , which stabilizes the feedback loop, reduces output noise, and improves transient response. The capacitor  $C_O$ ,

often accompanied by its equivalent series resistance (ESR), introduces a dominant pole and a zero in the loop transfer function, aiding stability but increasing system size and cost. Capacitor-less LDOs, however, eliminate large external capacitors to enhance integration into SoC designs, relying instead on internal compensation techniques, such as Miller compensation, adaptive biasing, or pole-zero cancellation, to maintain stability [15]. This shift introduces significant design challenges, including increased sensitivity to process, voltage, and temperature variations and degraded transient performance under dynamic loads.

## 2.2 LDO Types

LDO regulators are categorized based on the type of pass device and the presence or absence of an output capacitor, each influencing critical performance metrics such as dropout voltage, transient response, stability, and integration feasibility. The choice of pass device, PMOS or NMOS, affects the LDO's efficiency, control complexity, and suitability for specific applications, while the decision to use a capacitor-based or capacitor-less design impacts area efficiency and loop dynamics. This section explores these distinctions, focusing on their implications for advanced LDO designs in a 22 nm FDX-Plus process node, particularly for applications requiring low noise, high PSRR, and compact SoC integration.

### 2.2.1 Pass Device Configurations

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The pass device in an LDO serves as a variable resistor between the input supply  $V_{IN}$  and the output  $V_{OUT}$ , playing a pivotal role in regulating the output voltage by adjusting its resistance in response to the error amplifier's control signal. As shown in Figure 2.2, the choice of pass device, either a PMOS or NMOS transistor, significantly impacts the LDO's dropout voltage, transient response, loop stability, and overall design complexity, making it a critical consideration for advanced applications [4].

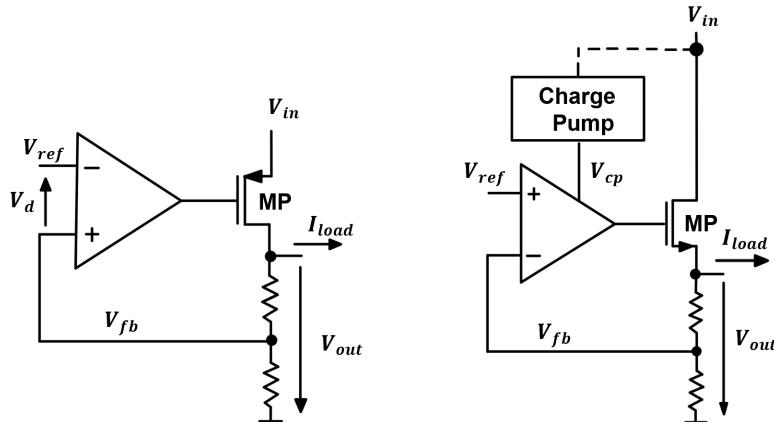


Figure 2.2 Fundamental LDO with PMOS (left) and NMOS (right) power transistor [16]

The left diagram in Figure 2.2 illustrates a PMOS-based LDO. The error amplifier (EA) drives the gate with a negative voltage relative to  $V_{IN}$ , enabling straightforward control since the gate voltage can be ground-referenced. PMOS pass devices are easy to drive at the gate, with the turn-on condition being  $V_G < V_S - |V_{th}| = V_{in} - |V_{th}|$ , making them well-suited for low-voltage applications. However, their higher  $R_{DS(on)}$  compared to NMOS transistors results in a larger dropout voltage, which can reduce efficiency, particularly at high load currents (e.g., up to 100 mA). Additionally, PMOS devices often require larger silicon area, posing challenges for area-constrained SoC designs [1].

The right diagram in Figure 2.2 depicts an NMOS-based LDO. NMOS pass devices benefit from lower  $R_{DS(on)}$ , enabling smaller dropout voltages and improved efficiency, which is advantageous for applications requiring tight voltage regulation (e.g., 1.5 V to 0.8 V conversion). However, driving the NMOS gate requires a voltage higher than  $V_{IN}$ , typically achieved using a charge pump or bootstrapping circuit, which increases design complexity, power consumption, and potential noise injection. The NMOS configuration

 offers superior transient response and load regulation due to its higher drive strength, making it suitable for dynamic load conditions in RF transceivers and analog circuits [15].

The trade-offs between PMOS and NMOS pass devices are particularly pronounced in capacitor-less LDO designs, where stability and transient performance are critical without the stabilizing effect of an external capacitor. PMOS-based LDOs simplify loop compensation but may struggle with stability at high load currents due to their higher output impedance. Conversely, NMOS-based LDOs require sophisticated compensation techniques, such as adaptive biasing or pole-zero cancellation, to mitigate instability while leveraging their efficiency advantages. These considerations are crucial for low-voltage, high-current applications in advanced 22 nm nodes, where process, voltage, and temperature variations further complicate design.

## 2.2.2 Capacitor Configurations

LDO regulators are classified based on their output capacitance configuration, which significantly influences stability, transient response, and integration feasibility. As depicted in Figure 2.3, LDOs can be categorized into capacitor-based designs, which rely on an external output capacitor, and capacitor-less designs, which eliminate external capacitors to enhance integration.

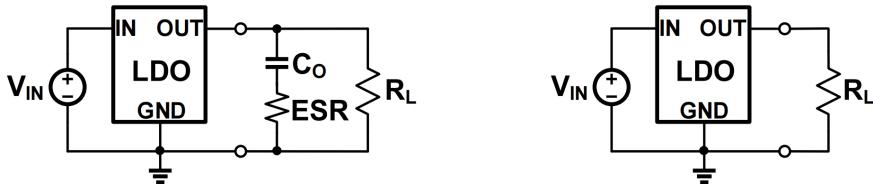


Figure 2.3 Capacitor LDO (left) or Capacitor-less LDO (right)

 In capacitor-based LDOs, an external output capacitor  $C_O$ , typically ranging from 1 to 10  $\mu\text{F}$ , is employed to stabilize the feedback loop and enhance transient response. The capacitor introduces a dominant pole in the loop transfer function, reducing the phase margin requirements for stability. Additionally, the equivalent series resistance (ESR) of  $C_O$  creates a zero that can compensate for the low-frequency pole at the output node, improving phase margin. 

通过内部补偿技术和小型寄生电阻来保持电路稳定性

Capacitor-less LDOs eliminate the external  $C_O$ , relying on internal compensation techniques and small parasitic capacitances to maintain stability. This approach significantly reduces silicon area and BoM costs, enabling full integration into advanced process nodes like 22 nm FDX-Plus, where area efficiency is paramount. However, the absence of  $C_O$  shifts the dominant pole to higher frequencies, reducing phase margin and increasing susceptibility to oscillations, particularly under dynamic load conditions (e.g., 10  $\mu\text{A}$  to 100 mA). To address these challenges, capacitor-less LDOs employ sophisticated compensation methods, such as Miller compensation, nested Miller compensation, adaptive biasing, or pole-zero cancellation, to stabilize the loop and improve transient performance [4]. These techniques, however, increase design complexity and may elevate quiescent current, posing trade-offs in power efficiency.

The choice between capacitor-based and capacitor-less LDOs depends on the target application's requirements. Capacitor-based designs are preferred in applications prioritizing robust stability and low noise, such as precision analog circuits and RF transceivers, where the external capacitor's filtering mitigates output ripple. Conversely, capacitor-less LDOs are advantageous in area-constrained, low-power applications, such as IoT sensors, medical implants, and edge computing devices, where integration and cost are critical.

## 2.3 Performance Evaluation of LDOs

The performance of an LDO is evaluated through a variety of metrics that determine its efficiency, stability, and reliability, directly impacting the functionality of the circuits they power. Key performance metrics

include static and dynamic regulation, dropout voltage, quiescent current, transient response, load current capability, temperature coefficient, and power supply rejection ratio. Static regulation encompasses line and load regulation under steady-state conditions, while dynamic regulation assesses the LDO's ability to respond to rapid changes in input voltage or load current. Other critical considerations include minimizing dropout voltage to enhance efficiency, reducing quiescent current for low-power operation, and ensuring stability across a wide range of loads and process, voltage, and temperature variations. This section analyzes these metrics in detail, emphasizing their definitions, physical significance, and trade-offs in practical LDO design.

### 2.3.1 Dropout Voltage

Dropout voltage is a key parameter for LDO regulators. It is defined as the minimal difference between the input and output voltage of an LDO at a normal working state [17]. It directly affects the efficiency and power consumption of the LDO. A lower dropout voltage is better for efficiency. Mathematically, the dropout voltage ( $V_{dropout}$ ) is expressed as:

$$V_{dropout} = V_{IN} - V_{OUT}, V_{dropout} = R_{on} \cdot I_{load} \quad (2.2)$$

where  $R_{on}$  is the equivalent conduction resistance of the pass transistor and  $I_{load}$  is the load current. A typical diagram in Figure 2.4 shows the relationship between  $V_{in}$  and  $V_{out}$ , highlighting the LDO's operating regions: the cutoff region, the dropout region, and the regulation region.  $V_{min}$  represents the lowest value of  $V_{in}$  for the regulation to work properly. The dropout voltage depends on the pass device or load current. The regulation fails when  $V_{in}$  falls below a certain threshold relative to  $V_{out}$ . The pass device's on-resistance  $R_{on}$  and the load current determine the voltage drop across it. For most LDOs, the dropout voltage typically ranges from 0.1 V to 0.5 V.

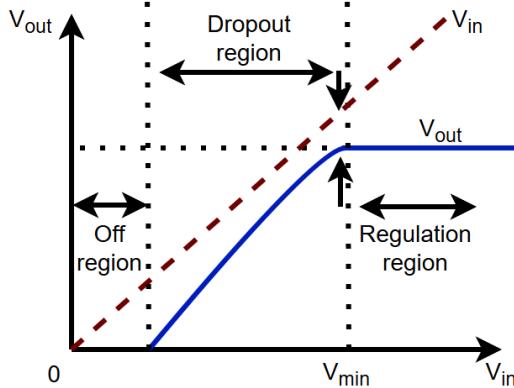


Figure 2.4 Dropout Voltage

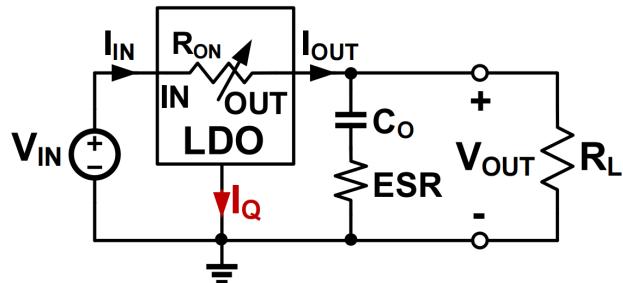
A low dropout voltage allows the LDO to operate efficiently with minimal input headroom, making it especially desirable for battery-powered or low-voltage systems. The dropout voltage is largely determined by the type and size of the pass transistor. Minimizing the dropout voltage is essential not only for efficiency but also to extend battery life and improve the overall power budget in low-power systems. Therefore, careful selection and sizing of the pass transistor is key to optimizing LDO performance in terms of dropout.

### 2.3.2 Quiescent Current LDO内部电路在维持输出稳压过程中所消耗的电流；并不会流向负载

Quiescent current ( $I_Q$ ) represents the current consumed by the LDO's internal circuitry to maintain regulation, excluding the load current ( $I_{OUT}$ ). As illustrated in Figure 2.5,  $I_Q$  flows through internal components such as the reference voltage generator, error amplifier, feedback resistors, and support circuits, and **does not contribute to the output load**. Mathematically, with total input current  $I_{IN}$  minus output current  $I_{OUT}$ , it is defined as:

$$I_Q = I_{IN} - I_{OUT}, \quad (2.3)$$

The quiescent current is primarily due to bias currents in the reference generator, error amplifier, feedback resistors, and support circuits. A key characteristic of  $I_Q$  in a well-designed LDO is that it is almost independent of the load current  $I_{OUT}$ , ensuring minimal power consumption overhead across varying load conditions. This independence is crucial for maintaining high efficiency, especially at low load currents, where  $I_Q$  can significantly impact the overall efficiency of the LDO.



**Figure 2.5 Quiescent Current**

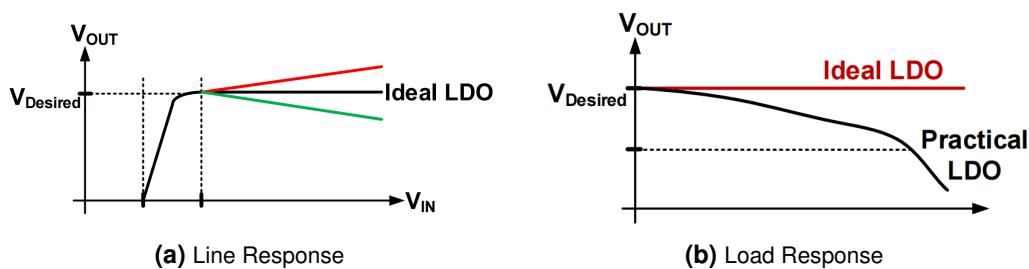
Minimizing quiescent current is essential in battery-powered or energy-constrained applications, such as wearable devices, IoT nodes, and always-on domains. A lower  $I_Q$  directly translates to higher system efficiency during standby or light-load conditions. In high-performance LDOs,  $I_Q$  can range from several microamperes down to the nanoampere level, depending on the circuit complexity and biasing strategy. However, reducing  $I_Q$  often comes at the cost of slower transient response and limited loop bandwidth, creating a trade-off between power consumption and dynamic performance. Careful design of the error amplifier, reference circuit, and biasing network is required to optimize  $I_Q$  while maintaining stability and regulation accuracy.

### 2.3.3 Regulation Capability

The regulation capability of a LDO regulator refers to its ability to maintain a stable output voltage  $V_{OUT}$  despite variations in input voltage  $V_{IN}$  or load current  $I_{LOAD}$ . Good regulation is achieved through effective feedback design and loop compensation, enabling the error amplifier to respond accurately to disturbances. For capacitor-less LDOs, maintaining tight regulation is particularly challenging due to the absence of external output capacitance, which exacerbates voltage droops and transient instability.

#### Static Regulation Metrics

Static regulation quantifies an LDO's ability to maintain a stable  $V_{OUT}$  under steady-state variations in  $V_{IN}$  or  $I_{LOAD}$ . Ideal LDOs would exhibit no deviation in  $V_{OUT}$ , but practical designs show some variation due to finite loop gain, pass device resistance, and circuit non-idealities. As illustrated in Figure 2.6, static regulation encompasses two primary components: line regulation and load regulation, which are critical for applications with fluctuating supply voltages or load demands [4].



**Figure 2.6 Static Regulation Metrics**

**Line Regulation** measures the change in  $V_{OUT}$  in response to a change in  $V_{IN}$ , reflecting the LDO's ability to reject input voltage variations. It is defined as:

$$LineRegulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad (2.4)$$

where  $\Delta V_{OUT}$  is the output voltage variation, and  $\Delta V_{IN}$  is the input voltage change. As shown in Figure 2.6(a), an ideal LDO maintains a constant  $V_{OUT}$  (flat line), while practical LDOs exhibit slight deviations due to limited loop gain and feedback accuracy. Lower line regulation values indicate better performance, typically achieved through high open-loop gain and robust PSRR. For example, in a 22 nm FDX-Plus process, line regulation values below 0.1 mV/V are desirable for noise-sensitive applications like RF transceivers [15].

**Load Regulation** quantifies the LDO's ability to maintain  $V_{OUT}$  as  $I_{LOAD}$  varies, defined as

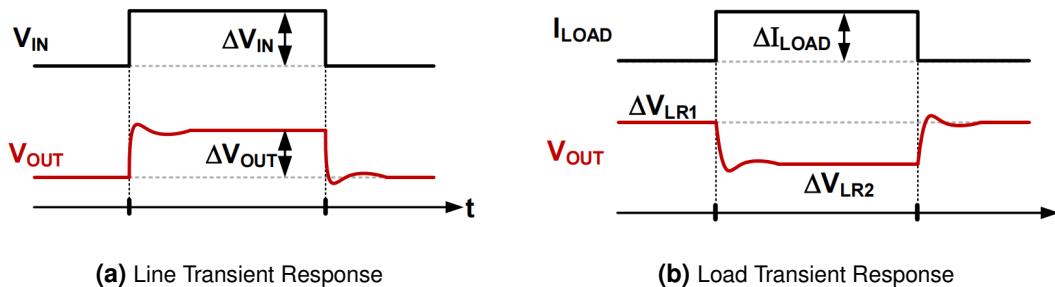
$$LoadRegulation = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \quad (2.5)$$

where  $\Delta I_{LOAD}$  is the change in load current. Figure 2.6(b) compares an ideal LDO (constant  $V_{OUT}$ ) with a practical LDO, where  $V_{OUT}$  typically drops under increasing  $I_{LOAD}$  due to the pass device's on-resistance and finite loop gain. Lower load regulation values, ideally below 0.1 mV/mA, are critical for applications with dynamic loads, such as microcontrollers or IoT sensors. In capacitor-less LDOs, achieving tight load regulation is challenging due to limited charge storage, necessitating high-gain error amplifiers and optimized feedback networks.

Both line and load regulation are essential for ensuring stable voltage delivery to sensitive circuits under steady-state conditions. Minimizing these metrics requires high loop gain, low output impedance, and effective compensation, particularly in capacitor-less designs.

### Dynamic Regulation Metrics

Dynamic regulation assesses an LDO's ability to maintain  $V_{OUT}$  stability during rapid changes in  $V_{IN}$  or  $I_{LOAD}$ , a critical requirement for modern digital and RF systems with fast-switching loads. Unlike static regulation, dynamic metrics focus on transient behavior, including voltage deviations, settling time, and stability under abrupt disturbances. As shown in Figure 2.7, dynamic regulation is evaluated through two key scenarios: line transient response and load transient response, which are particularly challenging for capacitor-less LDOs due to limited on-chip capacitance [4].



**Figure 2.7** Dynamic Regulation Metrics

**Line Transient Response** evaluates the change in  $V_{OUT}$  caused by a step change in  $V_{IN}$ , as depicted in Figure 2.7(a). Key parameters include the peak voltage deviation, settling time, and any overshoot or undershoot, which reflect the LDO's ability to reject input transients and maintain stability. A fast and well-compensated feedback loop minimizes  $\Delta V_{OUT}$  and reduces settling time, typically targeting deviations below 50 mV and settling times under 1  $\mu$ s for high-performance applications. In capacitor-less LDOs, limited charge buffering increases  $\Delta V_{OUT}$ , necessitating advanced compensation techniques like adaptive biasing or pole-zero cancellation to enhance transient stability [15].

undershoot:欠冲，下冲

overshoot: 过冲

**Load Transient Response** quantifies the LDO's response to a sudden change in  $I_{LOAD}$ , as shown in Figure 2.7(b). Voltage deviations include undershoot during a load increase and overshoot during a load decrease, influenced by the LDO's loop bandwidth, output capacitance, and equivalent series resistance. For capacitor-based LDOs, a large  $C_O$  reduces deviations but increases system size, while capacitor-less LDOs rely on high loop bandwidth and internal compensation to limit  $\Delta V_{LR1}$  and  $\Delta V_{LR2}$ , typically targeting values below 100 mV for a 10  $\mu$ A to 100 mA load step. Key metrics also include recovery time (e.g., <5  $\mu$ s) and the presence of oscillations, which indicate loop stability.

Dynamic regulation is critical for applications with rapidly switching loads, such as digital processors, RF modules, and energy-harvesting systems, where voltage stability directly impacts performance. Optimizing dynamic performance requires high gain-bandwidth, fast error amplifier response, and robust compensation strategies, particularly in capacitor-less LDOs, where limited capacitance exacerbates transient deviations.

### 2.3.4 Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) describes the circuit's ability to suppress variations in output voltage  $V_{OUT}$  caused by disturbances on the supply voltage  $V_{IN}$ . A high PSR ensures that supply noise, especially high-frequency ripple or digital switching noise, does not propagate to sensitive analog loads. This is particularly critical in mixed-signal systems, RF front-ends, and sensor applications, where power supply ripple or switching noise can degrade signal integrity or cause malfunction.

As illustrated in Figure 2.8, an AC disturbance superimposed on the input voltage  $V_{IN}$  appears attenuated at the output  $V_{OUT}$ , ideally being completely rejected. The PSRR varies with frequency. At low frequencies, the error amplifier actively suppresses input noise through negative feedback. At higher frequencies, the suppression depends on the intrinsic bandwidth of the amplifier, the impedance of the pass device, and the output capacitor.

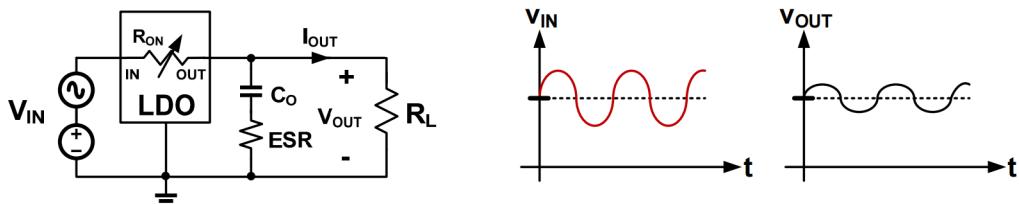


Figure 2.8 Power Supply Rejection Ratio

比率，比值

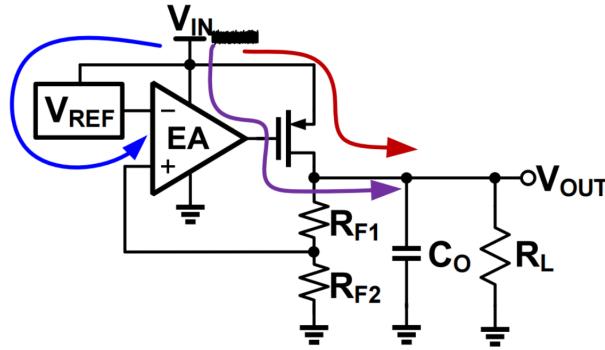
PSRR is defined as the ratio of the change in input voltage to the resulting change in output voltage, often expressed in decibels (dB):

$$\text{PSRR} = 20 \log \left| \frac{V_{IN}}{V_{OUT}} \right| \quad (2.6)$$

The greater the absolute value of PSRR, the better the ability to suppress ripple, resulting in a cleaner output voltage.

### Noise Paths in LDO

Understanding the noise propagation paths from  $V_{IN}$  to  $V_{OUT}$  is essential for optimizing PSRR, particularly in capacitor-less LDOs. As shown in Figure 2.9, supply disturbances couple to the output through multiple paths, each with frequency-dependent characteristics.



**Figure 2.9** Noise Paths in LDO

The key noise propagation paths from input to output include:

- **Reference Generator Path:** Noise on  $V_{IN}$  can modulate the bandgap reference voltage  $V_{REF}$ , which directly affects the control loop and shifts the target  $V_{OUT}$ .
- **Error Amplifier Path:** Since the error amplifier (EA) is often powered by  $V_{IN}$ , supply ripple can affect its internal gain or biasing conditions, indirectly passing noise to the gate of the pass device.
- **Pass Device Path:** Variations on  $V_{IN}$  can directly pass through the drain-source channel of the MOSFET pass device, especially at high frequencies where the loop gain is low.

The combined effect of these paths determines the LDO's overall PSRR, with each path's contribution varying by frequency. For example, at low frequencies (<1 kHz), the error amplifier's high loop gain provides strong rejection, while at high frequencies (>1 MHz), the pass device path dominates due to reduced loop response. In 22 nm FDX-Plus designs, achieving high PSRR across this spectrum requires careful optimization of each path, particularly for capacitor-less LDOs, where internal compensation must replace external filtering.

### 2.3.5 Efficiency and Accuracy

Efficiency and accuracy determine its power utilization and output voltage precision. This subsection defines current and power efficiency, their importance in LDO design, and the factors affecting the LDO's accuracy, including non-ideal effects.

#### Current Efficiency

The current efficiency  $\eta_I$  measures the ratio of the output current  $I_{OUT}$  to the total input current  $I_{IN}$ , accounting for the quiescent current  $I_Q$ :

$$\eta_I = \frac{I_{OUT}}{I_{IN}} \times 100 = \frac{I_{OUT}}{I_{OUT} + I_Q} \times 100, \quad (2.7)$$

where  $I_{IN} = I_{OUT} + I_Q$ . High current efficiency is crucial for minimizing power losses due to internal circuitry, especially at low load currents where  $I_Q$  can dominate.

#### Power Efficiency

The power efficiency  $\eta$  quantifies the ratio of output power to input power, considering both current and voltage drops across the LDO:

$$\eta = \frac{I_{OUT}V_{OUT}}{(I_{OUT} + I_Q)V_{IN}} \times 100 \approx \frac{V_{OUT}}{V_{IN}} \times 100, \quad (2.8)$$

where  $V_{OUT}$  and  $V_{IN}$  are the output and input voltages, respectively. The approximation holds when  $I_Q \ll I_{OUT}$ . Power efficiency highlights the impact of the dropout voltage ( $V_{IN} - V_{OUT}$ ), with higher efficiency achieved when  $V_{OUT}$  is closer to  $V_{IN}$ , a key advantage of LDOs over other regulators.

## Accuracy

The accuracy of an LDO reflects its ability to maintain  $V_{OUT}$  at the desired value, considering all non-ideal effects. These effects include: Line and load regulation ( $\Delta V_{LR}$ ,  $\Delta V_{LDR}$ ), Reference voltage drift ( $\Delta V_{O,REF}$ ), Error amplifier offset drift ( $\Delta V_{O,EA}$ ), Feedback resistor tolerance ( $\Delta V_R$ ). The overall accuracy is approximated as the sum of the absolute deviations and the root mean square of the error terms:

$$\text{Accuracy} \approx |\Delta V_{LR}| + |\Delta V_{LDR}| + \sqrt{\Delta V_{O,REF}^2 + \Delta V_{O,EA}^2 + \Delta V_R^2}. \quad (2.9)$$

This equation quantifies the cumulative impact of all non-idealities on  $V_{OUT}$ , guiding the design of LDOs for applications requiring high precision, such as analog and mixed-signal circuits.

## 2.4 Pole and Zero Distribution

The frequency response of a LDO regulator is fundamentally shaped by the locations of its poles and zeros, which directly influence loop stability, phase margin, and transient performance. Proper management of the pole-zero distribution is critical for ensuring robust operation, particularly in capacitor-less LDOs, where the absence of external capacitors limits traditional compensation strategies. The placement of poles and zeros affects the LDO's gain roll-off, phase margin (typically targeted at  $> 45^\circ$ ), and ability to handle dynamic load variations (e.g.,  $10 \mu\text{A}$  to  $100 \text{ mA}$ ).

### 2.4.1 Pole at the Output

The dominant pole in an LDO is typically located at the output node, resulting from the interaction between the output impedance and the **output capacitance  $C_O$** . Its frequency is given by:

$$f_{p1} = \frac{1}{2\pi R_{OUT} C_O}, \quad (2.10)$$

where  $R_{OUT}$  is the equivalent output resistance, determined by the parallel combination of the pass device's output impedance and the load resistance  $R_L$ . This pole dictates the low-frequency roll-off of the loop gain and plays a crucial role in establishing adequate phase margin. In capacitor-based LDOs, a large  $C_O$  pushes  $f_{p1}$  to lower frequencies, enhancing stability by providing a wide separation from higher-frequency poles. In capacitor-less LDOs, however,  $C_O$  is limited to small parasitic capacitances, shifting  $f_{p1}$  to higher frequencies and reducing phase margin, producing a pole shift, which necessitates advanced compensation techniques [15].

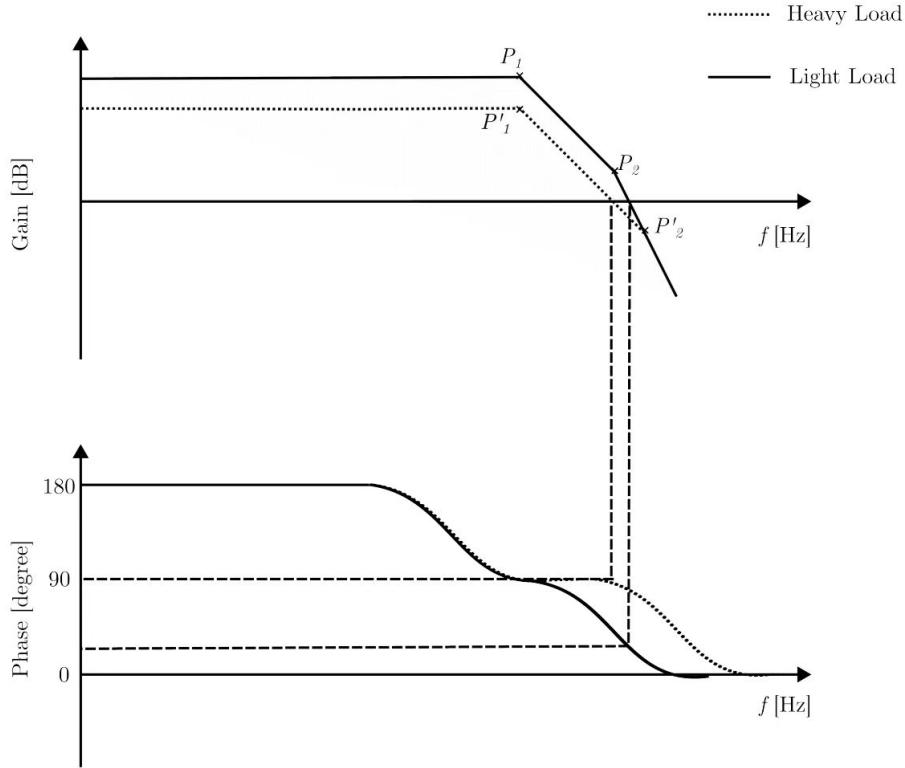
### 2.4.2 Pole at the Gate of the Pass Device

The second pole often arises at the gate of the pass transistor, introduced by the gate capacitance  $C_g$  (including parasitic and compensation capacitors) and the equivalent resistance  $R_g$  at the gate node. Its frequency is expressed as:

$$f_{p2} = \frac{1}{2\pi R_g C_g}. \quad (2.11)$$

In traditional LDOs with large output capacitors,  $f_{p2}$  is typically pushed to high frequencies due to low  $R_g$  (from the error amplifier's output stage) and small  $C_g$ , ensuring it lies beyond the unity-gain bandwidth. In capacitor-less LDOs, however, the reduced output capacitance shifts  $f_{p1}$  closer to  $f_{p2}$ , causing  $f_{p2}$  to fall within the unity-gain bandwidth, degrading phase margin and risking instability. This challenge is

exacerbated at light loads, where  $R_{\text{OUT}}$  increases, further separating  $f_{p1}$  and  $f_{p2}$ , as shown in Figure 2.10. Advanced compensation is required to mitigate this effect and maintain stability across load conditions.



**Figure 2.10** Influence of Pole Distribution on LDO Stability

### 2.4.3 ESR Zero

In capacitor-based LDOs, the equivalent series resistance (ESR) of the output capacitor  $C_O$  introduces a zero in the transfer function, given by:

$$f_z = \frac{1}{2\pi R_{\text{ESR}} C_O}. \quad (2.12)$$

This ESR zero adds a phase boost, counteracting the phase lag from the second pole  $f_{p2}$  and improving stability. For example, an ESR of 0.1–1  $\Omega$  with a 1  $\mu\text{F}$  capacitor places  $f_z$  in the 100 kHz to 1 MHz range, enhancing phase margin. Older LDO designs often specified a minimum ESR to ensure stability, but modern designs aim to minimize ESR dependence to reduce variability [15].

### 2.4.4 Additional High-Frequency Poles

Additional high-frequency poles arise from internal stages of the error amplifier, bias circuits, and parasitic capacitances within the LDO. These poles, often located beyond the unity-gain bandwidth, can cause gain peaking or phase dips if not properly managed. For instance, the error amplifier's internal nodes may introduce poles at frequencies determined by their parasitic capacitances and resistances, typically in the MHz range in 22 nm processes. In capacitor-less LDOs, these poles are more critical due to the higher-frequency placement of  $f_{p1}$  and  $f_{p2}$ , necessitating careful design to push them beyond the loop's crossover frequency. Techniques like cascaded amplifiers or low-capacitance biasing help minimize their impact [4].

The pole-zero distribution profoundly impacts the LDO's frequency response, stability, and transient behavior. At light loads, the large separation between  $f_{p1}$  and  $f_{p2}$  enhances phase margin but may limit

bandwidth, while at heavy loads, the poles' proximity can improve transient response but risks instability without proper compensation. By strategically introducing zeros (e.g., via Miller compensation or pole-zero cancellation), which can optimize phase margin and transient performance, ensuring reliable operation across the operating range.



# 3 Design and Analysis of LDO Circuit Architecture

The design specification of this paper is to meet a wide load current range (10 $\mu$ A-100mA) stabilized output voltage of 0.8 V at a supply voltage of 1.5 V. The circuit topologies of different LDOs are explored and studied: the PMOS type, the NMOS type, the traditional off-chip large-capacitor type, the voltage-type, and the current-type. This chapter describes the common structures of LDOs considered in the design and their limitations, discusses the compensation of the LDOs proposed in this paper and their detailed functionality.

## 3.1 Overall Circuit Analysis

As shown in Figure 3.1, a capacitor-less LDO typically consists of a pass transistor, an error amplifier, a reference voltage source, a feedback network, and a **On-chip small capacitor**.

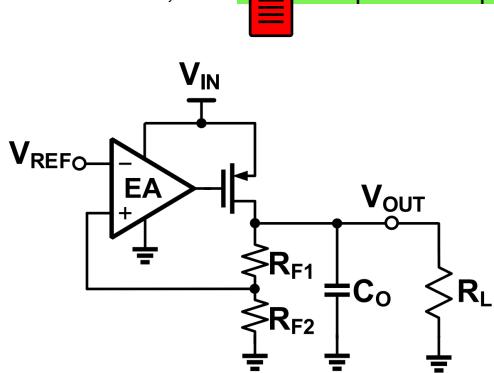


Figure 3.1 LDO without Output Capacitor

It can be considered as a whole with the LDO signal flow used to calculate the output voltage due to the input voltage  $V_{IN}$  shown in Figure 3.2. The graph includes the error amplifier (EA) with transfer function  $H_{EA}(s)$ , the pass device with transconductance  $g_{mP}$  and output impedance  $1/r_{dsp}$ , and the load impedance  $Z_L$ , which combines the load resistor  $R_L$ , output capacitor  $C_o$ , and equivalent series resistance (ESR).

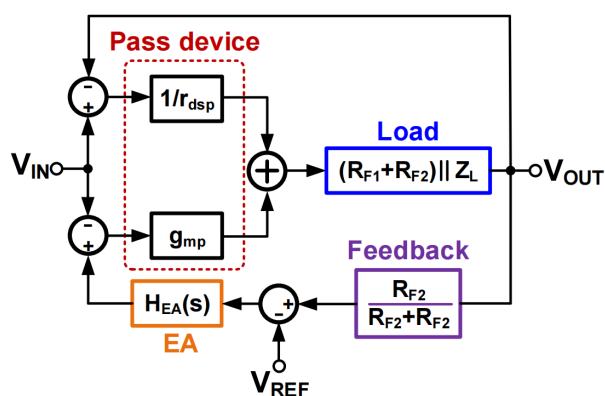


Figure 3.2 Signal Flow Graph of an LDO

The feedback factor is defined as:

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}. \quad (3.1)$$

Using Mason's Gain Rule, with the consideration of forward gain and loop gain, the transfer function is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{mP}R_{FL} + \frac{1}{r_{dsp}}R_{FL}}{1 + A_{EA0}g_{mP}R_{FL}\beta + \frac{R_{FL}}{r_{dsp}}}. \quad (3.2)$$

Assuming  $r_{dsp} \gg R_{FL}$ , so  $\frac{R_{FL}}{r_{dsp}} \approx 0$ , and factoring the denominator:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1 + g_{mP}r_{dsp}}{1 + \left(A_{EA0}g_{mP}R_{FL}\beta + \frac{R_{FL}}{r_{dsp}}\right)} \quad (3.3)$$

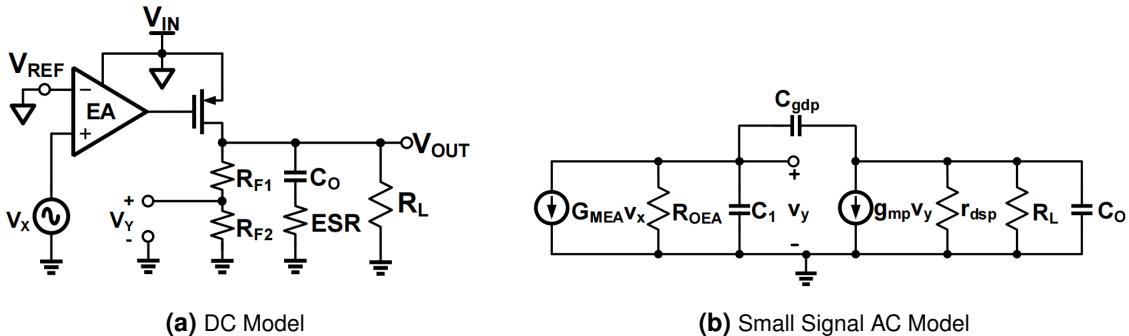
With  $g_{mP}r_{dsp} \gg 1$ , this further simplifies to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{A_{EA0}\beta}. \quad (3.4)$$

This result indicates that a high loop gain ( $A_{EA0}\beta$ ) and large pass device output impedance ( $r_{dsp}$ ) minimize the contribution of  $V_{IN}$  to  $V_{OUT}$ . This aligns with the LDO's design goal of rejecting input variations, achieving high PSRR and robust regulation [4].

### 3.1.1 Loop Gain Analysis

The loop gain of a LDO is a critical parameter that determines its stability, line regulation, and load regulation. This subsection derives the loop gain in both DC and frequency-domain forms, based on the schematic shown in Figure 3.3.



**Figure 3.3** Loop Gain Analysis

#### DC Loop Gain

The loop gain  $T(s)$  is defined as the gain around the feedback loop, measured as the ratio  $\frac{-V_Y}{V_X}$  when the loop is broken at points  $V_X$  and  $V_Y$ . For the PMOS LDO, the DC loop gain is derived considering the error amplifier (EA), PMOS pass device, and feedback network. The loop gain expression is:

$$T(s) = \frac{-V_Y}{V_X} = H_{EA}(s) \cdot g_{mP} \cdot [r_{dsp} \parallel (R_{F1} + R_{F2}) \parallel Z_L] \cdot \beta, \quad (3.5)$$

where  $H_{EA}(s)$  is the error amplifier gain,  $g_{mP}$  is the transconductance of the PMOS pass device,  $r_{dsp}$  is the PMOS output impedance,  $R_{F1}$  and  $R_{F2}$  are the feedback resistors,  $Z_L$  is the load impedance, and  $\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$  is the feedback factor. At DC,  $H_{EA}(s) = A_{EA0}$  and  $Z_L \approx R_L$ , simplifying the expression to:

$$T_0 \approx A_{EA0} \cdot g_{mP} \cdot r_{dsp} \cdot \beta. \quad (3.6)$$

A high DC loop gain  $T_0$  ensures effective suppression of input voltage variations and enhances the LDO's line regulation, as it minimizes the impact of  $V_{IN}$  on  $V_{OUT}$ .

## Loop Gain Transfer Function

To analyze the frequency-dependent behavior, the loop gain transfer function is derived by modeling the error amplifier with transconductance  $G_{MEA}$ , output resistance  $R_{OEA}$ , and capacitance  $C_1$ , and the PMOS pass device with transconductance  $g_{mP}$ , output impedance  $r_{dsp}$ , and gate-drain capacitance  $C_{gdp}$ . The output impedance at the load is:

$$R_{OUT} = r_{dsp} \parallel R_L \parallel (R_{F1} + R_{F2}). \quad (3.7)$$

The loop gain transfer function is given by:

$$T(s) = \frac{-V_Y(s)}{V_X(s)} = \frac{\beta G_{MEA} R_{OEA} g_{mP} R_{OUT} \left(1 - \frac{sC_{gdp}}{g_{mP}}\right)}{1 + bs + as^2}, \quad (3.8)$$

where the coefficients  $a$  and  $b$  account for the poles introduced by the capacitances:

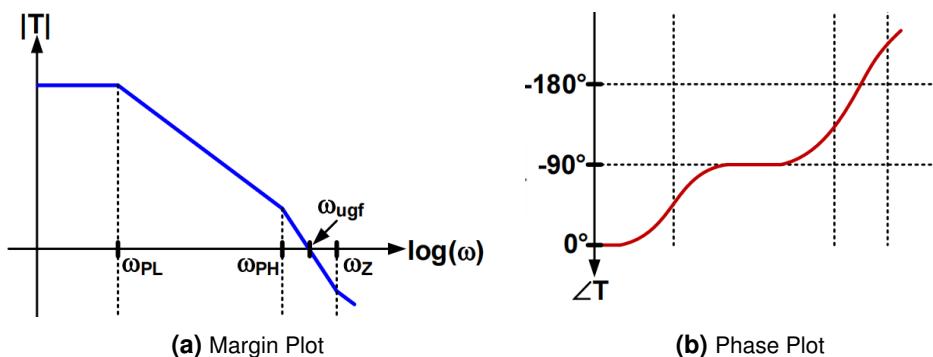
$$a = (C_o + C_{gdp})R_{OUT} + (C_1 + C_{gdp})R_{OEA} + g_{mP}R_{OUT}R_{OEA}C_{gdp}, \quad (3.9)$$

$$b = R_{OEA}R_{OUT}(C_1C_{gdp} + C_1C_o + C_oC_{gdp}). \quad (3.10)$$

The term  $1 - \frac{sC_{gdp}}{g_{mP}}$  introduces a right-half-plane zero due to the gate-drain capacitance  $C_{gdp}$ , which can affect stability. The denominator  $1 + bs + as^2$  indicates a second-order system with two poles, influenced by the capacitances  $C_o$ ,  $C_1$ , and  $C_{gdp}$ . A high loop gain at low frequencies ensures good regulation, while the frequency response must be carefully managed to maintain stability, often requiring compensation techniques to handle the poles and zero.

### 3.1.2 Approximate Pole and Zero Locations

The stability and transient response of a PMOS LDO are determined by the locations of its poles and zeros in the loop gain transfer function. This subsection analyzes the approximate pole and zero locations based on the schematic and Bode plot shown in Figure 3.4.



**Figure 3.4** PMOS Loop Gain Bode Plot

The LDO schematic includes an error amplifier, a PMOS pass device, feedback resistors  $R_{F1}$  and  $R_{F2}$ , an output capacitor  $C_o$ , and a load resistor  $R_L$ . The loop gain transfer function, derived previously, has two dominant poles and one right-half-plane (RHP) zero. The approximate locations of these poles and zero are given by:

$$\omega_{PL} \approx \frac{1}{R_{OUT}C_o}, \quad (3.11)$$

where  $R_{OUT} = r_{dsp} \parallel R_L \parallel (R_{F1} + R_{F2})$  is the output impedance at the load node, and  $C_o$  is the output capacitance. This pole, associated with the output node, typically dominates at low frequencies due to the large value of  $C_o$ .

$$\omega_{PH} \approx \frac{1}{R_{OEA}[C_1 + g_{mP}R_{OUT}C_{gdp}]}, \quad (3.12)$$

where  $R_{OEA}$  is the output resistance of the error amplifier,  $C_1$  is the capacitance at the error amplifier output,  $g_{mP}$  is the transconductance of the PMOS pass device, and  $C_{gdp}$  is the gate-drain capacitance of the PMOS. This pole arises from the error amplifier stage and is influenced by the Miller effect of  $C_{gdp}$ .

$$\omega_Z \approx \frac{g_{mP}}{C_{gdp}}, \quad (3.13)$$

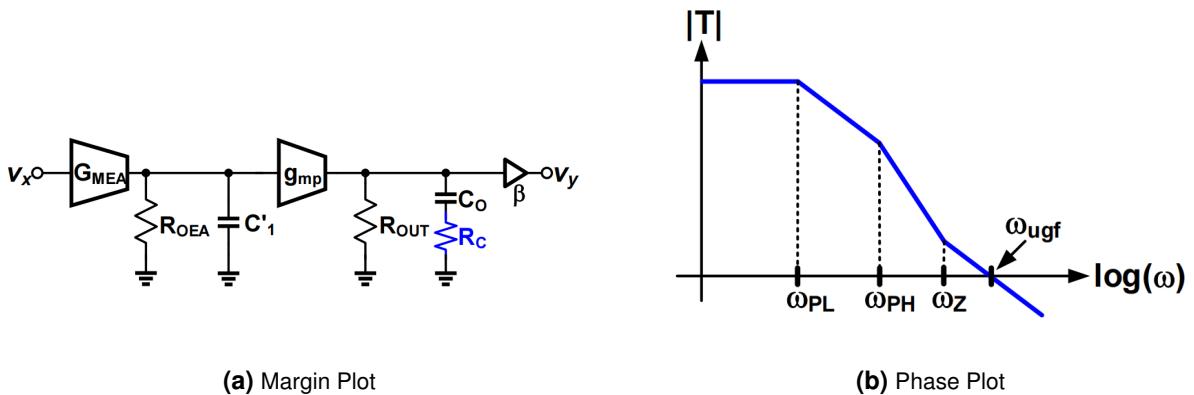
which is an RHP zero caused by the feedforward path through  $C_{gdp}$ . This zero can degrade the phase margin, potentially leading to instability if not properly compensated.

The Bode plot illustrates the magnitude  $|T|$  and phase  $\angle T$  of the loop gain. The low-frequency pole  $\omega_{PL}$  causes the initial roll-off in the magnitude and a phase shift towards  $-90^\circ$ . The second pole  $\omega_{PH}$  introduces further roll-off and pushes the phase towards  $-180^\circ$ . The RHP zero  $\omega_Z$  increases the magnitude slope and adds a positive phase shift, counteracting the phase loss from the poles. The unity-gain frequency  $\omega_{ugf}$  occurs where  $|T| = 1$ , and the phase margin is determined by the phase at this frequency. To ensure stability, the phase margin should be sufficiently positive (typically  $> 45^\circ$ ), which may require compensation techniques such as adding a series resistor with  $C_o$  to introduce a left-half-plane zero or adjusting  $C_1$  to shift  $\omega_{PH}$ .

In capacitor-less LDOs, due to the lack of large  $C_O$  capacitance, the poles described above also suffer from positional shifts influenced by the load current. For example, the main poles are mainly affected by the LDO outputs for light load currents ( $10 \mu\text{A}$ ) and are located mainly at the error amplifier outputs for heavy load currents ( $100\text{mA}$ ). Therefore, frequency compensation technique is necessary, as the small parasitic capacitance (e.g.,  $<100 \text{ pF}$ ) shifts  $\omega_Z$  and  $\omega_{PL}$  to impractically high frequencies. Therefore, several frequency compensation techniques like Miller compensation, Feed-forward compensation, buffer compensation, and so on will be discussed in the following.

### 3.2 Frequency Compensation with Series Resistors

Frequency compensation is critical for ensuring the stability of LDO regulators by managing the phase margin of the loop gain, particularly under varying load conditions. This section explores a compensation technique that introduces a series resistor  $R_C$  in conjunction with the output capacitor  $C_o$ , as depicted in Figure 3.5. This method, commonly used in capacitor-less LDOs, leverages the ESR to introduce a LHP zero, enhancing phase margin and stabilizing the feedback loop.



**Figure 3.5** LDO with frequency compensation using  $R_C$

### Modified Output Impedance

The addition of  $R_C$  in series with  $C_o$  modifies the output impedance  $Z_{out}$ . The impedance at the output node is:

$$Z_{out} = R_{OUT} \parallel \left( \frac{1}{sC_o} + R_C \right) = \frac{(1 + sR_C C_o) R_{OUT}}{1 + s(R_{OUT} + R_C) C_o}, \quad (3.14)$$

where  $R_{OUT} = r_{dsp} \parallel R_L \parallel (R_{F1} + R_{F2})$ . This introduces a LHP zero at  $\omega_Z = \frac{1}{R_C C_o}$  and shifts the output pole to  $\omega_{PL} = \frac{1}{(R_{OUT} + R_C) C_o}$ , improving the phase margin by counteracting the phase loss from the poles.

### Compensated Loop Gain Transfer Function

The loop gain transfer function  $T(s)$ , incorporating the RHP zero from the gate-drain capacitance and the new LHP zero from  $R_C$ , is:

$$T(s) = \frac{\beta G_{MEA} R_{OEA} g_{mP} R_{OUT} (1 + s/\omega_Z) (1 - s/\omega_{Z_{RHP}})}{(1 + s/\omega_{PH}) (1 + s/\omega_{PL})}, \quad (3.15)$$

where  $\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$ ,  $G_{MEA}$  is the transconductance of the error amplifier,  $R_{OEA}$  is its output resistance,  $g_{mP}$  is the transconductance, and the pole locations are:

$$\omega_{PH} = \frac{1}{R_{OEA} C_1}, \quad \omega_{PL} = \frac{1}{(R_{OUT} + R_C) C_o}, \quad \omega_Z = \frac{1}{R_C C_o}, \quad \omega_{Z_{RHP}} = \frac{g_{mP}}{C_{gdp}}. \quad (3.16)$$

### Bode Plot and Phase Margin

The compensated Bode plot illustrates the effect of the LHP zero. The magnitude  $|T|$  rolls off due to  $\omega_{PL}$ , but the zero  $\omega_Z$  flattens the magnitude before the second pole  $\omega_{PH}$  causes further roll-off. The phase starts at  $0^\circ$ , decreases due to the poles, but the LHP zero  $\omega_Z$  adds a positive phase shift, improving the phase margin. The unity-gain frequency  $\omega_{ugf}$  occurs where  $|T| = 1$ , and the phase margin is approximately:

$$\Phi_M \approx \arctan \left( \frac{\omega_{ugf}}{\omega_Z} \right). \quad (3.17)$$

By choosing  $R_C$  such that  $\omega_Z$  is positioned before  $\omega_{ugf}$ , the phase margin is enhanced, ensuring stability. Typically, a phase margin of  $45^\circ$  to  $60^\circ$  is targeted to balance stability and transient response.

## 3.3 Frequency Compensation with Feed-forward Capacitors

To improve the stability of an LDO, advanced frequency compensation techniques can eliminate the output pole  $\omega_{PF}$ , which often limits the phase margin. This subsection introduces a feedforward capacitor  $C_F$ , as shown in Figure 3.6.

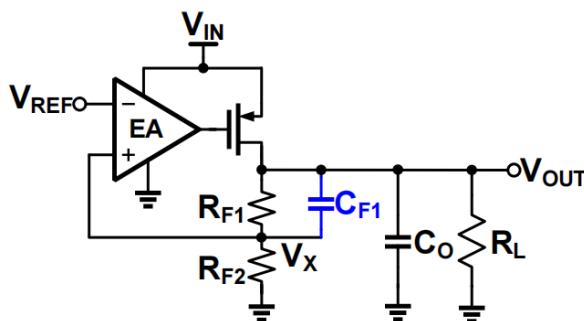


Figure 3.6 LDO with Feed-forward Capacitor

The feed-forward capacitor  $C_F$  is integrated into the LDO schematic, as shown. The feedback network's transfer function is:

$$\frac{V_X(s)}{V_{OUT}(s)} = \left( \frac{R_{F2}}{R_{F1} + R_{F2}} \right) \cdot \left( \frac{1 + sC_F R_{F1}}{1 + sC_F(R_{F1} \parallel R_{F2})} \right), \quad (3.18)$$

introducing a zero and a pole:

$$\omega_{ZF} = \frac{1}{R_{F1} C_F}, \quad \omega_{PF} = \frac{1}{(R_{F1} \parallel R_{F2}) C_F}. \quad (3.19)$$

At DC, the transfer function yields  $\frac{V_{OUT}}{V_{REF}} = 1 + \frac{R_{F1}}{R_{F2}}$ , maintaining the desired output voltage. The condition  $\omega_{ZF} \sim \omega_{PH} < \omega_{UGF}$  ensures the zero improves phase margin before the unity-gain frequency. With  $\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}$  and unchanged  $\omega_{PH}$ , the output pole shifts to:

$$\omega_{PL} = \frac{1}{R_{OUT} \left( C_o - \frac{C_F}{\beta} \right)} \quad (3.20)$$

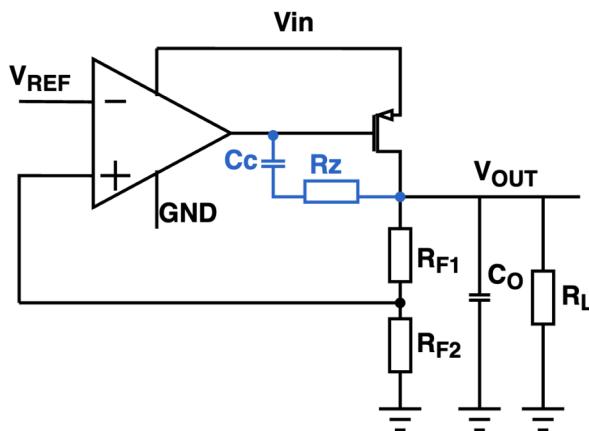
## 3.4 Miller Compensation

Miller compensation is a classical technique used to stabilize multi-stage amplifiers and LDO regulators by introducing a dominant pole through a capacitor connected between the output and input of a gain stage. In the context of LDO design, Miller compensation is often applied across the output and the gate of the pass transistor, using a capacitor  $C_C$  and optionally a series resistor  $R_Z$  to generate a beneficial zero.

### Principle of Miller Compensation

A capacitor-less LDO eliminates the large output capacitor  $C_o$ , reducing the overall area and enabling integration in systems where external capacitors are impractical, where  $C_o$  is reduced to a few hundred pF, significantly altering the frequency response. With a small  $C_o$ ,  $\omega_{PH}$  shifts to a higher frequency, making it difficult for the output pole to be dominant, as it typically is in a conventional LDO with a large  $C_o$ . Instead,  $\omega_{PL}$  at the EA output becomes the dominant pole due to the Miller effect of  $C_{gdp}$ , which amplifies the effective capacitance at the EA output. The RHP zero  $\omega_Z$  further complicates stability by introducing a negative phase shift.

To ensure stability, the EA output pole  $\omega_{PL}$  must be dominant, which can be achieved through Miller Compensation. As shown in Figure 3.7, it adds a compensation capacitor between the EA output and the pass device gate enhances the Miller effect, splitting the poles further and making  $\omega_{PL}$  dominant while pushing  $\omega_{PH}$  to higher frequencies.



**Figure 3.7** Miller Implementation

## Pole Splitting and Phase Margin Improvement

The key mechanism of Miller compensation is pole splitting. The dominant pole is pulled to a lower frequency, while the non-dominant pole is pushed to a higher frequency, increasing the separation between them and enhancing phase margin. The Miller capacitor effectively multiplies the capacitance seen at the input by the gain of the stage:

$$C_{\text{eq}} = C_C(1 + A) \quad (3.21)$$

The Miller capacitor  $C_C$  creates a feedback path that leverages the Miller effect to split the poles of the system. The dominant pole at the EA output is lowered, while the output pole is pushed to a higher frequency, improving phase margin.

While Miller compensation ensures stability across a wide range of load conditions, it introduces several trade-offs. The large  $C_C$  makes the LDO sensitive to load current variations, as changes in the load affect the effective pole locations. Additionally, Miller compensation results in poor high-frequency PSRR due to the direct coupling of high-frequency noise from the input to the output through  $C_C$ . This can degrade the LDO's ability to suppress supply noise at higher frequencies, impacting overall performance in noise-sensitive applications. This shifts the dominant pole to:

$$f_{p1} = \frac{1}{2\pi R_{\text{OUT}} C_{\text{eq}}} \quad (3.22)$$

## Use Series Resistors

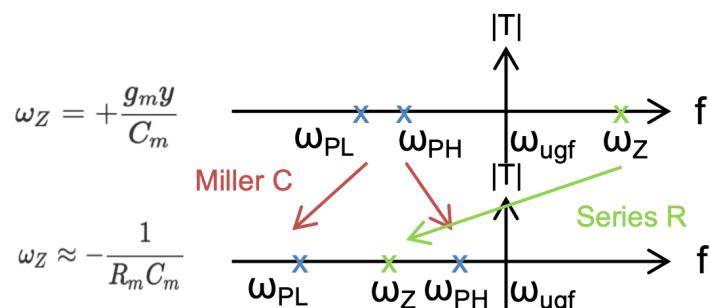
To further improve stability, a resistor  $R_Z$  can be added in series with the Miller capacitor to introduce a left-half-plane (LHP) zero that counteracts the phase lag of the second pole:

$$f_z = \frac{1}{2\pi R_Z C_C} \quad (3.23)$$

Choosing  $f_z \approx f_{p2}$  allows for partial or full phase cancellation, which enhances phase margin and transient response. Meanwhile, the second pole (often at the gate of the pass device) is pushed to higher frequencies, improving stability.

## Pole-Zero Movement in Miller Compensation

As shown in Figure 3.8, the plot illustrates the shift in poles and zeros due to Miller compensation. Initially, without compensation, the poles  $\omega_{PL}$  and  $\omega_{PH}$  are positioned closer to each other, leading to a limited bandwidth. With the addition of Miller  $C$ , the dominant pole moves to a lower frequency, while the non-dominant pole moves to a higher frequency. However, an RHP zero also emerges, potentially destabilizing the system. Adding a series resistor mitigates this issue by shifting the zero to the LHP, aiding in phase margin enhancement.



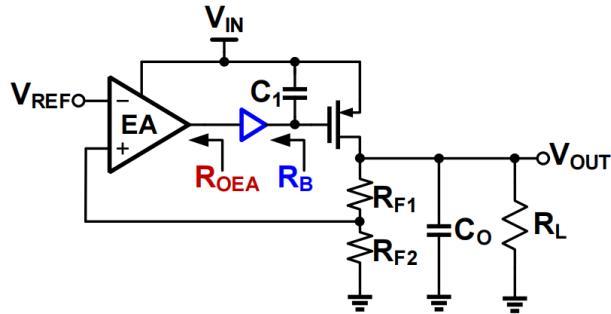
**Figure 3.8** Pole-Zero Movement in Miller Compensation

Overall, Miller compensation remains a robust and widely-used strategy in LDO design, especially when paired with techniques like nulling resistors and gain-boosted amplifiers to achieve stability under varying load and process conditions.

### 3.5 Frequency Compensation with a Buffer

In modern LDO designs, especially capacitor-less architectures, conventional Miller or ESR-based compensation may be insufficient due to the absence of a large output capacitor or the capacitive nature of the gate node of the pass transistor. In such cases, introducing a buffer stage between the error amplifier and the gate of the pass device provides an effective means of frequency compensation.

When using an NMOS pass transistor, the gate requires a voltage higher than the output voltage and exhibits high input capacitance. Directly driving this capacitive gate from the error amplifier introduces a low-frequency pole, significantly degrading phase margin. Frequency compensation for an LDO aims to improve stability by shifting the pole  $\omega_{PH}$  beyond the unity-gain frequency  $\omega_{ugf}$ . This subsection explores the approach of reducing the capacitance  $C_1$  at the EA output and using a buffer to mitigate loading effects, as shown in Figure 3.9.



**Figure 3.9** Frequency Compensation with a Buffer

The buffer isolates the dominant pole at the output node from the second pole at the gate of the pass device, effectively pushing the latter to a higher frequency. By reducing the impedance seen by the gate node, the second pole is shifted beyond the unity-gain bandwidth, resulting in improved phase margin and stability. Two dominant poles  $\omega_{PL}$  at the output node and  $\omega_{PH}$  at the EA output are given by:

$$\omega_{PL} \approx \frac{1}{R_L C_o}, \quad \omega_{PH} \approx \frac{1}{R_{OEA} C_1} \quad (3.24)$$

where  $R_L$  is the load resistance,  $C_o$  is the output capacitance,  $R_{OEA}$  is the EA output resistance, and  $C_1$  is the capacitance at the EA output. To improve phase margin,  $\omega_{PH}$  must be shifted beyond  $\omega_{ugf}$ . Reducing  $C_1$  increases  $\omega_{PH}$ , but  $C_1$  is constrained by the load current  $I_{LOAD}$  and the pass device's saturation voltage  $V_{DSAT}$ . Additionally, reducing  $R_{OEA}$  to increase  $\omega_{PH}$  degrades load and line regulation due to lower EA gain.

#### Using a Buffer to Shield

To reduce  $C_1$  without compromising the EA, a buffer is inserted between the EA output and  $C_1$ :

$$\omega_{PH} = \frac{1}{R_{OEA} C_x}, \quad C_x = C_{OEA} + C_{IBUF} \ll C_1, \quad (3.25)$$

$$\omega_{PB} = \frac{1}{R_B C_1}, \quad R_B \ll R_{OEA}, \quad (3.26)$$

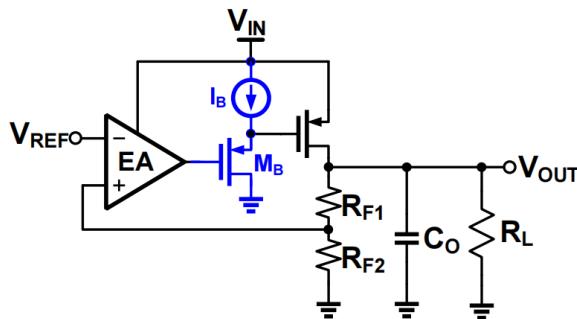
where  $C_x$  is the combined capacitance at the EA output (including the buffer's input capacitance  $C_{IBUF}$ ), and  $R_B$  is the buffer's output resistance. The buffer isolates  $C_1$ , introducing a new pole  $\omega_{PB}$  at a higher frequency due to the low  $R_B$ , ensuring minimal impact on the phase margin.

## Buffer Implementation

Buffer-assisted compensation involves inserting a unity-gain buffer, often a source follower or a simple amplifier stage, between the error amplifier output and the gate of the pass transistor. The main purpose of the buffer is to isolate the capacitive load at the gate of the power transistor from the high-impedance output of the error amplifier. This configuration modifies the pole-zero distribution without introducing a detrimental RHP zero. A source follower is used as the buffer with:

$$R_B \approx \frac{1}{g_{mB}} \propto \frac{1}{(W/L)_{I_B}}, \quad (3.27)$$

where  $g_{mB}$  is the transconductance of the buffer transistor, and  $(W/L)_{I_B}$  is its aspect ratio with bias current  $I_B$ . The source follower has a small input capacitance, but its high output impedance can lead to increased power consumption. Feedback can be used to lower the output impedance, though this increases power usage.



**Figure 3.10** Buffer Implementation

While buffers can greatly enhance stability and bandwidth, they also introduce additional design complexity and power consumption. It must ensure that the buffer itself does not become a source of instability. In ultra-low-power designs, the trade-off between quiescent current and transient performance must also be carefully considered.

Frequency compensation using a buffer is a powerful technique to overcome the limitations of Miller compensation. Isolating high capacitance nodes and eliminating undesirable RHP zeros enables better control over the system's dynamic response and ensures robust stability across varying load and process conditions. This makes it particularly suitable for modern, capacitor-less LDO designs and high-speed analog systems. Unfortunately, this design was not well realized in the experimental study of this paper.



# 4 Implementation and Preparation of Sub-circuits

Before carrying out circuit simulations and performance evaluations, several essential building blocks and theoretical foundations must be established. This chapter outlines the preparatory work required for the later implementation of the capacitor-less LDO design. It includes the pass transistors comparison, the design and analysis of key analog modules such as the operational transconductance amplifier (OTA), bandgap voltage reference, and a source-follower-based pre-filter. These components serve as the functional basis for the proposed architecture, ensuring stability, accurate reference generation, and improved PSRR in the subsequent experimental stages.

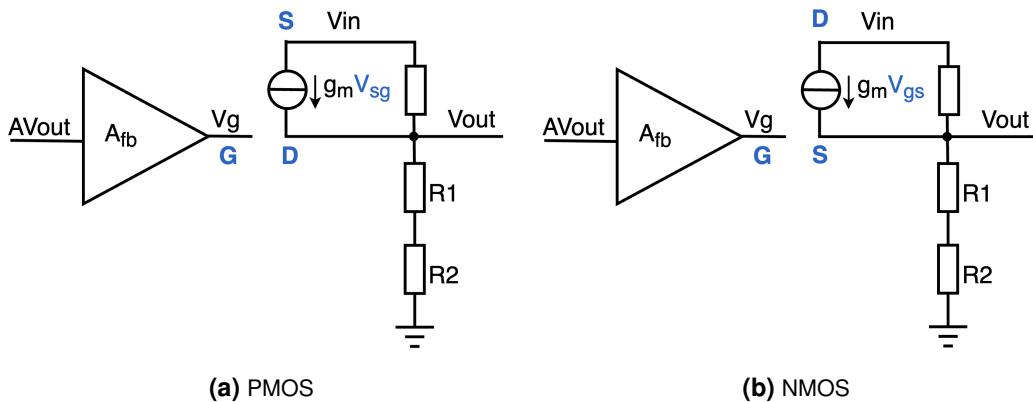
## 4.1 Pass Transistors

The pass element is a significant part of the LDO. A wide load current range has to flow through it. Compared to other transistors of the IC, which conduct only a few  $\mu\text{A}$ , conducting mA is challenging. The current through pass transistor is expressed as follows:

$$I_D = \frac{1}{2} K_p \frac{W}{L} (U_{GS,p} - U_{th,p})^2 \quad (4.1)$$

The ratio  $\frac{W}{L}$  should be large enough to supply a large load current. To keep the size of the pass transistor as small as possible, the length is often chosen to be minimal.

In LDO design, the choice of pass transistor, either PMOS or NMOS, significantly impacts performance parameters such as driving voltage requirements, load capacity, chip area, and PSRR, particularly at high frequencies. A clear comparison is presented in Fig. 4.1.



**Figure 4.1** Comparison between PMOS and NMOS

### Driving Voltage Consideration

One major difference between PMOS and NMOS pass transistors lies in how their gate voltages must be driven. For PMOS devices, the gate voltage must be lower than the input voltage ( $V_{gate} < V_{in}$ ), which allows the error amplifier to directly drive the gate without additional circuitry. In contrast, NMOS transistors require a gate voltage higher than the input ( $V_{gate} > V_{in}$ ), necessitating the use of a charge pump or boosted gate driver. While this adds design complexity, it enables superior performance in some metrics, especially when using advanced processes that support on-chip charge pumps.

## Load Drive Capability and Area Efficiency

Due to the mobility difference between electrons and holes ( $\mu_n > \mu_p$ ), NMOS transistors generally offer higher drive strength than their PMOS counterparts. As a result, NMOS pass transistors can achieve the same load current capacity with smaller  $W/L$  ratios, leading to a smaller silicon area. Conversely, PMOS devices require larger dimensions for the same drive capability, increasing layout area.

### High-Frequency PSRR Performance

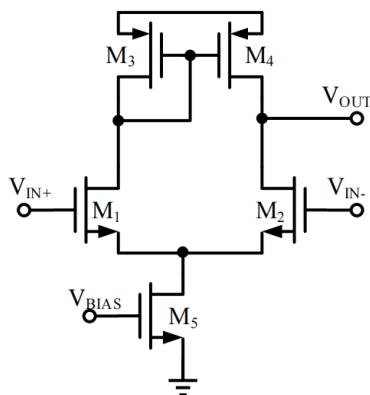
In high-frequency domains, PSRR becomes critical, especially in systems with sensitive analog or clock circuits. PMOS devices are more susceptible to high-frequency noise because variations on  $V_{in}$  can couple directly to the gate through the source, degrading PSRR. NMOS transistors, however, benefit from a source-driven configuration, where the boosted gate voltage isolates the device from input supply fluctuations, resulting in better high-frequency PSRR.

## 4.2 Operational Transconductance Amplifier

Traditional amplifiers, such as single-stage common-source or Miller-compensated topologies, often face limitations in LDO applications. Single-stage amplifiers may not provide sufficient open-loop gain to ensure precise output regulation, while two-stage structures, though capable of higher gain, introduce complexity in frequency compensation and can suffer from poor phase margin or slower transient response. These issues are particularly problematic in modern low-voltage, fast-response LDOs.

### 4.2.1 Simple OTA Architecture

Figure 4.2 depicts a fundamental OTA structure, designed to convert a differential input voltage into a proportional output current. The core consists of a differential input stage formed by transistors  $M_1$  and  $M_2$ , which are driven by input voltages  $V_{IN+}$  and  $V_{IN-}$ . These transistors operate as a differential pair, biased by a tail current source  $M_5$ , which is controlled by the bias voltage  $V_{BIAS}$ . The differential pair is loaded by a current mirror composed of transistors  $M_3$  and  $M_4$ , which converts the differential current into a single-ended output voltage  $V_{OUT}$  at the drain of  $M_4$ .



**Figure 4.2** Simple Transconductance Amplifier Structure

The small-signal voltage gain of the amplifier is derived from the transconductance of the input stage and the output impedance. Assuming  $M_1$  and  $M_2$  are matched, the gain is given by:

$$A_v = -g_{m1} (r_{o2} \parallel r_{o4}), \quad (4.2)$$

where  $g_{m1}$  is the transconductance of  $M_1$  or  $M_2$ , and  $r_{o2}$  and  $r_{o4}$  are the output resistances of  $M_2$  and  $M_4$ , respectively. The negative sign reflects the phase inversion typical of a single-stage amplifier with a PMOS current mirror load.

The output resistance of the amplifier is determined by the parallel combination of the output resistances of  $M_2$  and  $M_4$ :  $R_{\text{out}} = r_{o2} \parallel r_{o4}$ . The output voltage swing is constrained by the circuit's topology and the transistors' operating regions. The output voltage  $V_{\text{OUT}}$  must remain within the following range to ensure proper operation:

$$V_{\text{CM}} - V_{\text{th},M2} \leq V_{\text{OUT}} \leq V_{\text{DD}} - V_{\text{sat},M4}, \quad (4.3)$$

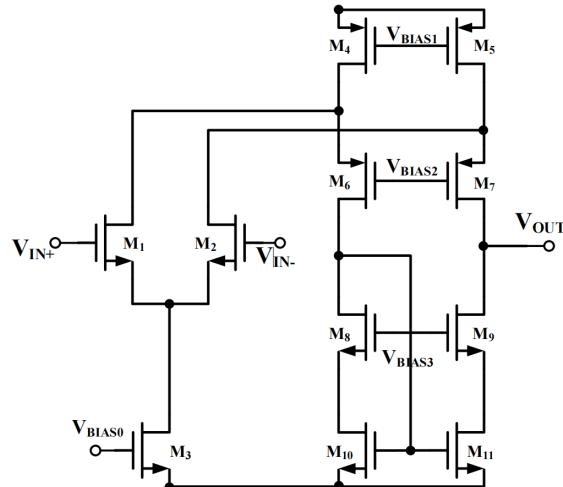
where  $V_{\text{CM}}$  is the common-mode input voltage,  $V_{\text{th},M2}$  is the threshold voltage of  $M_2$ ,  $V_{\text{DD}}$  is the supply voltage, and  $V_{\text{sat},M4}$  is the saturation voltage of  $M_4$ .

This simple transconductance amplifier offers several advantages, including high input impedance and linear voltage-to-current conversion, due to the differential pair's properties. The current mirror formed by  $M_3$  and  $M_4$  ensures symmetry in the differential-to-single-ended conversion, enhancing the output signal strength and rejecting common-mode noise. Meanwhile, the tail current source  $M_5$  provides a stable bias current, improving the amplifier's linearity and overall performance.

However, this basic design has limitations. The single-stage architecture provides moderate gain, and the output swing is limited by the supply voltage and transistor characteristics. Additionally, the amplifier's CMRR and PSRR may be suboptimal without further enhancements, such as cascoding or additional biasing circuits. In practical designs, compensation techniques, such as folded cascode OTAs, will be better to improve phase margin and stability.

#### 4.2.2 Folded Cascode OTA Architecture

The schematic of the proposed folded cascode OTA is presented in Figure 4.3, which illustrates a differential input stage comprising transistors  $M_1$  and  $M_2$ , driven by input voltages  $V_{\text{IN}+}$  and  $V_{\text{IN}-}$ . The differential pair is biased by transistor  $M_3$ , controlled by the bias voltage  $V_{\text{BIAS}0}$ , ensuring stable operation of the input stage.



**Figure 4.3** Folded Cascode OTA Architecture

The cascode structure is realized using transistors  $M_4$  to  $M_7$ , with bias voltages  $V_{\text{BIAS}1}$  and  $V_{\text{BIAS}2}$  applied to  $M_4$  and  $M_5$ , and  $M_6$  and  $M_7$ , respectively. This configuration significantly boosts the output impedance, thereby enhancing the overall voltage gain. The folding mechanism is implemented through transistors  $M_8$  and  $M_9$ , biased by  $V_{\text{BIAS}3}$ , which redirect the differential pair's current to the output stage. Transistors  $M_{10}$  and  $M_{11}$  form a current mirror load, facilitating precise current steering to the output node  $V_{\text{OUT}}$ .

The voltage gain of the folded cascode OTA is expressed as:

$$A_v = -g_{m1}(r_{o6} \parallel r_{o8}) \approx -g_{m1} \cdot g_{m6}r_{o6}(r_{o1} \parallel r_{o4}) \parallel g_{m8}r_{o8}r_{o10}, \quad (4.4)$$

where  $g_{m1}$  is the transconductance of  $M_1$ , and the output impedance is amplified by the cascode effect, involving the transconductances and output resistances of the cascode and mirror transistors. The approximation holds under high-gain conditions, where cascode transistors dominate the impedance. The output resistance, a critical parameter for gain, is given by:

$$R_{\text{out}} = r_{o4} \parallel r_{o6} \parallel r_{o8} \parallel r_{o10}, \quad (4.5)$$

The output voltage swing is notably flexible, as it is not tightly constrained by the common-mode input voltage, making it suitable for driving large loads. The swing range is defined as:

$$2V_{\text{sat,n}} \leq V_{\text{OUT}} \leq V_{\text{DD}} - 2V_{\text{sat,p}}, \quad (4.6)$$

where  $V_{\text{sat,n}}$  and  $V_{\text{sat,p}}$  are the saturation voltages of the NMOS and PMOS transistors, respectively, and  $V_{\text{DD}}$  is the supply voltage.

The folded cascode OTAs offer a balanced solution by providing high gain, a wide input common-mode range, and improved frequency response, all within a single-stage architecture. Their structure avoids the need for complex compensation and supports low-voltage operation, making them ideal for capacitor-less LDOs. In the general circuits of this design, folded cascode operational transconductance amplifiers are used; in the low-power design, simple operational amplifiers with transconductance structures are selected in consideration of bandwidth and other factors.

#### 4.2.3 Results

Operational amplifiers are designed and evaluated in two configurations: a simple transconductance amplifier for ultra-low quiescent current applications, and a folded cascode topology targeting high gain and wide bandwidth performance. In both architectures, the reference current is injected into the input stage via a current mirror, setting the operating point and defining key trade-offs between gain-bandwidth product (GBW), phase margin, and PSRR.

As shown in Equation 4.1, the gain of the operational amplifier depends not only on the output impedance but also on the input transconductance, where  $g_m$  is the transconductance of the input differential pair and  $R_{\text{out}}$  is the output impedance of the amplifier. Table 4.1 summarizes the simulation results of the folded cascode and simple OTA structures.

	<b>Folded Cascode OTA</b> ( $V_{\text{ref}} = 600$ mV)	<b>Simple OTA</b> ( $V_{\text{ref}} = 600$ mV)
GBW	26.5764 MHz	737.931 kHz
DC Gain [dB]	82.1762	53.6735
Phase Margin (with $C_o = 1$ pF)	89.14°	69.65°
PSRR @1Hz [dB]	-86.4865	-55.1993

**Table 4.1** Simulation Results of Folded Cascode OTA and Simple OTA

Both designs essentially meet the requirements. The folded cascode OTA demonstrates excellent performance across all key metrics. Its gain bandwidth product of 26.6 MHz helps it respond quickly to transient changes. In terms of DC gain, the folded cascode design provides approximately 82 dB, and the high gain ensures accurate error correction and higher regulation accuracy. It provides greater phase margins, offering greater safety margins for variable load or parasitic condition situations. Furthermore, the folded cascode OTA's power supply rejection ratio (PSRR) of -86.5 dB at 1 Hz provides a strong guarantee of the overall system PSRR. However, the design of the simple OTA is slightly lacking compared to the folded

cascode OTA due to its topological characteristics and the limitation of low quiescent current subthreshold operation.

## 4.3 Bandgap Voltage Reference

A stable and accurate reference voltage is essential for the operation of linear voltage regulators and other analog building blocks. The Bandgap Voltage Reference (BGR) circuit is widely used in integrated circuits due to its ability to generate a temperature-independent voltage, which remains stable across variations in supply voltage, temperature, and process corners.

In the LDO design, the bandgap reference provides the reference voltage  $V_{\text{ref}}$  for the error amplifier, ensuring consistent regulation of the output regardless of operating conditions. The accuracy and low drift of the BGR are critical to achieving tight output voltage tolerance, especially in precision applications such as clock generation or analog signal conditioning.

### 4.3.1 Fundamental Principle

The principle behind a BGR is to combine two voltage components with opposite temperature coefficients: the base-emitter voltage of a bipolar junction transistor  $V_{\text{BE}}$ , where a CTAT (Complementary-To-Absolute-Temperature) decreases with increasing temperature, and a PTAT (Proportional To Absolute Temperature) voltage that increases linearly with temperature. The basis of the bandgap voltage reference is to combine two voltages with opposite temperature coefficients to achieve a reference voltage that is independent of temperature.

Specifically, a voltage with a negative temperature coefficient, such as the base-emitter voltage  $V_{\text{BE}}$  of a bipolar junction transistor, is summed with a voltage that has a positive temperature coefficient  $V_+$  in PTAT voltage, typically generated from a difference in  $V_{\text{BE}}$ , and a negative temperature coefficient  $V_-$  in CTAT voltage. By selecting proper weighting coefficients, the temperature dependencies can be canceled, resulting in a stable reference voltage  $V_{\text{REF}}$  [18]:

$$V_{\text{REF}} = \alpha \cdot V_+ + \beta \cdot V_- \quad (4.7)$$

#### Negative Temperature Coefficient Voltage

For a bipolar transistor, the base-emitter voltage  $V_{\text{BE}}$  decreases with increasing temperature. According to the Shockley equation:

$$I_C = I_S \exp \left( \frac{V_{\text{BE}}}{V_T} \right) \quad (4.8)$$

$V_T$  represents the thermal voltage, which is defined as  $kT/q$ , where  $k$  is the Boltzmann constant and  $q$  is the charge of an electron.  $I_S$  denotes the saturation current of a bipolar junction transistor (BJT). Differentiating  $V_{\text{BE}}$  with respect to temperature yields the temperature coefficient:

$$\frac{\partial V_{\text{BE}}}{\partial T} = \frac{V_{\text{BE}} - (4 + m)V_T}{T} - \frac{E_g}{qT} \quad (4.9)$$

Here,  $m \approx -1.5$ , and  $E_g = 1.12 \text{ eV}$  is the bandgap energy of silicon. As seen in Eq. 4.9, the temperature coefficient of the  $V_{\text{BE}}$  voltage is itself temperature dependent.

#### Positive Temperature Coefficient Voltage

By using two BJTs biased at different current densities, the difference in their  $V_{\text{BE}}$  voltages becomes a PTAT voltage. This difference is:

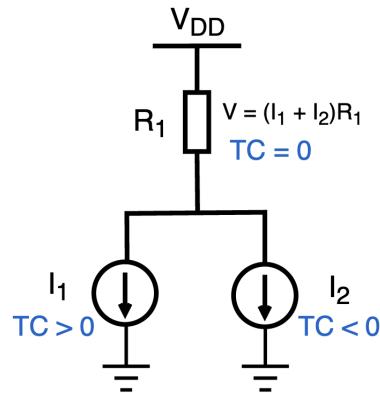
$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} = V_T \ln n \quad (4.10)$$

where  $n$  is the current density ratio between the two transistors. This voltage increases linearly with temperature, and its derivative is:

$$\frac{\partial(\Delta V_{BE})}{\partial T} = \frac{k}{q} \ln(n) \quad (4.11)$$

### 4.3.2 Zero Temperature Coefficient

The above positive and negative temperature coefficient voltages are used to realize a zero temperature coefficient (ZTC), i.e., to obtain an essentially temperature-independent bandgap reference voltage. As shown in Figure 4.4, this is realized by combining two voltages with opposing temperature behaviors, a CTAT voltage and a PTAT voltage.



**Figure 4.4** Zero Temperature Coefficient

For instance, a PTAT current can be formed as  $I_1 = V_T \ln n / R$ , and a CTAT current as  $I_2 = V_{BE} / R$ . By summing these two currents and converting the result into a voltage using a resistor, a reference voltage with near-zero temperature dependence can be achieved. The CTAT component is typically the base-emitter voltage  $V_{BE}$  of a bipolar junction transistor, which decreases with increasing temperature at a rate of approximately  $-1.5 \text{ mV}/^\circ\text{C}$ . The PTAT component is derived from the voltage difference between two BJTs operating at different current densities,  $\Delta V_{BE}$ , which increases linearly with temperature. Mathematically, the reference voltage can be expressed as:

$$V_{REF} = V_{BE} + \beta \cdot \Delta V_{BE} = V_{BE} + \beta \cdot V_T \ln(n) \quad (4.12)$$

where  $V_T = \frac{kT}{q}$  is the thermal voltage,  $n$  is the emitter area or current density ratio of the two BJTs, and  $\beta$  is a weighting factor set by resistor ratios in the circuit.

To achieve zero temperature coefficient, the temperature derivatives of the two components must cancel:

$$\frac{dV_{REF}}{dT} = \frac{dV_{BE}}{dT} + \beta \cdot \frac{d(\Delta V_{BE})}{dT} = 0 \quad (4.13)$$

Given typical values:

$$\frac{dV_{BE}}{dT} \approx -1.5 \text{ mV}/^\circ\text{C}, \quad \frac{d(\Delta V_{BE})}{dT} = \frac{k}{q} \ln(n) \approx +0.087 \text{ mV}/^\circ\text{C}$$

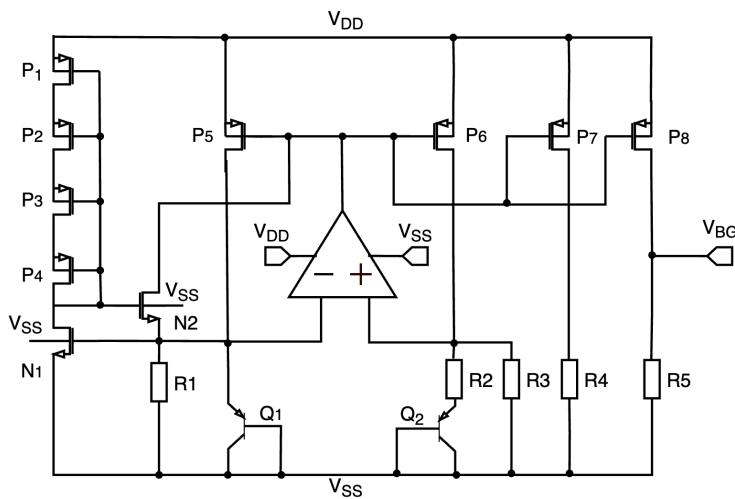
Solving the cancellation condition yields:

$$\beta \cdot \ln(n) = \frac{1.5}{0.087} \approx 17.2 \quad (4.14)$$

This result shows that a scaling factor  $\beta$  and current density ratio  $n$  can be chosen such that their product satisfies the cancellation condition, resulting in a reference voltage with a near-zero temperature coefficient. This condition sets the required resistor ratio or current ratio in the bandgap circuit to achieve minimal temperature sensitivity. When properly tuned, the reference voltage  $V_{\text{REF}}$  will exhibit a flat temperature curve near the designed operating point[19].

### 4.3.3 Implementation

Figure 4.5 illustrates a typical implementation of a BGR circuit using bipolar transistors  $Q_1$  and  $Q_2$ , as well as MOSFET current mirrors and a feedback operational amplifier. This circuit topology generates a temperature-independent reference voltage  $V_{\text{BG}}$  by summing a CTAT component  $V_{\text{BE}}$  and a PTAT component  $\Delta V_{\text{BE}}$  with appropriate weighting.



**Figure 4.5** Bandgap Voltage Reference Design

Transistors  $Q_1$  and  $Q_2$  are configured to operate at different current densities by sizing their emitter areas differently or by introducing a resistor  $R_1$  in series with  $Q_1$ . This results in a  $V_{\text{BE}}$  difference between the two BJTs, producing the PTAT voltage:

$$\Delta V_{\text{BE}} = V_T \ln \left( \frac{J_2}{J_1} \right) \quad (4.15)$$

This PTAT voltage appears across resistor  $R_1$ , generating a PTAT current, which then flows through  $R_2-R_5$  to develop a voltage with a positive temperature coefficient.

MOSFETs  $P_1-P_4$  and  $N_1-N_2$  form the startup and biasing circuits, ensuring proper initial conditions for the BGR to operate.  $P_5$ ,  $P_6$ , and  $P_7$  implement current mirrors to replicate and distribute the PTAT current across the resistor ladder ( $R_2$  to  $R_5$ ). Finally,  $P_8$  buffers the output and provides the stable reference voltage  $V_{\text{BG}}$  to the rest of the system. The design achieves an output of 1.21 V with a temperature coefficient of 21.94 ppm/ $^{\circ}\text{C}$ , and an output of 597.3 mV with a temperature coefficient of 76.74 ppm/ $^{\circ}\text{C}$ . However, since the performance is not fully optimized, a voltage source is used to directly provide the bandgap reference in the following experimental design.

## 4.4 Source-Follower-Based Pre-Filter

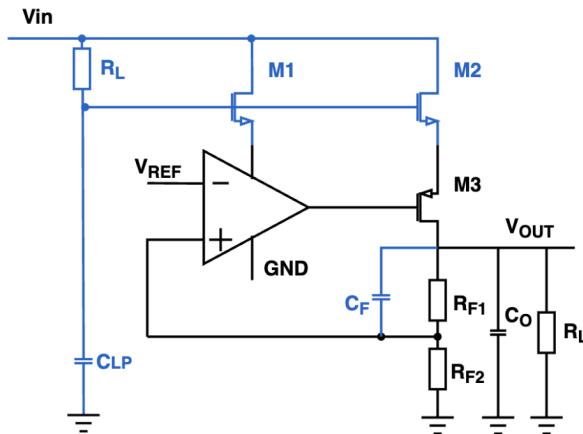
In modern highly integrated mixed-signal systems, one of the major design challenges is reducing interference between co-existing analog and digital circuits. Among the various coupling mechanisms, supply

line noise is particularly problematic, especially in cases where switching circuits, such as digital logic or switch-mode power converters, share the same supply with noise-sensitive analog blocks. To suppress such noise, linear voltage regulators are widely used due to their ability to isolate and clean up the supply voltage.

Several methods have been explored to enhance the PSR of linear regulators, which involve placing a pre-filter in front of the regulator, cascading multiple regulator stages [20], and Feedforward ripple cancellation [21]. A more practical solution is to insert a source-follower-based pre-filter between the RC filter and the regulator. This method allows the filter to operate at high impedance while still delivering the necessary current.

#### 4.4.1 Circuit Design

In order to improve the PSRR of the LDO system to reduce the effect of input noise, a pre-filter architecture based on a source follower [22], as shown in Fig. 4.6. The regulator is designed to output a clean supply and uses an NMOS pass transistor M3 due to its inherently low output impedance in source-follower configuration. This helps to reduce voltage variations at the output and contributes to PSRR improvement.



**Figure 4.6** Source Follower Based Pre-Filter

The pre-filter stage consists of a low-pass RC filter formed by  $R_{LP1}$ ,  $C_{LP1}$ , followed by two source followers, M1 and M2. Transistor M1 decouples the input voltage from the error amplifier EA1, while M2 provides isolation for the gate of the pass transistor M3. Splitting the source-follower stage into two devices reduces the current load on M1 and M2, which allows for narrower devices, improving integration and reducing parasitic coupling. To enhance loop stability and transient behavior, a capacitor  $C_F$  is added in a feedforward path to introduce a zero in the frequency response, improving phase margin. The resistors  $R_{F1}$  and  $R_{F2}$  form the voltage divider for feedback regulation.

The output capacitor  $C_O$  is fully integrated on-chip with a small value. This is sufficient to suppress high-frequency noise without occupying large chip area.

#### 4.4.2 Results and Challenges

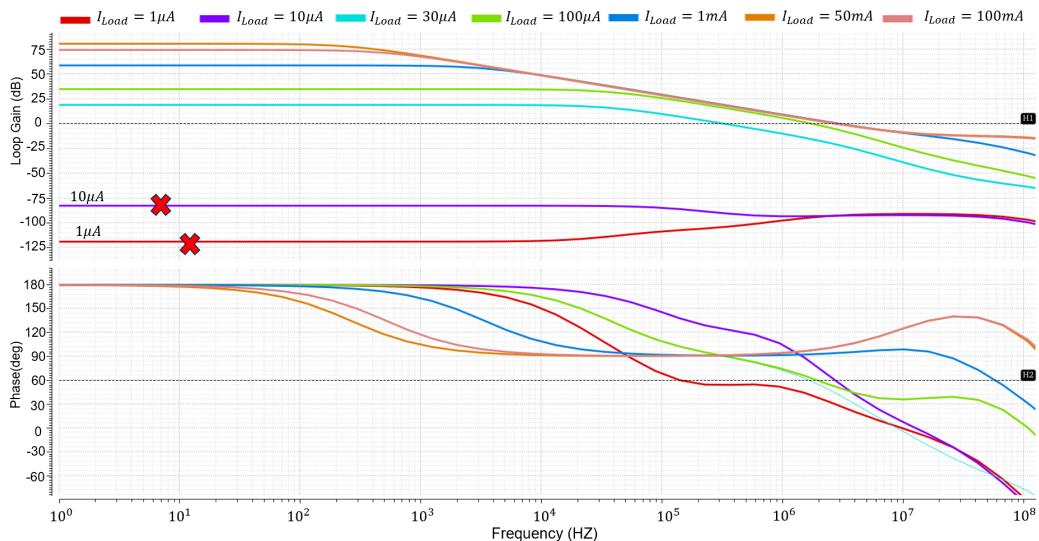
Simulation and measurement results confirm that the proposed pre-filter significantly enhances PSRR at high frequencies. Fig. 4.7 shows the loop gain and phase response, while Fig. 4.8 presents the corresponding PSRR curve.

The pre-filtering was tried to optimize the folder cascode capacitorless PMOS voltage type with poor PSRR. However, during the experiment, it was found that with a supply voltage of only 1.5V, it is difficult to achieve full saturation of 5 transistors in one branch, even with a pFET\_b/nFET\_b threshold voltage ( $V_{th}$ ) of about 350 mV- 400 mV. During further try, some transistors, such as M1, are set to work in sub-threshold

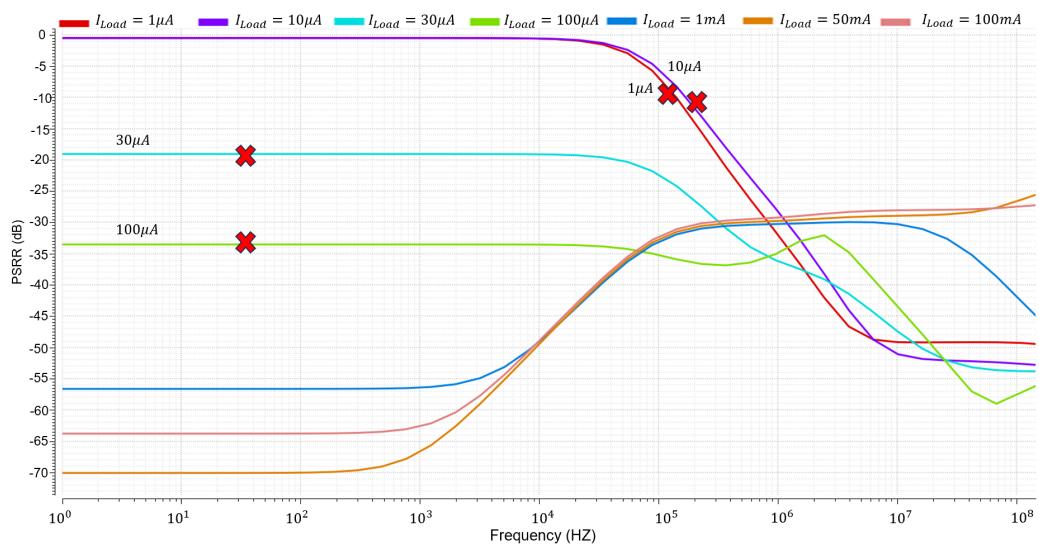
state, and it can be found that: PSRR is optimized under high frequency indeed, and the total load current stability and PSRR situation is good, but the PSRR under light load current is not improved. And the circuit is no longer in normal operation at light load (less than 30 $\mu$ A), and a stable voltage output of 0.8V cannot be realized.

Analysis of the cause of failure: less than 30 $\mu$ A load current case, due to the combined effect of the M1 voltage divider and power transistor gate voltage raised, so that the error amplifier can not work correctly, the circuit began to be out of balance. At light loads, the current in the power transistor branch is very small, and the gate voltage is raised, causing some of the transistors of the error amplifier to enter the linear region, and also pulling down the loop gain.

In addition, another disadvantage of this method is that in order to meet the load current capability to work normally in a 100mA system, M2 needs to be able to support a current of 100mA as well. The use of two transistors in series also consumes part of the voltage, and in order to reduce the on-resistance of the power transistor to ensure the normal operation of the circuit, the power transistor also needs to increase its width-to-length ratio (W/L). Therefore, this method requires a large area loss in design size.



**Figure 4.7 Loop Gain and Loop Phase**



**Figure 4.8 PSRR**



# 5 Experiments

## 5.1 Large Capacitor-based LDOs Design

Conventional LDO regulators typically rely on large off-chip capacitors, ranging from  $1 \mu\text{F}$  to  $10 \mu\text{F}$ , to ensure transient load stability and improve overall dynamic performance. These capacitors act as charge reservoirs, supplying instantaneous load current during sudden transients while the control loop adjusts the pass transistor output. To further enhance stability, the ESR of the output capacitor, or an intentionally added small series resistor, introduces an LHP zero, thereby improving the system's phase margin[23].

### 5.1.1 Principle

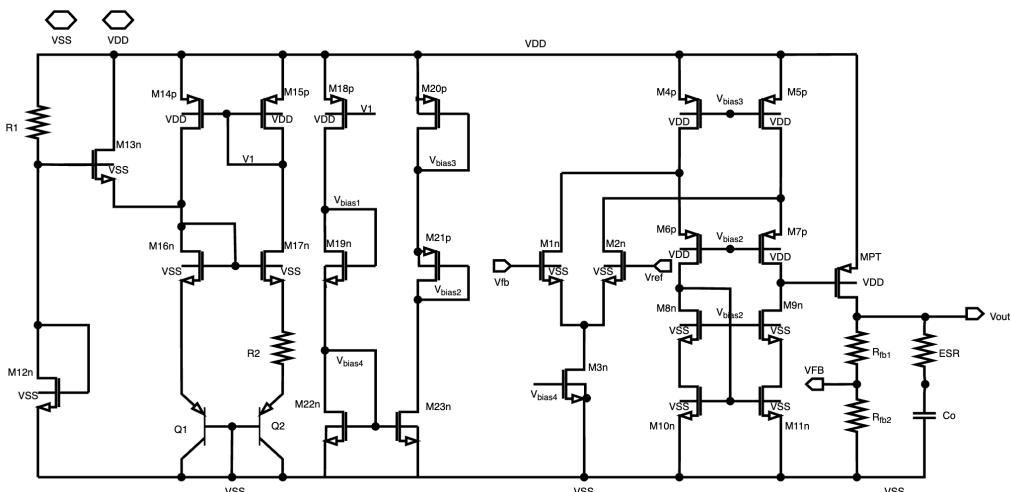
When the initial current through the pass transistor  $M_p$  is zero and the load current abruptly transitions from 0 to  $I_{\max}$ , the maximum voltage peak occurs. In this scenario, the maximum output voltage variation is approximately determined by the following equation:

$$\Delta V_{\text{out}} \approx \frac{I_{\max} \cdot \Delta t}{C_{\text{out}}} \quad (5.1)$$

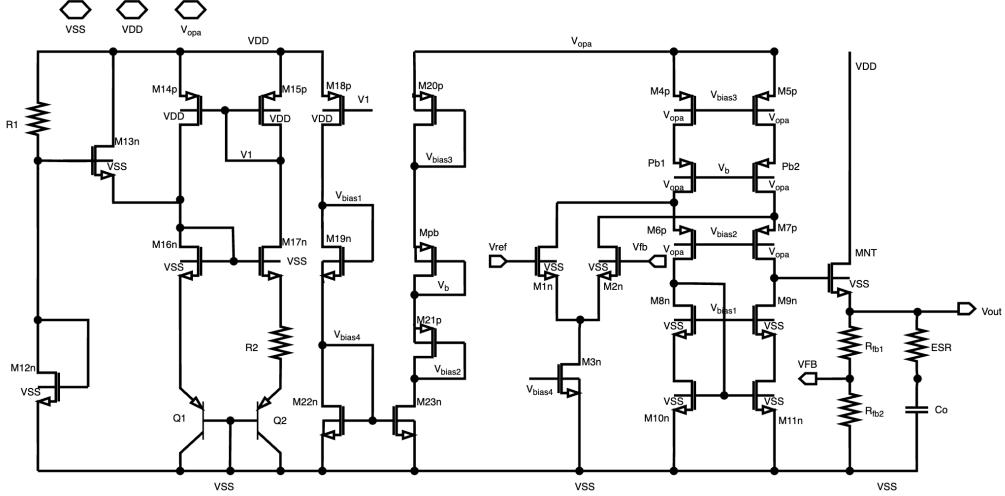
In this equation,  $t$  represents the time required for the loop to respond. Consequently, the output voltage variation is inversely proportional to the output capacitance  $C_{\text{out}}$ . By increasing  $C_{\text{out}}$ , the output voltage ripple during a given load transient can be reduced. This effect becomes more pronounced when the load transient is significantly faster than the loop's gain-bandwidth product, often resulting in peak voltages exceeding 100 mV. This expression serves as a critical reference for selecting the appropriate output capacitance.

### 5.1.2 Schematic Implementation

Figures 5.1 and 5.2 respectively show the designs of capacitor-based LDOs using PMOS and NMOS pass transistors. These designs incorporate essential building blocks such as a bandgap reference, a folded cascode error amplifier, bias generation circuitry, an off-chip output capacitor  $C_o$ , and a resistive feedback network.



**Figure 5.1** PMOS Capacitor-based LDO



**Figure 5.2** NMOS Capacitor-based LDO

The structure of the two designs is almost the same. The difference is that the NMOS case is affected by its conduction conditions; in order to ensure its normal operation, there is a need for the threshold voltage to be higher than that of the NMOS case. The output voltage of the error amplifier cannot be pulled up to close to the supply voltage (VDD) or even higher, otherwise its internal transistors are easily over-volted. In this case, it requires additional means to boost the gate voltage (e.g., charge pumps, level shifters, dual-voltage designs, etc.). In this paper, the use of a  $2V_{in}$  voltage source to achieve a dual-voltage source or analog charge pump situation to supply power to the error amplifier, to raise its output swing.

As the voltage is raised, it also brings up the issue of the transistor withstand voltage. As shown in Table 5.1 in the reference manual, first Idnfet3p3 was selected to replace the transistors found by simulation that may be out of their voltage withstand range. It was found that this type made it more difficult for the circuit to operate in a normal state due to lower mobility and usually larger channel lengths, and finally, the EGSLVT type was used as a replacement. However, the egslvt type can only withstand a maximum of  $V_{ds,max}=1.98$ , and there is still the possibility that the input transistor may be over-voltage when the error amplifier is supplied with a voltage of 3V [24]. Therefore, a set of voltage divider paths with equal currents to the current mirror load branch are added to reduce the voltage at the output node of the error amplifier to avoid the transistor's  $V_{DS}$  over the reliability limit when the charge pump is boosting the power supply. This design is applicable to all the NMOS circuit cases mentioned below.

FET	vgs_min	vgs_max	vgd_min	vgd_max	vds_min	vds_max	period
<b>SG rules</b>							
nfet	-sg_limit	sg_limit	-sg_limit	sg_limit	-sg_limit	sg_limit	1.00E-12
p fet	-sg_limit	sg_limit	-sg_limit	sg_limit	-sg_limit	sg_limit	1.00E-12
<b>LDMOS rules</b>							
Idnfet3p3	-1.98	1.98	-3.63	1.98	-1.98	3.63	1.00E-08
Idpfet3p3	-1.98	1.98	-1.98	3.63	-3.63	1.98	1.00E-08
<b>EG rules</b>							
egslvtnfet	-eg_limit	eg_limit	-eg_limit	eg_limit	-eg_limit	eg_limit	1.00E-08
egslvtpfet	-eg_limit	eg_limit	-eg_limit	eg_limit	-eg_limit	eg_limit	1.00E-08
<b>Note:</b> sg_limit = 0.9; eg_limit = 1.98; evg_limit = 1.65; egu_limit = 1.32. Defined in soa.inc(scs).							

**Table 5.1** Table 5.1: Safe Operating Area (SOA) Rules for SG, LDMOS, and EG Devices [24]

## 5.2 Capacitor-less Voltage LDOs Design

For the design of LDO regulators without external capacitors, two key challenges must be addressed: (1) **minimizing output voltage overshoot and undershoot during load transients**, and (2) **ensuring the stability of the regulation loop under varying operating conditions**. To overcome these challenges, **voltage-mode LDO** architectures commonly adopt techniques such as Miller compensation, feed-forward paths, and the strategic placement of LHP zeros, as previously discussed in Chapter III.

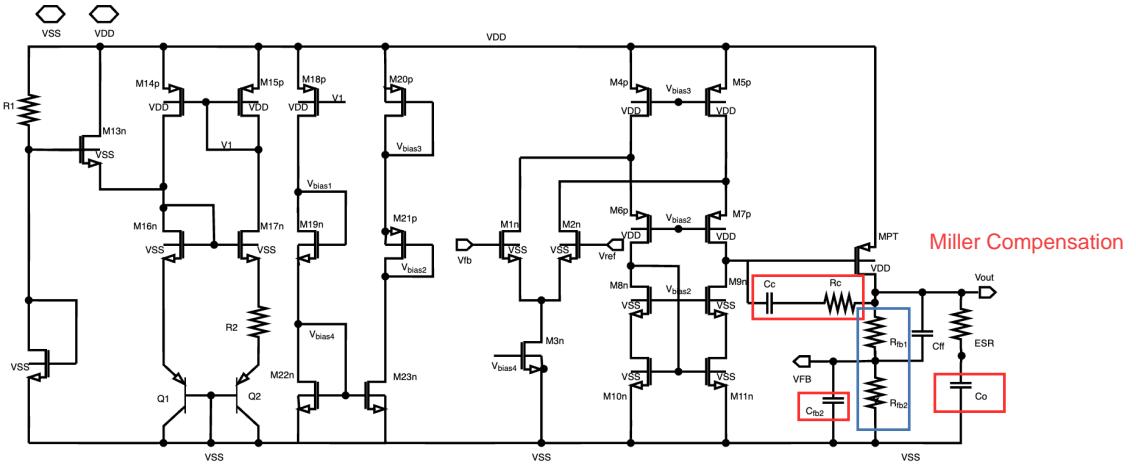


Figure 5.3 PMOS Capacitor-less LDO

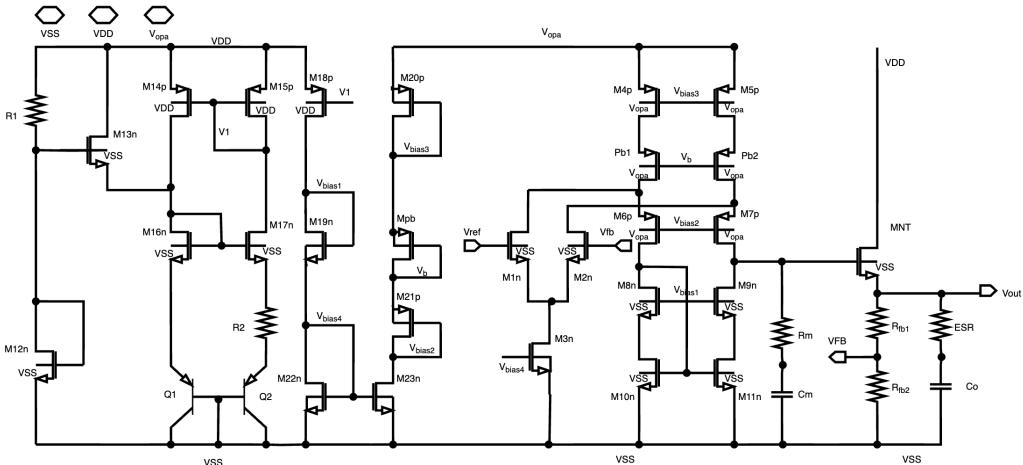


Figure 5.4 NMOS Capacitor-less LDO

Figure 5.3 and 5.4 show the full transistor-level schematic implementations of capacitor-less LDOs using both PMOS and NMOS pass transistors. These architectures are designed for full integration, utilizing an on-chip capacitor of 100 pF, eliminating the need for large off-chip output capacitors.

The upper diagram 5.3 illustrates a PMOS-based capacitor-less LDO. Similar to conventional designs, it **uses a folded cascode error amplifier for high gain** and a PMOS pass transistor  $M_{PT}$  to regulate the output. Where the DC gain varies with the current load, bringing about large variations in pole shift resulting in large fluctuations in phase margin. Most of the variation is absorbed between 0 and 1 mA load current, when the transfer transistor enters the subthreshold region where the output pole shift is very large. The LDO regulator normally becomes stable when the load current is above 1 mA. **To maintain loop stability without relying on large output capacitance**, the circuit includes advanced frequency compensation techniques. Specifically, a compensation capacitor  $C_c$  and a resistor  $R_c$  are introduced between the amplifier output

and the pass transistor gate to form a Miller compensation network. This creates a dominant low-frequency pole and introduces a left-half-plane zero that boosts phase margin. In addition, the feedback network includes a small integrated capacitor  $C_{fb}$  for local compensation. The output capacitor  $C_o$  remains on-chip, and stability is maintained through precise loop design.

The lower diagram 5.4 shows an NMOS-based counterpart. As with other NMOS designs, a boosted gate drive voltage  $V_{gss}$  is required to maintain the NMOS pass transistor  $M_{NT}$  in saturation. The error amplifier drives the gate of the pass transistor through a compensation network consisting of  $C_m$  and  $R_m$ , which again implements Miller-like compensation. This version also includes a local feedback capacitor  $C_{fb}$ , and a current-efficient biasing structure to ensure minimal quiescent current. Compared to the PMOS structure, the NMOS pass device offers lower on-resistance and faster transient response. However, the design complexity increases due to the need for gate-boosting circuitry and careful level shifting to maintain stability over varying loads and line conditions.

### 5.3 Capacitor-less LDOs without Feedback Resistors Design

In traditional LDOs, the output voltage is set by a feedback resistor, connected between the output and the error amplifier to reduce the input swing required by the error amplifier, and appropriately selected resistors are also used to set the output voltage. However, at low output voltages, the resistive divider may not be necessary at times. In this case, the error amplifier typically uses an internal fixed ratio or reference voltage to directly compare the output voltages without relying on external passive components. This simplification significantly reduces layout complexity and leakage paths.

Capacitor-less LDOs without feedback resistors represent a highly integrated voltage regulation solution tailored for modern SoC and portable applications, where area, power, and stability constraints are critical. Unlike traditional LDOs that rely on large off-chip output capacitors and a resistive feedback network to regulate output voltage, these designs eliminate both, resulting in reduced silicon area and improved integration compatibility. Figure 5.5 and 5.6 show two implementations of capacitor-less LDOs, one with a PMOS pass device and the other with an NMOS pass device, both operating without a conventional resistive feedback divider. This modification reflects a design trend toward fully integrated, ultra-low-power systems, where minimizing static current consumption is a primary goal.

Overall, removing the resistive feedback network offers significant benefits in power efficiency and area savings, at the cost of increased sensitivity to process variations and reduced programmability. These designs are particularly attractive for fixed-output, always-on power domains in advanced SoCs.

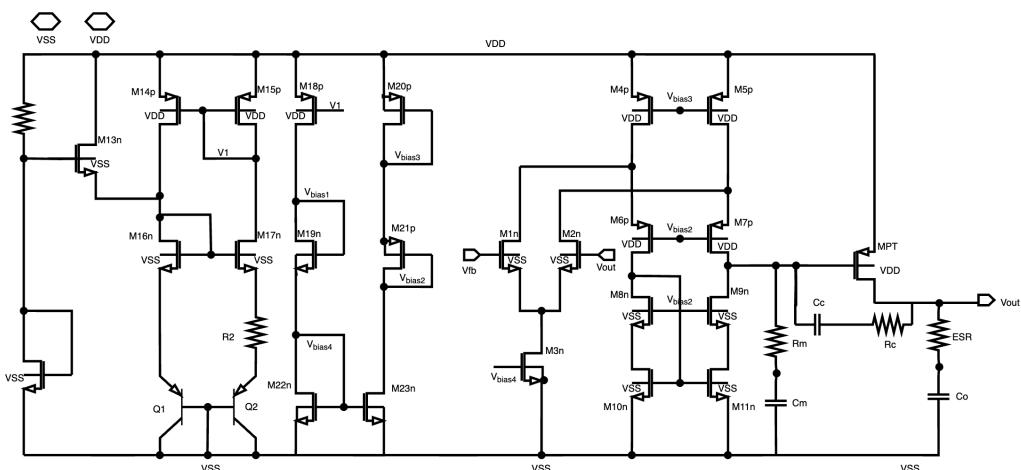
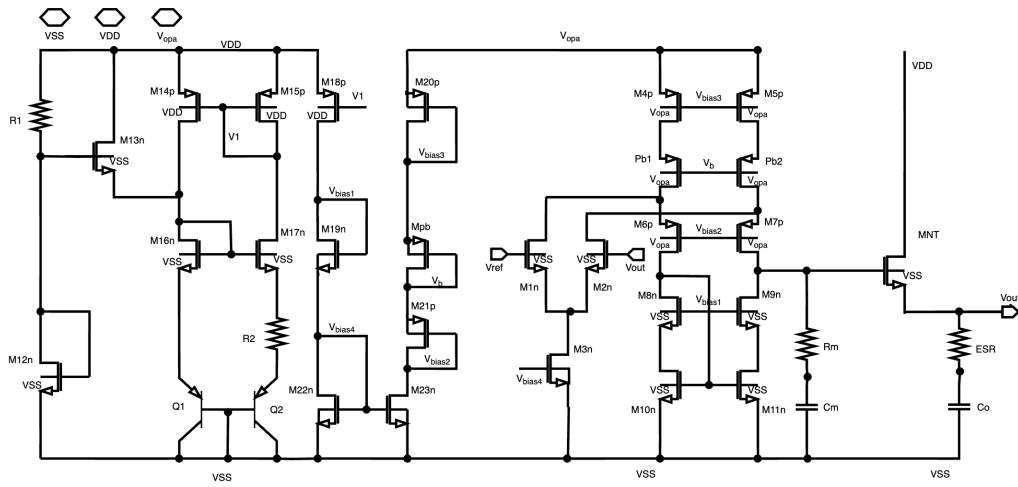


Figure 5.5 PMOS Capacitor-less LDO without Feedback Resistors



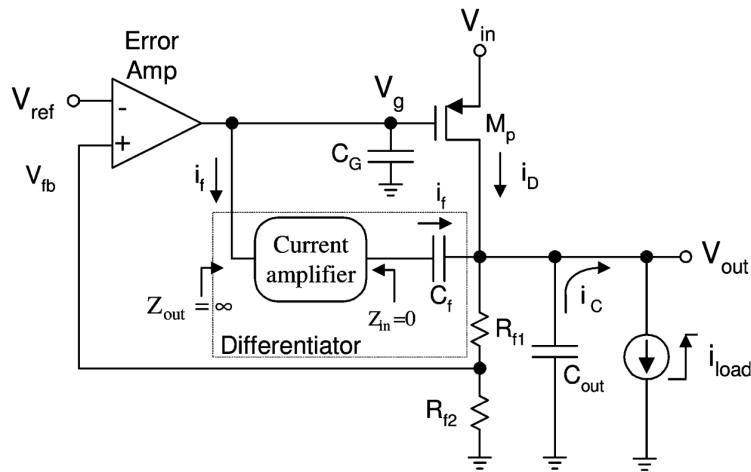
**Figure 5.6** NMOS Capacitor-less LDO without Feedback Resistors

## 5.4 Current-Mode LDOs Design

The Current-Mode LDO (CM-LDO) breaks through the single-loop regulation of traditional voltage-mode LDOs and reorganizes the control system by introducing a voltage-current dual-feedback topology (Figure 5.7). Its core innovation is to incorporate the load current dynamic parameters into the closed-loop regulation.

### 5.4.1 Block Diagram

Figure 5.7 illustrates the architecture of a current-mode LDO, which differs fundamentally from traditional voltage-mode counterparts. Instead of relying solely on voltage feedback, this design introduces a current feedback path that actively senses and responds to load current variations, thereby significantly enhancing transient response.



**Figure 5.7** Current Mode LDO [4]

In this architecture, a key feature is the inclusion of a differentiator block composed of a capacitor  $C_f$  and a high-gain current amplifier. The differentiator senses the dynamic current  $i_f$  flowing through the output node and provides rapid feedback to the error amplifier. The input impedance of the differentiator is ideally zero ( $Z_{in} = 0$ ), ensuring that all high-frequency load current perturbations are accurately sensed, while the output impedance is ideally infinite ( $Z_{out} = \infty$ ) to isolate the control loop.



This current-mode feedback loop acts in parallel with the conventional voltage-mode path, enabling faster regulation of output voltage  $V_{out}$  during sudden load steps. In particular, the differentiator circuit improves the system's slew rate and reduces output overshoot or undershoot. The output capacitor  $C_{out}$  and its ESR form part of the compensation network. Since the current-mode feedback accelerates dynamic adjustment, the overall design can tolerate smaller output capacitance without compromising stability or transient performance.

### Dual Loop Cooperative Mode

The current-mode LDO adopts a dual-loop feedback structure that leverages the complementary advantages of both voltage and current regulation. The outer voltage loop maintains steady-state accuracy by continuously comparing the output voltage with a stable reference  $V_{ref}$ . This loop is primarily responsible for determining the long-term DC operating point of the regulator.

Concurrently, the inner current loop monitors instantaneous variations in the pass transistor or load current through real-time current sensing circuits, such as current mirrors, low-ohmic sensing resistors, or sensing capacitors. These current signals are processed by a transconductance amplifier to generate fast compensation responses. Operating in a feed-forward manner, this loop preemptively corrects disturbances before they propagate through the slower voltage control path.

### Dynamic Disturbance Suppression

The dual-loop system achieves fast transient response through a division of control effort in the time domain. The current loop is optimized for microsecond-scale disturbance suppression, allowing it to promptly counter sudden load changes and prevent large output deviations. Meanwhile, the voltage loop ensures long-term voltage regulation and output accuracy under steady-state and slowly varying conditions.

By decoupling fast dynamic correction from steady-state control, this hierarchical regulation approach significantly mitigates the need for large output capacitance. As a result, the system supports fully integrated, capacitor-less implementations, making it particularly attractive for compact, low-power SoC and analog-mixed-signal platforms.

#### 5.4.2 Circuit Design

As shown in Figure 5.8 and 5.9, a current feedback path is added to the previous folder cascode voltage mode, and a low quiescent current design combining a simple transconductance opamp form is also realized. Both circuits are implemented in the same way, using the key component sense capacitor  $C_{f1}$  and controlling the MOSFET turn-on and turn-off to create the current charging and discharging path:

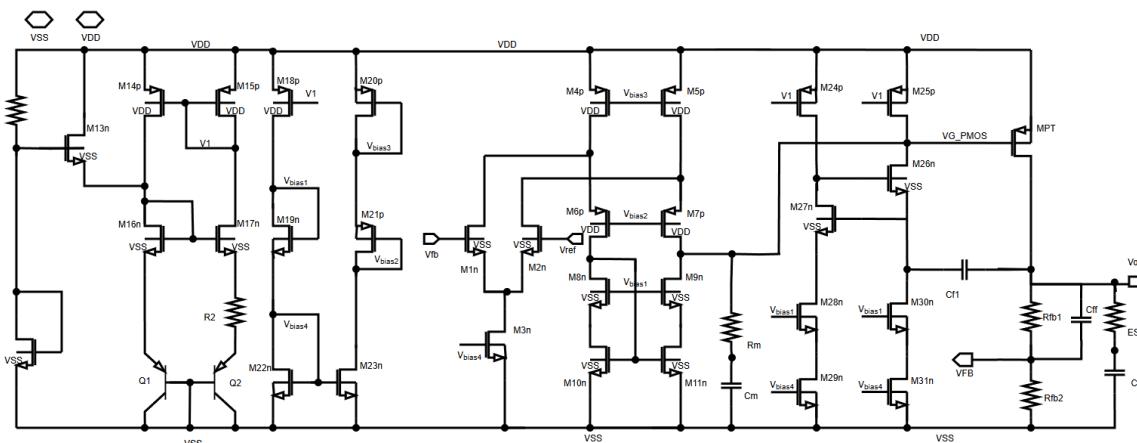
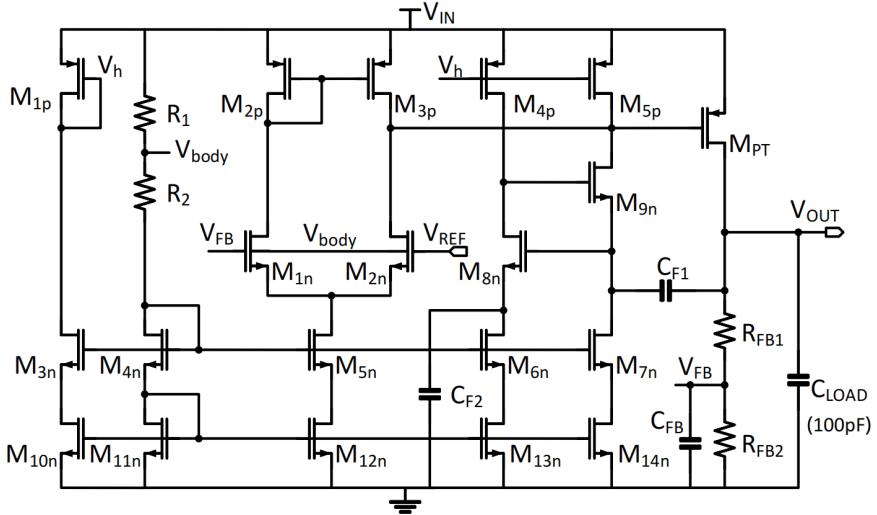


Figure 5.8 PMOS Folder-cascode CM-LDO



**Figure 5.9** Low Quiescent CM-LDO

In the transient enhancement path, transistor  $M_{9n}/M_{26n}$  plays a critical role. When a sudden load current increase occurs (e.g., 0 to  $I_{MAX}$ ), its high transconductance  $g_m$  rapidly discharges the gate node of the pass transistor through a low-impedance path. This mechanism accelerates the pass device's turn-on behavior and minimizes output voltage droop.

Meanwhile, transistor  $M_{8n}/M_{27n}$  acts as a controlled switch. During load surges, it is turned off to avoid interfering with the discharge process of  $M_{9n}/M_{26n}$ . Under normal or falling load conditions,  $M_{8n}/M_{27n}$  participates in regulating the gate charging path, thereby enabling stable voltage control.

### 5.4.3 Performance Analysis

Simulation and measurement results demonstrate that the proposed CM-LDO architecture outperforms traditional voltage-mode designs in several key areas:

**1. Transient Response:** During abrupt load step events (e.g.,  $10 \mu\text{A} \rightarrow 100 \text{ mA}$ ), the CM-LDO significantly reduces output voltage overshoot and undershoot. Additionally, the recovery time is notably shortened. This improvement stems from the proactive behavior of the current feedback loop, which adjusts the gate of the pass device in real time before a large voltage deviation occurs.

**2. Loop Stability:** The current-mode loop introduces a nonlinear damping effect that enhances the regulator's open-loop phase margin. Furthermore, the use of compensation techniques introduces an LHP zero, further boosting stability and suppressing high-frequency peaking.

**3. Integration and Area Efficiency:** By relying on fast current feedback rather than large output capacitors, the CM-LDO greatly reduces its dependence on external capacitance. This enables full on-chip integration, reducing overall silicon area and making it highly suitable for SoC applications.

## 5.5 Simulation Results Analysis and Performance Comparison

### 5.5.1 Dropout Voltage and Input Voltage Analysis

Table 5.2 presents the comparison of dropout voltage  $V_{dropout}$  and minimum input voltage  $V_{in,min}$  for various LDO configurations under different load conditions, including both PMOS- and NMOS-based architectures. These results highlight the trade-offs between external-capacitor and capacitor-less implementations, as well as voltage-mode versus current-mode control strategies.

Due to the higher mobility of carriers in NMOS than in PMOS, the dropout voltage of NMOS LDOs is significantly lower than that of PMOS architectures. Higher carrier mobility allows NMOS to obtain lower

on-resistance ( $R_{on}$ ) under the same process, and its dropout voltage can be approximated as  $V_{\text{Dropout}} = I_{\text{Load}} \times R_{on}$ , usually NMOS dropout voltage is reduced by about 60% to 70% under the same current load, especially suitable for low-power situations where the difference between the input and output voltages is very small. As shown in the simulation results (Table 5.2), the NMOS LDO dropout is smaller than that of PMOS LDO, and it is found that the circuit with no feedback resistor has the smallest dropout, which can be as small as 192.95 mV among the eight designs, and as shown in Fig. With the increase of  $V_{in}$  from 0–1.5 V, all circuits have the smallest  $V_{in}$  for the normal operation as the  $I_{\text{Load}}$  increases.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
$V_{\text{dropout}}$ [mV]	352.03	385.24	226.47	317.66	577.49
$V_{in, min}$ [mV] $I_{\text{Load}} = 1 \mu A$	810	810	810	810	800.94
$V_{in, min}$ [mV] $I_{\text{Load}} = 10 \mu A$	810	810	840	810	810
$V_{in, min}$ [V] $I_{\text{Load}} = 100 \text{ mA}$	1.11	1.14	1.02	1.11	1.37

(a)  $V_{\text{Dropout}}$  and  $V_{in, min}$  Comparison (PMOS)

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
$V_{\text{dropout}}$ [mV]	200.81	213.98	192.95
$V_{in, min}$ [mV] $I_{\text{Load}} = 1 \mu A$	810	810	810
$V_{in, min}$ [mV] $I_{\text{Load}} = 10 \mu A$	810	810	810
$V_{in, min}$ [mV] $I_{\text{Load}} = 100 \text{ mA}$	997.56	990	990

(b)  $V_{\text{Dropout}}$  and  $V_{in, min}$  Comparison (NMOS)

**Table 5.2** Dropout voltage and Minimum Input Voltage Comparison

For PMOS-based architectures, as shown in Table 5.2 (a), the dropout voltage varies significantly across the designs. The conventional LDO with a large external capacitor ( $C = 2.5 \mu F$ ) exhibits a dropout of 352.03 mV. The capacitor-less voltage-mode version without feedback resistors further reduces this to 226.47 mV. Among the current-mode designs, the standard version achieves 317.66 mV dropout, whereas the low-quiescent-current variant reaches the highest dropout voltage of 577.49 mV. This increase is attributed to the limited gate drive strength and slower response speed due to bias current constraints.

In terms of minimum input voltage, the differences are negligible at light loads ( $1\text{--}10 \mu A$ ), where all designs maintain  $V_{in, min} = 810 \text{ mV}$ . However, under a heavy load of 100 mA, the voltage-mode designs exhibit better performance with input requirements around 1.02–1.14 V. In contrast, the low- $I_Q$  current-mode LDO requires a higher minimum input of 1.37 V, primarily due to degraded transient performance and slower gate adjustment.

For NMOS-based implementations, as presented in Table 5.2 (b), the dropout voltage is consistently lower than in PMOS designs. The best performance is achieved by the capacitor-less voltage-mode design without resistive feedback, with a minimum dropout of 192.95 mV. This reflects the inherently lower on-resistance of NMOS transistors and the efficiency of their gate drive when sufficient  $V_{\text{boost}}$  is available.

The minimum input voltage for all NMOS variants remains constant at 810 mV for low-load conditions, and only slightly increases to around 990–997 mV at full load. Compared to PMOS counterparts, this demonstrates the superior conduction efficiency and low-dropout capability of NMOS LDOs under high-current conditions.

Overall, the results confirm several important trends. Capacitor-less LDOs are viable for full integration without sacrificing light-load input performance, though care must be taken to preserve efficiency at higher load currents. Current-mode architectures provide enhanced transient control but may incur higher dropout if designed for ultra-low quiescent current. NMOS pass devices consistently offer lower dropout and improved input voltage margins, making them highly suitable for high-performance and energy-sensitive applications, provided that boosted gate drive voltage is available.

### 5.5.2 Loop Stability Comparison

In this application, the phase margin of the system loop must be sufficient to provide a stable output voltage, and for stability, it is usually required that the phase margin over the full load range is at least 45 (above 60 is usually expected). Tables 5.3 and 5.4 show the simulated loop gain and phase margin of the proposed LDO in the global loop under different load conditions. To simulate the loop gain, the global loop is disconnected at  $V_{fb}$ . The overall results are slightly affected by the load current. Where  $f_c$  is the Gain Crossover Frequency.

Among them, the NMOS case is easier than PMOS to achieve stability. NMOS-based designs demonstrate consistently high gain and bandwidth across all load conditions. No off-chip capacitance voltage mode PMOS (using only Miller compensation, feed-forward compensation, etc.) in the case of light load due to the load current is too small power tube operating in the sub-threshold region, and the gate of the PMOS directly affects the error amplifier's output voltage, resulting in the point of over-high part of the amplifier in the MOSFETs into the linear region, pulling down the gain and so on.

For PMOS-based designs, the capacitor-less current-mode architecture provides superior transient stability. At 100 mA load, the current-mode version achieves a phase margin of 116.1° and a crossover frequency of 5.52 MHz, indicating robust high-frequency control. In contrast, the low- $I_Q$  variant maintains acceptable phase margin of 64.37° but sacrifices bandwidth and speed. This trade-off highlights the balance between low-power operation and transient performance.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
<i>I<sub>Load</sub> = 1 μA</i>					
Loop Gain [dB]	47.79	26.17	60.48	61.23	71.95
Phase Margin $f_c$	90.06 249.61 kHz	81.33 88 kHz	63.57 227.26 kHz	70.78 489.59 kHz	72.21 68.86 kHz
<i>I<sub>Load</sub> = 10 μA</i>					
Loop Gain [dB]	66.70	42.85	70.56	68.45	77.41
Phase Margin $f_c$	90.24 2.26 MHz	41.31 1.07 MHz	67.24 2.95 MHz	62.65 2.65 MHz	84.74 64.43 kHz
<i>I<sub>Load</sub> = 50 mA</i>					
Loop Gain [dB]	110.28	95.01	76.00	98.01	75.82
Phase Margin $f_c$	85.58 1.83 MHz	157 9.95 MHz	90.41 50.73 MHz	97.62 35.10 MHz	64.08 65.98 kHz
<i>I<sub>Load</sub> = 100 mA</i>					
Loop Gain [dB]	88.61	78.85	86.09	92.06	68.40
Phase Margin $f_c$	86.74 2.43 MHz	155 7.58 MHz	90.62 67.41 MHz	116.1 5.52 MHz	64.37 70.33 kHz

Table 5.3 Loop Gain, Phase Margin, and Crossover Frequency Comparison (PMOS)

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
$I_{Load} = 1 \mu A$			
Loop Gain [dB]	103.50	103.80	106.74
Phase Margin $f_c$	60.26 15.73 kHz	58.39 481.552 kHz	69.49 1.18785 MHz
$I_{Load} = 10 \mu A$			
Loop Gain [dB]	103.99	103.96	106.8
Phase Margin $f_c$	84.41 88.00 kHz	81.69 2.43 MHz	61.32 5.44 MHz
$I_{Load} = 50 mA$			
Loop Gain [dB]	102.40	102.37	105.01
Phase Margin $f_c$	69.74 29.79 MHz	69.84 48.56 MHz	86.21 67.41 MHz
$I_{Load} = 100 mA$			
Loop Gain [dB]	100.04	100.27	102.58
Phase Margin $f_c$	69.64 30.48 MHz	71.48 41.95 MHz	86.63 67.41 MHz

**Table 5.4** Loop Gain, Phase Margin, and Crossover Frequency comparison (NMOS)

### 5.5.3 Power Supply Rejection Ratio Comparison

The PSRRs of the designed circuits are shown in Table 5.5 and 5.6. It can be seen that the PSRR of the LDO is better at low frequencies and decreases with a gradual increase in AC frequency. The PSRR rises to nearly 0 dB at high frequencies and no longer rejection of ripple. The PSRR needs to be improved for both the low quiescent current-mode PMOS design and the voltage-type PMOS capacitorless design. And the low-frequency PSRR results of the voltage-type PMOS capacitorless design are not very good at low frequencies due to its lack of system gain. In addition, the current-type performs better than the voltage-type at medium and high frequencies.

For PMOS-based LDOs in Table 5.5, the use of an external capacitor ( $C = 2.5 \mu F$ ) provides the highest PSRR across all frequencies and load conditions, with performance reaching  $-105.2$  dB at  $10$  kHz and light load. In contrast, capacitor-less voltage-mode designs show significant PSRR degradation, particularly at higher frequencies, where the absence of a large output capacitor limits the ability to filter high-frequency ripple.

$I_{Load}$	Frequency	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$
$1 \mu A$	1 Hz	-68.3 dB	-27.7 dB	-55.2 dB	-54.1 dB	-70.8 dB
	10 kHz	-105.2 dB	-27.3 dB	-41.2 dB	-45.3 dB	-31.3 dB
	1 MHz	-101.3 dB	-19.2 dB	-29.1 dB	-24.5 dB	-16.4 dB
$10 \mu A$	1 Hz	-69.6 dB	-42.2 dB	-67.2 dB	-56.1 dB	-71.3 dB
	10 kHz	-81.2 dB	-41.2 dB	-43.8 dB	-45.3 dB	-31.2 dB
	1 MHz	-85.3 dB	-6.4 dB	-19.4 dB	-18.8 dB	-2.6 dB
$50 mA$	1 Hz	-79.6 dB	-81.1 dB	-71.5 dB	-63.4 dB	-63.4 dB
	10 kHz	-72.6 dB	-49.4 dB	-43.8 dB	-43.0 dB	-17.2 dB
	1 MHz	-34.1 dB	-11.1 dB	-20.0 dB	-14.8 dB	186.2 mdB
$100 mA$	1 Hz	-61.3 dB	-63.6 dB	-75.1 dB	-61.4 dB	-48.1 dB
	10 kHz	-61.0 dB	-48.9 dB	-43.8 dB	-40.5 dB	-17.1 dB
	1 MHz	-33.1 dB	-10.8 dB	-19.9 dB	-10.1 dB	187.7 mdB

**Table 5.5** PSRR Comparison of PMOS-based

$I_{Load}$	Frequency	External Capacitor $C = 2.5 \mu F$	Cap-less $C = 100 pF$ Voltage-type	Cap-less $C = 100 pF$ Voltage-type No $R_{fb1}, R_{fb2}$
$1 \mu A$	1 Hz	-135.3 dB	-135.3 dB	-133.9 dB
	10 kHz	-81.3 dB	-76.6 dB	-78.6 dB
	1 MHz	-80.1 dB	-48.5 dB	-44.6 dB
$10 \mu A$	1 Hz	-136.9 dB	-136.9 dB	-131.7 dB
	10 kHz	-82.9 dB	-76.6 dB	-78.6 dB
	1 MHz	-63.3 dB	-42.2 dB	-44.3 dB
50 mA	1 Hz	-119.2 dB	-119.2 dB	-117.3 dB
	10 kHz	-81.7 dB	-76.1 dB	-78.1 dB
	1 MHz	-42.1 dB	-41.8 dB	-43.4 dB
100 mA	1 Hz	-110.3 dB	-110.3 dB	-110.8 dB
	10 kHz	-80.0 dB	-72.4 dB	-75.6 dB
	1 MHz	-40.5 dB	-40.0 dB	-42.3 dB

**Table 5.6** PSRR Comparison of NMOS-based

Interestingly, the cap-less current-mode architecture achieves better high-frequency PSRR than voltage-mode designs due to its faster gate regulation enabled by the current loop. For instance, at  $I_{Load} = 1 \mu A$ , the current-type LDO reaches  $-24.5$  dB at 1 MHz, outperforming the voltage-mode counterpart at  $-19.2$  dB. However, the low-quiescent-current current-mode design experiences substantial degradation, especially under heavy loads.

NMOS-based designs in Table 5.6 consistently demonstrate superior PSRR performance over PMOS implementations, especially at high frequencies. This improvement stems from the higher transconductance of NMOS pass devices and the stronger gate drive enabled by the boosted supply  $V_{boost}$ .

These results highlight several key insights. First, external capacitors remain essential for achieving optimal PSRR, particularly in PMOS designs. Second, current-mode control offers improved high-frequency PSRR in capacitor-less configurations.

### 5.5.4 Load Regulation and Line Regulation Comparison

#### Load Regulation

The LDO output voltage depends on the load current and input voltage. The load regulation represents the ability of  $V_{out}$  of the LDO system to reject changes in  $I_{Load}$ , and the experimental results are shown in Table 5.7.

As shown in Table 5.7 (a), the PMOS LDO with an external capacitor achieves the best performance, with a load regulation of  $13.59 \text{ mV/A}$  under a  $1 \mu A$  to  $100 \text{ mA}$  load step, and  $6.89 \text{ mV/A}$  under a  $10 \mu A$  to  $100 \text{ mA}$  transition. The large output capacitor enables energy buffering during sudden load transitions, effectively suppressing output voltage deviation. Among the capacitor-less designs, the current-mode architecture exhibits significant improvements compared to voltage-mode types. Specifically, the current-mode CM-LDO achieves  $41.39 \text{ mV/A}$  regulation under full load swing, far outperforming the cap-less voltage-mode design ( $309.26 \text{ mV/A}$ ), which suffers due to the lack of a feedback-assisted dynamic path. The design without feedback resistors further improves regulation to  $67.55 \text{ mV/A}$ . The low- $I_Q$  current-mode design maintains decent regulation ( $39.91 \text{ mV/A}$ ) despite its lower power consumption. The NMOS-based designs demonstrate excellent load regulation, as shown in Table 5.7 (b). All implementations achieve sub- $40 \mu \text{V/A}$  regulation across both load conditions.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
$1 \mu A \rightarrow 100 \text{ mA}$	13.59	309.26	67.55	41.39	39.91
$10 \mu A \rightarrow 100 \text{ mA}$	6.89	77.68	35.56	27.67	35.45

(a) Load regulation of PMOS-based LDOs in mV/A

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
$1 \mu A \rightarrow 100 \text{ mA}$	37.99	37.42	28.83
$10 \mu A \rightarrow 100 \text{ mA}$	34.84	34.83	25.62

(b) Load regulation of NMOS-based LDOs in  $\mu V/A$

Table 5.7 Load regulation comparison of PMOS-based (a) and NMOS-based (b) LDOs.

## Line Regulation

The linear regulation represents the rejection ability of  $V_{out}$  of the LDO system for the change of  $V_{in}$ , and the experimental results are shown in Table 5.8. The different power transistors have some influence on the line regulation rate. For example, from the small-signal circuit in Fig. 5.10, the line regulation results of PMOS/NMOS type LDO are deduced as follows [16]:

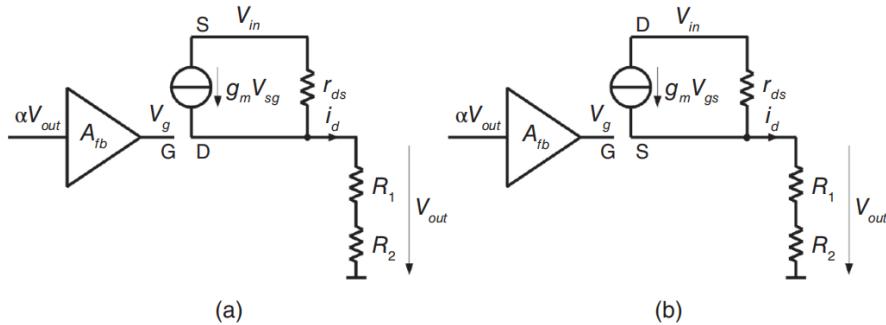


Figure 5.10 Small-signal Equivalent Circuits of PMOS- and NMOS-LDOs

PMOS type LDO:

$$\left| \frac{\Delta V_{out}}{\Delta V_{in}} \right| \approx \left| \frac{v_{out}}{v_{in}} \right|_{i_{load}=0} = \frac{g_m(R_1 + R_2)}{1 + g_m(R_1 + R_2)\alpha A_{fb}} \approx \frac{1}{\alpha A_{fb}}. \quad (5.2)$$

NMOS type LDO:

$$\left| \frac{\Delta V_{out}}{\Delta V_{in}} \right| \approx \left| \frac{v_{out}}{v_{in}} \right| = \frac{(R_1 + R_2)/r_{ds}}{1 + (R_1 + R_2)g_m(1 + \alpha A_{fb})} \approx \frac{1}{g_m r_{ds} \alpha A_{fb}}. \quad (5.3)$$

For PMOS designs, as shown in Table 5.8 (a), the external capacitor version delivers the best overall performance under light loads. At  $1 \mu A$  and  $10 \mu A$ , the line regulation values are  $1.87 \text{ mV/V}$  and  $0.92 \text{ mV/V}$ , respectively, demonstrating strong rejection of input voltage fluctuations. However, under heavy load ( $100 \text{ mA}$ ), performance deteriorates, reaching  $107.67 \text{ mV/V}$  due to the limited dynamic response speed of the PMOS pass device.

Among the capacitor-less designs, the voltage-mode LDO suffers from significant degradation under all load conditions, especially at light load where the absence of a large output capacitor leads to poor suppression of line disturbances (e.g., 39.50 mV/V at 1  $\mu$ A). In contrast, the current-mode architecture shows marked improvement, achieving 7.92 mV/V and 6.17 mV/V at light loads and 19.38 mV/V at 100 mA. These results demonstrate the effectiveness of current feedback in compensating for input perturbations, even without external capacitance. The low-quiescent-current version performs reasonably well at light loads (4.71 mV/V at 1  $\mu$ A), but suffers under heavier loads due to insufficient bias current, leading to a rise in line regulation to 77.89 mV/V.

NMOS designs, as shown in Table 5.8 (b), deliver superior line regulation across all test conditions. Even at 100 mA, performance remains excellent, with values ranging from 5.78 mV/V to 7.42 mV/V. The best result is seen in the capacitor-less voltage-mode LDO without feedback resistors, which achieves 5.78 mV/V line regulation under full load. From both the experimental results and the above equations, LDOs with NMOS power transistors show significantly better linear regulation than PMOS types.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
1 $\mu$ A	1.87	39.50	9.62	7.92	4.71
10 $\mu$ A	0.92	10.19	12.78	6.17	1.99
100 mA	107.67	125.45	12.65	19.38	77.89

(a) Line Regulation of PMOS-based LDOs (mV/V)

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
1 $\mu$ A	0.13	0.13	0.09
10 $\mu$ A	0.25	0.25	0.21
100 mA	6.46	7.42	5.78

(b) Line Regulation of NMOS-based LDOs (mV/V)

Table 5.8 Line Regulation Comparison of PMOS-based (a) and NMOS-based (b) LDOs.

### 5.5.5 Transient Response Comparison

#### Input Voltage Transient Response

The line transient response of the output voltage to the input voltage is shown in Table 5.9. The input voltage was applied with a step of 200 mV from 1.5 V to 1.7 V and 1  $\mu$ s rising/falling edge at a current load of 100 mA.

As shown in Table 5.9 (a), the PMOS LDO with external capacitor demonstrates excellent transient performance. The transient response slows down significantly when a large capacitor is removed. The response performance of the low quiescent current current mode LDO is reduced, and there is a large output voltage undershoot swing when  $V_{in}$  changes from 1.7V to 1.5V. NMOS-based designs in Table 5.9 (b) show superior transient response compared to their PMOS counterparts across all configurations. Even in capacitor-less versions, NMOS LDOs maintain better control than PMOS counterparts. The worst-case overshoot in NMOS designs is 0.44 mV, and the undershoot is 0.54 mV.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
$I_{Load} = 100 \text{ mA}, V_{in}(1.5 \sim 1.7) \text{ V}, T_{edge} = 1 \mu s$					
Overshoot Voltage $\Delta V_{out}$ [mV]	0.77	11.11	12.35	15.56	47.24
Overshoot settling time $\Delta t [\mu s]$	2.29	1.54	5.58	4.43	5.9
Undershoot Voltage $\Delta V_{out}$ [mV]	0.78	11.43	13.17	14.15	191.10
Undershoot settling time $\Delta t [\mu s]$	4.66	1.50	4.46	4.63	15

(a) Transient response of PMOS-based LDOs at  $I_{Load} = 100 \text{ mA}$

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
$I_{Load} = 100 \text{ mA}, V_{in}(1.5 \sim 1.7) \text{ V}, T_{edge} = 1 \mu s$			
Overshoot Voltage $\Delta V_{out}$ [mV]	0.24	0.44	0.29
Overshoot settling time $\Delta t [\mu s]$	1.09	2.89	9.34
Undershoot Voltage $\Delta V_{out}$ [mV]	0.25	0.54	0.34
Undershoot settling time $\Delta t [\mu s]$	1.14	5.33	8.27

(b) Transient response of NMOS-based LDOs at  $I_{Load} = 100 \text{ mA}$

**Table 5.9** Comparison of Input Voltage Transient Response in PMOS-based (a) and NMOS-based (b) LDOs.

## Load Current Transient Response

Figure 5.10 provides the simulated transient response for load current steps from  $10 \mu A$  to  $100 \text{ mA}$  at  $1 \mu s$  rising/falling edge. The results for the current type capacitorless PMOS are relatively good, with both the undershoot and overshoot cases stabilizing the voltage within  $4 \mu s$  without significant voltage ripple. For the low quiescent current case, the results are poor due to the sub-threshold design that prevents the circuit from adjusting and suppressing the ripple as fast as the load current rises/falls in a  $1 \mu s$  step. Also NMOS presents better output voltage fluctuation rejection than PMOS due to its higher stability.

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$	Cap-less Current-type $C = 100 pF$	Cap-less Current-type Low- $I_Q$ $C = 100 pF$
$10 \mu A \sim 100 \text{ mA}, T_{edge} = 1 \mu s$					
Undershoot Voltage $\Delta V_{out}$ [mV]	12.49	128.54	108.12	139.21	438.34
Undershoot settling time $\Delta t [\mu s]$	2.20	1.39	4.78	3.80	19.92
Overshoot Voltage $\Delta V_{out}$ [mV]	6.34	221.67	92.77	117.76	682.02
Overshoot settling time $\Delta t [\mu s]$	686.288	5.25	4.52	3.74	17.73

(a) Load Transient Response of PMOS-based LDOs ( $10 \mu A$  to  $100 \text{ mA}$ )

Spec	External Capacitor $C = 2.5 \mu F$	Cap-less Voltage-type $C = 100 pF$	Cap-less Voltage-type No $R_{fb1}, R_{fb2}$ $C = 100 pF$
$10 \mu A \sim 100 \text{ mA}, T_{edge} = 1 \mu s$			
Undershoot Voltage $\Delta V_{out}$ [mV]	20.70	74.78	60.16
Undershoot settling time $\Delta t [\mu s]$	1.05	2.80	7.58
Overshoot Voltage $\Delta V_{out}$ [mV]	8.44	70.99	44.1376
Overshoot settling time $\Delta t [\mu s]$	2.10	2.89	8.32

(b) Load Transient Response of NMOS-based LDOs ( $10 \mu A$  to  $100 \text{ mA}$ )

**Table 5.10** Comparison of Load Current Transient Response in PMOS-based (a) and NMOS-based (b) LDOs

As shown in Table 5.10 (a), the PMOS LDO with external capacitor exhibits relatively moderate undershoot (12.49 mV) and overshoot (6.34 mV), but suffers from long overshoot settling time (686.29  $\mu$ s), due to energy exchange between the large capacitor and the output node. Capacitor-less voltage-mode designs display excessive overshoot and undershoot. For instance, overshoot reaches up to 221.67 mV and undershoot up to 128.54 mV. While the removal of resistive feedback improves performance somewhat, both current-mode and low- $I_Q$  current-mode versions still exhibit significant voltage excursions, particularly in the latter case, where overshoot spikes to 682.02 mV and undershoot reaches 438.34 mV. The prolonged recovery time of 17.73  $\mu$ s in the low- $I_Q$  version requires further optimization of the circuit structure.

NMOS designs demonstrate superior transient handling, as shown in Table 5.10 (b). In comparison, the fluctuation values of output voltage overshoot and undershoot caused by load changes are less than 75 mV.

### 5.5.6 Chapter Summary

This chapter mainly describes the detailed implementation of each circuit type with the discussion of simulation results. Among them, the quiescent current directly reflects the power consumption of the circuit, and the average of the above circuit design is around 41  $\mu$ A, except for the low quiescent current-current PMOS which is 1.57  $\mu$ A. From the experimental simulation data, it can also be seen that the NMOS type has better Dropout Voltage, line regulation rate, stability and so on. The current type is better than the voltage type in terms of load transient response, and the current detection loop also helps the system gain, stability and PSRR when pulling down the gate voltage of the power transistor.



# 6 Conclusion and Outlook

For the development of SoC systems-on-chip in recent years, capacitorless LDOs have become the current development trend. An integrated capacitorless linear voltage regulator was explored, designed, implemented, simulated and discussed in this thesis. A summary and an outlook for further improvements are discussed in this chapter.

## 6.1 Conclusion

In this work, eight distinct LDO architectures were designed, implemented, and analyzed based on a 22 nm FDX CMOS technology. All designs target a regulated 0.8 V output from a 1.5 V input supply, while supporting a wide dynamic load current range from  $10\ \mu\text{A}$  to 100 mA. The implemented structures span both PMOS- and NMOS-based topologies, including external-capacitor designs, capacitor-less voltage-mode designs with or without resistive feedback, and current-mode capacitor-less designs, including one optimized for ultra-low quiescent current.

The results demonstrate that NMOS-based LDOs consistently outperform PMOS counterparts across nearly all performance categories. NMOS pass transistors, enabled by their higher carrier mobility and lower on-resistance, achieve significantly lower dropout voltages—up to 60–70% improvement under equivalent load conditions. In terms of regulation, NMOS designs maintain excellent line and load regulation, even in fully integrated, capacitor-less forms.

Capacitor-less NMOS LDOs further show strong power supply rejection, particularly in high-frequency domains, and exhibit outstanding transient behavior. Voltage deviations during input or load transitions remain within tens of millivolts, with sub-10  $\mu\text{s}$  settling times, outperforming many PMOS-based structures. Among the eight designs, the NMOS voltage-mode LDO without feedback resistors achieves the best trade-off between compactness, dynamic response, and regulation accuracy.

Current-mode architectures also demonstrate clear advantages in transient control for PMOS designs, helping to compensate for their inherently slower response. However, the effectiveness of this technique is highly dependent on bias strength. The low- $I_Q$  current-mode version exhibits notable performance degradation due to insufficient dynamic drive.

In conclusion, these eight designs collectively demonstrate the feasibility of building high-performance, fully integrated, and capacitor-less LDOs on advanced technology nodes. The 22 nm CMOS implementation validates that even with aggressive area and power constraints, modern compensation strategies—including current-mode control and feedback elimination—can enable stable and efficient regulation across wide operating conditions.

## 6.2 Outlook

Although the performance of the capacitorless LDO designed in this paper can basically meet the targets, there are still deficiencies and areas for improvement.

Mainly for the voltage type LDO topology architecture can be for the transient response and PSRR function of the demand for topology design improvements: for example, add the appropriate Buffer structure, add Flipped Voltage Follower (FVF) combined Super Source Follower (SSF) to improve the response speed, bias current for dynamic design. In addition to the core design, the layout design of a low dropout regulator (LDO) can also be developed using the layout module to more fully analyze and optimize the LDO architecture. Transistor size has a significant impact on system performance, and further optimization of transistor size can effectively balance chip area and performance. Moreover, there is still room for

improvement in the temperature coefficient and power supply rejection ratio (PSRR) of the bandgap reference voltage circuit. In the simulation experiments of this paper, the reference voltage is directly provided by an ideal voltage source.

On the other hand, to achieve ultra-low quiescent currents in capacitorless low dropout regulator (LDO) designs, the following innovations can be explored:

**Bandgap reference voltage storage:** The bandgap reference voltage can be stored in a capacitor, after which the bandgap module is turned off to eliminate its power consumption. The voltage stored on the capacitor then powers subsequent circuitry, significantly reducing quiescent power consumption.

**Error Amplifier Capacitor Storage:** Similarly, an error amplifier can use capacitor storage to maintain its operating voltage. Ideally, this approach allows the amplifier to operate without consuming continuous current, thus further reducing power consumption.

The above idea brings with it the challenge of variable load currents: if the load current changes, the stored voltage may no longer match the value required by the dynamics, leading to circuit failures. Therefore, to solve this problem, a clock module can be introduced to control the periodic switching. By running the clock at a frequency higher than the rate of change of the load current, the system can dynamically adapt to sudden changes in current demand, ensuring stable operation.

# A Appendix

## A.1 Design Path

This chapter describes the location in the 22 nm FDX library of the design corresponding to the image above.

Figure 4.2, Simple transconductance amplifier structure located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/LDO_Current/OPA_PMOS2/maestro`.

Figure 4.3, Folded Cascode OTA Architecture located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/2_OPAMP/opampstart6_startup/maestro`

Figure 4.5, Bandgap Voltage Reference Design located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/3_BG/opampstart6_startup2_stb_res2/maestro`

Figure 4.6, Source Follower Based Pre-Filter located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/LDO_millier_test/lD0test_OPA6_millier5+SF2/maestro`.

Figure 5.1, PMOS Capacitor-based LDO (Large off-chip capacitor 2.5  $\mu\text{F}$ ) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/0top/top1_CP`. The test platform uses the `tb_top1_CP` series in the same directory.

Figure 5.2, NMOS Capacitor-based LDO (Large off-chip capacitor 2.5  $\mu\text{F}$ ) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/0top/top1_CN_egs`. The test platform uses the `tb_top1_CN` series in the same directory.

Figure 5.3, PMOS Capacitor-less LDO (Voltage-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/LDO_millier_test/lD0test_OPA6_PMOS4_millier3/maestro`.

Figure 5.4, NMOS Capacitor-less LDO (Voltage-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/0top/top2_CN_egs_100p_symbol`. The test platform uses the `tb_top1_CN` series in the same directory.

Figure 5.5, PMOS Capacitor-less LDO without Feedback Resistors (Voltage-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/Vref0.8/top5_OPA6_P4_noR1/maestro`.

Figure 5.6, NMOS Capacitor-less LDO without Feedback Resistors (Voltage-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/Vref0.8/top5_N_noR/maestro`.

Figure 5.8, PMOS Folder-cascode CM-LDO (Current-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/LDO_Current/LDO_PMOS+OPA6_3/maestro`.

Figure 5.8, Low Quiescent CM-LDO (Current-mode On-chip capacitor 100 pF) located in the `nas/ei/share/TUEILSEprojects/pmic/Forschungsdaten/ge48vam_Lou/FDX22/LDO/LDO_Current/LDO_PMOS1_1/maestro`.



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