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Design of a High-Performance Power Supply Module with Subsection Compensation BGR and Capless LDO for Chip Applications

Chiyuan Zhang
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China
220190611@aa.seu.edu.cn

Bin Wang
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China
binjingshi@163.com

Hongju Yue
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China
18192537355@163.com

Ting Li
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China

Liang Yang
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China

Lijun Gao
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China
gaolijun1234@126.com

Haisong Li
Intergrated circuit design division
CASC NO. 771 Institute
Xi'an, China
holibible@126.com

***Abstract*—A high-performance power supply module for chip applications is presented in this paper using 180nm CMOS technology. The module includes a subsection compensation bandgap reference (BGR) and a capless low-dropout regulator (LDO) to address low temperature drift and low load adjustment (LDR) challenges. The temperature coefficient (TC) of the power supply module output voltage can be reduced using the subsection compensation technique. Additionally, the capless LDO with transient enhancement ensures proper functionality of the power supply module within the chip. Simulation results demonstrate that the proposed power supply module achieves a TC lower than 3 ppm/K, LDR lower than 0.002%, and overshot and undershot voltage lower than 400 μV, confirming its effectiveness in meeting low temperature drift and low load adjustment rate requirements.**

Keywords—Power supply module, Bandgap reference, Low-dropout regulator, Subsection compensation, Transient enhancement.

I. INTRODUCTION

When designing integrated circuits (IC), the power supply module faces a significant challenge due to the need to adjust the output current for other modules[1]. For instance, the power supply module is used as a reference source to power the charge redistribution digital-to-analog converter (CDAC) in a successive-approximation-register analog-to-digital (SAR ADC). In case the reference source undergoes temperature changes, the circuit can cause a significant gain error. During the SAR ADC process, if LDR of the power supply module is too low, it can result in out-of-code situations[2][3]. With increasing chip operating frequencies, power module designs have stricter requirements, including the ability to switch more quickly.

Recently, the basic structure of the power supply module is shown in Fig. 1. The basic circuit modules include BGR and

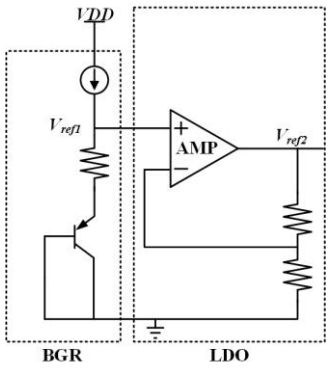


Fig. 1. The basic circuit of an on-chip reference source

LDO [4]. Firstly, the *VDD* of the input chip is transformed through BGR into V_{REF1} which is independent of the *VDD* and temperature. The next step involves converting the voltage to V_{REF2} through an LDO that comprises an amplifier and feedback network. This ensures that V_{REF2} has a high-drive capability and low-temperature drift, making it suitable for powering the chip's internal components.

The power supply module source on the chip utilizes a BGR to ensure low temperature drift of the output voltage. Various BGR compensation solutions have been proposed in the literature [5][6], which introduce different temperature compensation techniques to reduce the TC variation of the BGR output to about 5 ppm/K. In literature [7], a method of piecewise compensation is proposed in, where different compensation measures are applied in the low temperature and high temperature sections, respectively. In this paper, a subsection temperature compensation method is presented, where the complementary to absolute temperature (CTAT) current is input

at low temperature and the proportional to absolute temperature (PTAT) current is output at high temperature to compensate for the reduction of reference voltage in high and low temperature. As a result, a temperature drift of lower than 3 ppm/K is achieved.

LDO is designed to improve the driving capability of the reference source in the power supply module. Conventional LDO modules typically require external load capacitors to maintain loop stability and minimize overshoot and undershoot voltages caused by switching [8]. Capless LDO offers the advantage of supplying power to on-chip modules requiring a reference source without the need for external pins on the chip's periphery, facilitating chip layout and connection. The literature [9][10] describes transient response enhancement circuits for LDO during load switching, but these structure required additional power and circuit. This paper presents an effective circuit for enhancing the transient response of a LDO that enables rapid response to load changes through different operating modes when switching between two types of loads, without increasing the static current consumption.

II. Proposed Circuit

A. Bandgap with subsection temperature compensation

Based on prior research, the fundamental principle of BGR is to combine the voltage of a positive TC and the voltage of a negative TC to produce the voltage of a zero TC, as illustrated in Fig. 2. The positive TC is supplied by V_{R1} while the negative TC is provided by V_{BE1}:

$$\begin{cases} \dfrac{\partial \mathrm{V}_{R1}}{\partial \mathrm{T}} = \dfrac{k}{q}\ln n \\ \dfrac{\partial \mathrm{V}_{BE1}}{\partial \mathrm{T}} = \dfrac{\mathrm{V}_{BE} - (4+m)\mathrm{V}_T - E_g/q}{T} \end{cases} \tag{1}$$

Equation (1) reveals that the positive TC remains constant, while the negative TC varies with temperature. Typically, the TC is about 10 ppm/K without any compensation. In conventional BGR, the reference voltage in both high and low temperature regions will be decreased, and the output voltage waveform will appear as an open downward parabolic curve. To reduce the TC of the reference voltage, this paper adopts a subsection temperature compensation that adjusts the current in the branch to increase the reference voltage in the high and low temperature ranges.

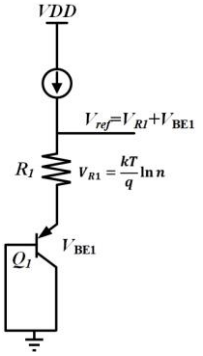


Fig. 2. The basic circuit of an on-chip reference source

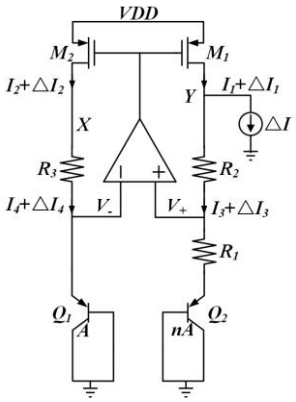


Fig. 3. A PTAT current increment $\triangle I$ is extracted from node Y.

The following section discusses the high and low temperature compensation techniques. Fig. 3 illustrates the high temperature compensation circuit for the BGR circuit. When current $\triangle I$ is extracted from node Y, the current flowing through each branch will change accordingly. Initially, V_- is equal to V_+ and I_1, I_2, I_3, and I_4 are equal. Assuming that the change in $\triangle I_3$ is small, PMOS M_1 and M_2 will provide a larger current, resulting in $\triangle I_1 = \triangle I_2 = \triangle I_4 = \triangle I$. The operational amplifier clamping effect forces $\triangle V_-$ to equal $\triangle V_+$.

$$\begin{cases} \triangle V_- = V_T \ln\dfrac{I_4 + \triangle I_4}{I_s} - V_T \ln\dfrac{I_4}{I_s} \\ \triangle V_+ = (I_3 + \triangle I_3)R_1 + V_T \ln\dfrac{I_3 + \triangle I_3}{nI_s} - \left(I_3 R_1 + V_T \ln\dfrac{I_3}{nI_s}\right) \end{cases} \tag{2}$$

Due to the small size of $\triangle I$, the term $\ln(1+\triangle I/I)$ can be approximated as $\triangle I/I$:

$$\triangle I_3 = \frac{\dfrac{V_T}{I_4}}{R_1 + \dfrac{V_T}{I_3}} \triangle I_4 \tag{3}$$

Substituting the parameters of the designed BGR core circuit yields $\triangle I_3 = 0.3\triangle I_4$, which ultimately results in $\triangle I_3 = 0.429\triangle I$. The increment of the reference voltage can be expressed as:

$$\triangle V_{ref} = \triangle I_3(R_1 + R_2) + V_T \frac{\triangle I_3}{nI_s} \tag{4}$$

If $\triangle I$ represents a PTAT current that is cut off at low temperature and gradually increases with increasing temperature. The extracted current $\triangle I$ at low temperature has no impact on the reference voltage, while at high temperature it will cause an increase in the reference voltage. To compensate TC at low temperatures, CTAT current is required to be injected into the circuit. However, it is not recommended to inject and extract current simultaneously in the same branch in order to avoid introducing an additional degeneracy state. Thus, in this design, the current is injected into another branch instead, as illustrated in Fig. 4.

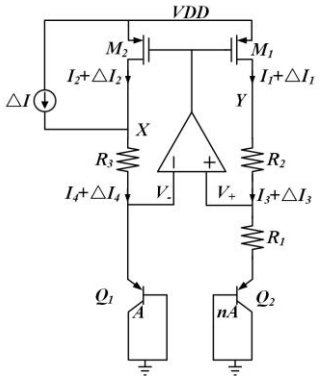


Fig. 4. A CTAT current increment $\triangle I$ is intracted into node X.

The mirroring action of the current mirror M_1 and M_2 results in $\triangle I_1 = \triangle I_2$. Additionally, from the previous analysis, $\triangle I_3 = 0.3\triangle I_4$ can be obtained:

$$\begin{cases} \triangle I_2 = \triangle I_4 - \triangle I \\ \triangle I_1 = \triangle I_2 = \triangle I_3 = 0.3\triangle I_4 \end{cases} \tag{5}$$

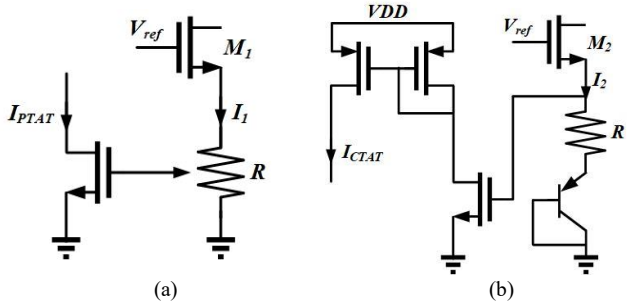
By substituting the value of this design, $\triangle I_4 = 1.429\triangle I$ and $\triangle I_3 = 0.429\triangle I$. The increment of the reference voltage can be obtained from Equation (4), which remains the same when calculated using the values obtained from Equation (5). If $\triangle I$ is a CTAT current, the current injected at high temperature will not affect the reference voltage, but at low temperature, it will increase the reference voltage.

The TC of the reference voltage is reduced by adjusting the current of the node X and Y in the high and low temperature range.

B. PTAT and CTCT current generation

Fig. 5 shows the circuit that generates the PTAT and CTAT currents. In Fig. 5(a), the MOS transistor operates in the saturation region at high temperature:

$$\begin{cases} \mathrm{V}_{ref} = \sqrt{\dfrac{2I_1}{C_{ox}\mu_n \dfrac{W}{L}_1}} + \mathrm{V}_{th} + I_1 R \\ \mathrm{I}_{PTAT} = \dfrac{1}{2} C_{ox}\mu_n \dfrac{W}{L}_2 (I_1 R - \mathrm{V}_{th})^2 \end{cases} \tag{6}$$



(a) (b)

Fig. 5. The circuit of generating calibration current（a）PTAT（b）CTAT

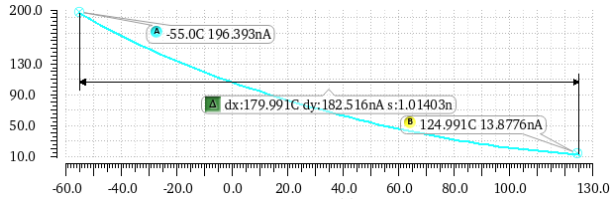
Taking into account the temperature coefficients of μ_n and V_{th}, Equation (6) is differentiated with respect to temperature (T):

$$\begin{cases} \dfrac{\partial I_1}{\partial T} = \dfrac{\dfrac{1}{\mu_n}\sqrt{\dfrac{I_1}{2C_{ox}\mu_n \dfrac{W}{L}_1}}\dfrac{\partial \mu_n}{\partial T} - \dfrac{\partial \mathrm{V}_{th}}{\partial T}}{R + \sqrt{\dfrac{1}{2I_1 C_{ox}\mu_n \dfrac{W}{L}_1}}} \\ \dfrac{\partial \mathrm{I}_{PTAT}}{\partial T} = K * \left((I_1 R - \mathrm{V}_{th})\dfrac{\partial \mu_n}{\partial T} + R\mu_n \dfrac{\partial I_1}{\partial T} - \mu_n \dfrac{\partial \mathrm{V}_{th}}{\partial T} \right) \end{cases} \tag{7}$$

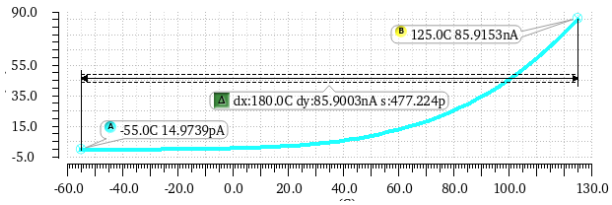
In Equation (7), $K=C_{ox}\mu_n W/L_1$. By calculation, $R\mu_n \partial I_1/\partial T$ is larger than the other two coefficients, it can be found that I_1 and I_{PTAT} have positive TC. Similarly, the following can be analyzed in Fig. 5(b):

$$\begin{cases} \dfrac{\partial I_2}{\partial T} = \dfrac{\dfrac{1}{\mu_n}\sqrt{\dfrac{I_2}{2C_{ox}\mu_n \dfrac{W}{L}_3}}\dfrac{\partial \mu_n}{\partial T} - \dfrac{\partial \mathrm{V}_{th}}{\partial T} - \dfrac{\partial V_{BE}}{\partial T}}{R + \sqrt{\dfrac{1}{2I_3 C_{ox}\mu_n \dfrac{W}{L}_3}}} \\ \dfrac{\partial \mathrm{I}_{CTAT}}{\partial T} = K * \left((I_2 R + \mathrm{V}_{BE} - \mathrm{V}_{th})\dfrac{\partial \mu_n}{\partial T} + R\mu_n \dfrac{\partial I_2}{\partial T} + \mu_n \left(\dfrac{\partial \mathrm{V}_{BE}}{\partial T} - \dfrac{\partial \mathrm{V}_{th}}{\partial T} \right) \right) \end{cases} \tag{8}$$

In Equation (8), $K=C_{ox}\mu_n W/L_2$. I_2 remains a positive TC current, while I_{CTAT} is a negative TC current since $\mu_n \partial V_{BE}/\partial T$ is larger than the other coefficients. The simulation results for PTAT and CTAT currents are presented in Fig. 6. Fig. 6. shows that the CTAT current decreased from 196 nA at low temperature to 14 nA at high temperature, while the PTAT current increased from 15 pA at low temperature to 86 nA at high temperature, consistent with the temperature coefficient calculation.



（a）CTAT



（b）PTAT

Fig. 6. The Current simulation results（a）CTAT（b）PTAT

C. Capless-LDO

When the LDO is switched, there will be an instantaneous current difference in the power transistor. Firstly, the current difference charges and discharges the load capacitor, which changes the output voltage of the LDO. V_{out} affects the amplifier through the feedback system, causing the amplifier to enter the large signal state.

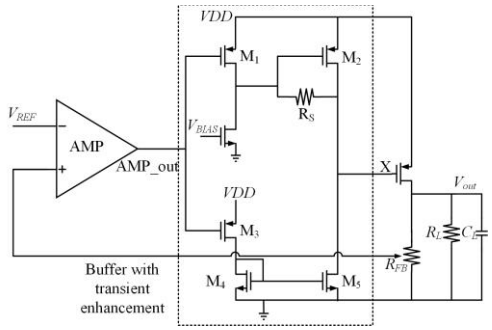


Fig. 7. Capless-LDO with transient enhancement buffer

Due to the large size of the power transistor, its gate capacitance results in slow gate voltage changes. The amplifier bias current rapidly charges and discharges the gate capacitor of the power transistor, which adjusts V_{out} voltage.

The LDO utilizes an off-chip capacitor to maintain loop stability and mitigate voltage fluctuations during transient switching. This design incorporates a capless-LDO with a transient enhancement function for the power transistor drive buffer. The purpose of this design is to effectively handle the significant voltage changes that occur due to off-chip capacitance during transient response. The circuit diagram for this capless-LDO is shown in Fig. 7.

The buffer in this design offers the greatest advantage of quick charging and discharging of node X in response to changes in output current after the amplifier enters the big signal working state. The transient responses in the two different operating states are shown in Fig. 8.

In Fig. 8(a), when V_{out} decreases, the *AMP_out* decreases, and M_1 and M_3 cut off in the buffer. The offset current of M_1 discharges the gate of M_2, causing the gate voltage of M_2 to rapidly decrease, thereby increasing the output voltage of the LDO. In Fig. 8(b), when V_{out} rises and the *AMP_out* rises, the V_{GS} of M_1 and M_3 increase, leading to more current. The additional current in M_1 charges the gate capacitor of M_2, making M_2 cut off completely, while the increased current in M_5 charges node X, lowering the gate voltage of the power tube, thereby decreasing the output voltage of the LDO.

The buffer with transient enhancement changes the operating state of M_2 and M_5 by detecting changes in the amplifier output voltage when the LDO output goes up or down.

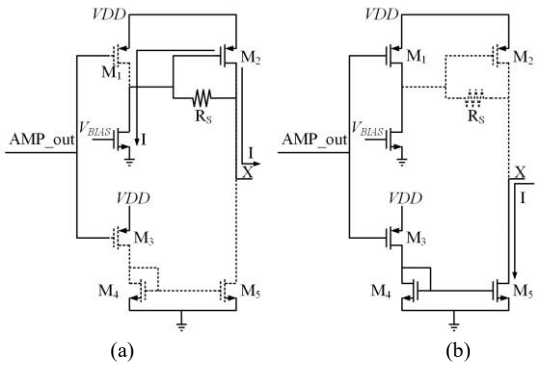


Fig. 8. Charge and discharge node X under different operating modes (a) charge (b) discharge

The current flowing through M_2 or M_5 is charged and discharged directly to the grid of the power tube without static power consumption. The simulation results depicted demonstrate that the buffer exhibits a current of over 30 μA for charging and discharging node X during the switching of output current between 20 mA and 200 μA. After the conversion is completed, the current in the buffer returns to the normal static current.

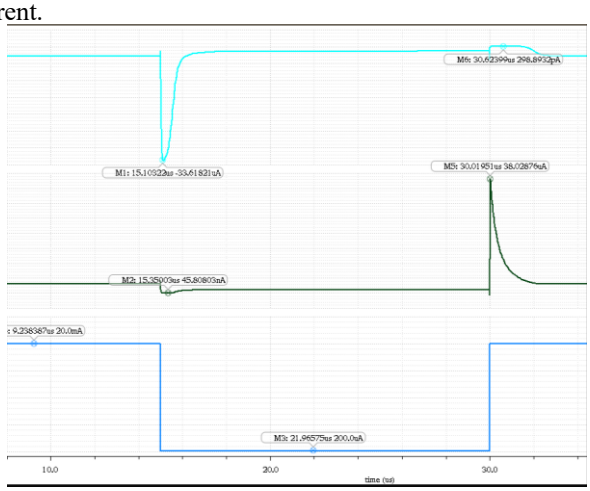


Fig. 9. Current changes in the buffer with transient enhancement

Compared to the traditional source follower buffer with transient enhancement, another advantage is that it has its own gain. The buffer's own gain boosts the loop gain, which in turn reduces load and line regulation of the LDO, leading to lower output voltage fluctuation:

$$A_V = g_{M1}R_S + g_{M3}\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}\frac{1}{g_{M2}} \tag{9}$$

Achieving loop stability is another design challenge of the capless LDO. It is common for LDO to have three poles: the dominant pole from the operational amplifier, the output pole from the power transistor and the pole from node X. The frequency of pole from node X is much higher than that of the other two poles.

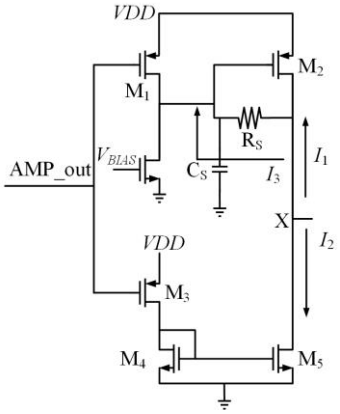


Fig. 10. The zero point introduced by two paths in transient-enhancement buffer

However, due to the presence of two paths in the transient-enhanced buffer, an additional zero is introduced in the loop where the current is zero, as depicted in Fig. 10. In the circuit, KCL analysis and calculations were performed to determine:

$$g_{M2}\left(-g_{M1}V_{in}\left(R_S//\frac{1}{sC_s}\right)\right)+g_{M1}V_{in}\frac{\frac{1}{sC_s}}{R_S+\frac{1}{sC_s}}-g_{M3}V_{in}=0 \quad (10)$$

Based on the calculation and analysis of the KCL equation in the circuit, it can be deduced from Equation (10):

$$z=\frac{g_{M1}-g_{M1}g_{M2}R_S-g_{M3}}{g_{M3}R_SC_s} \quad (11)$$

The purpose of introducing the additional zero in the loop is to cancel out the pole of the operational amplifier, as explained in Equation (10). This allows the LDO to have only one dominant output pole, which can be biased to serve as the primary pole of the capless-LDO with only a 10 pF on-chip capacitor.

III. Simulation Results

A. Simulation of BGR

The simulation results for various calibration techniques of the BGR are presented in Fig. 11, based on the analysis of the bandgap reference. These calibration techniques include no-calibration, high-temperature calibration, low-temperature calibration, and subsection calibration.

Observing Fig. 11, it is apparent that the BGR without temperature compensation forms an open-down parabolic curve and the TC is 12 ppm/K. When high-temperature compensation is applied, the reduction of the reference voltage is significantly reduced, while low-temperature compensation results in a smoothed rise of the reference voltage. The compensation curve with the lowest TC of 2.3 ppm/K is achieved through piecewise compensation. Furthermore, two points with zero temperature coefficients are visible on this curve. A comparison of their temperature coefficients is shown in Fig. 12.

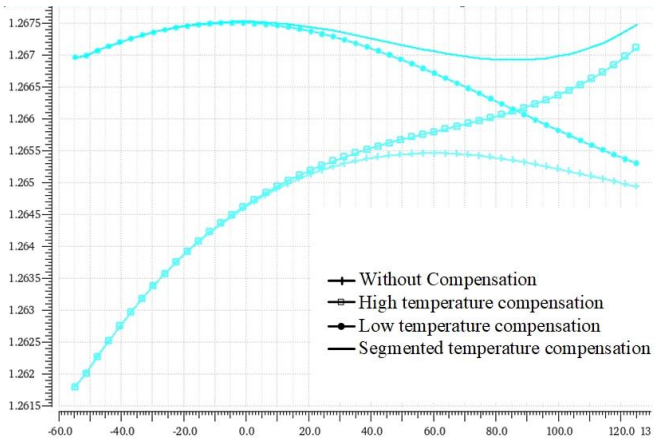


Fig. 11. The simulation results of BGR with different calibration modes

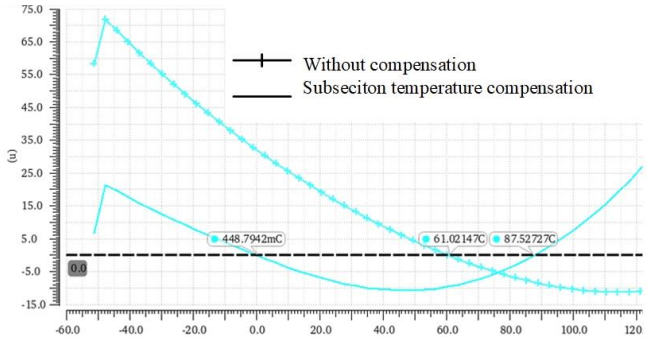


Fig. 12. The rate of the output voltage of BGR with and without compensation

As depicted in Fig. 12, the curve with compensation shows two points where the TC is zero. At lower temperatures, the temperature coefficient shows a smoother drop. On the other hand, in the high-temperature range, the TC initially decreases but eventually starts to increase.

B. Simulation of Capless-LDO

In the simulation of capless-LDO, a reference voltage of 0.6V from DC power was input into the capless-LDO with a feedback coefficient of 2, and the output current was switched between 200 uA and 20 mA over a duration of 1 ns, as depicted in Fig. 13. As shown in Fig. 13, the LDO's recovery time to ±10% of 1.2 V was 0.22 us and 0.29 us, respectively.

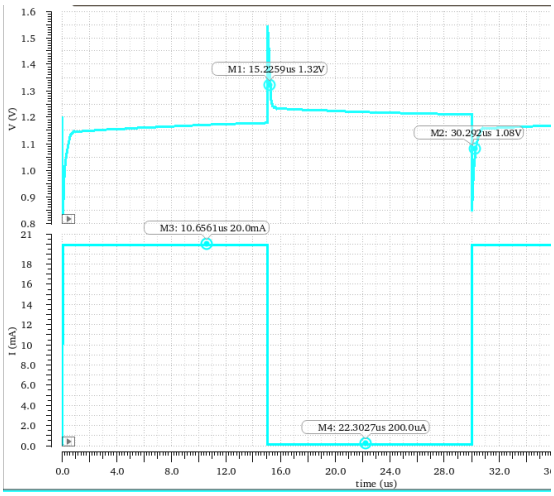


Fig. 13. Simulation of LDO transient load switching

C. Simulation of Power Supply Module

Subsequently, the output of the bandgap reference is connected to the LDO through the voltage divider to simulate and verify the entire system's function.

The validity of the subsection temperature compensation circuit is verified by analyzing the output voltage variation of the power supply module with temperature at each corner. As illustrated in Fig. 14, the output voltage of the power supply module exhibits little variation with temperature at each corner, indicating the effectiveness of the temperature compensation scheme. The TC under tt corners is measured to be 2.3 ppm/K.

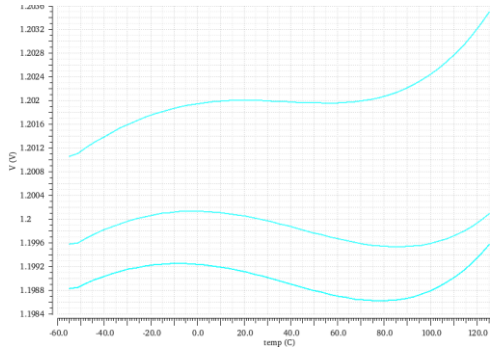


Fig. 14. Output voltage variation with temperature at each process corner

The effectiveness of the system's transient switching circuit is verified by simulating and analyzing the transient response, as illustrated in Fig. 15. It can be observed that at every process corner, the system swiftly stabilizes to less than 10% of the reference voltage following load switching, demonstrating the circuit's capability to handle transients. Furthermore, the down-conversion time under tt corner is less than 0.3 us.

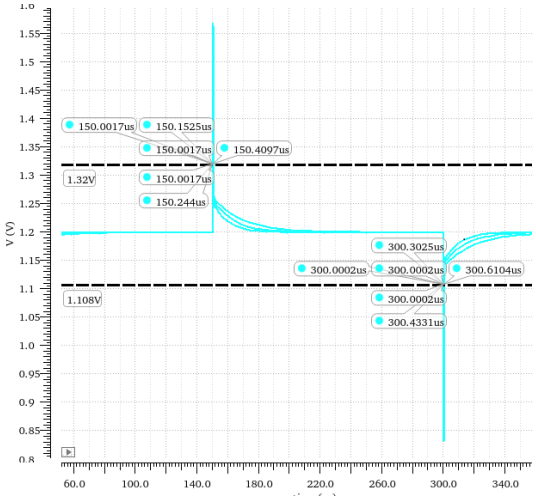


Fig. 15. Transient response at each process corner

The circuit for simulating the system with power supply voltage (from 2.5 V to 3.6 V) and corner as variables is shown in Fig. 16. The output voltage of the power supply module varies with the supply voltage and corner. The linear adjustment rate under tt is about 0.03%.

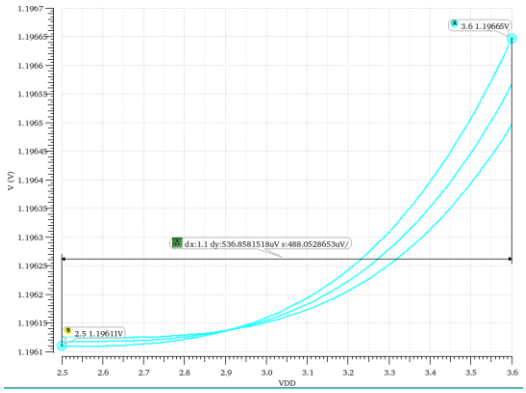


Fig. 16. Linear adjustment rate at each process corner

Fig. 17 illustrates the circuit used to simulate the system with load current and process corners as variables. The results show that the output voltage of the power supply module varies with changes in load current (from 200 uA to 20 mA) and process corner, with the LDR of 0.58% under tt.

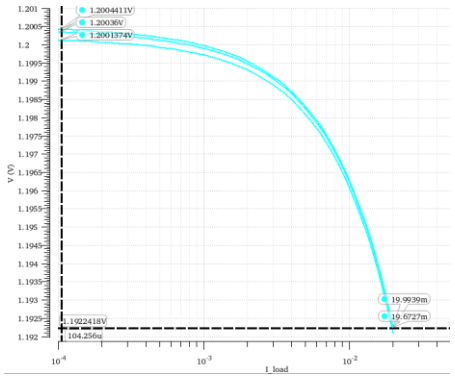


Fig. 17. LDR at each process corner

IV. Summary

This thesis presents the design of an in-chip power supply module that exhibits low temperature drift and low load adjustment rate. To minimize the TC of the output voltage, an effective subsection temperature compensation scheme is introduced, resulting in a reduction of the reference voltage variation with temperature to 2.3 ppm/K. Additionally, to address load current variation, a capless-LDO with a transient enhancement buffer is designed, reducing LDR to 0.58% and the recovery time to 0.3 us. The designed power supply module exhibits stable output voltage under varying temperature and load conditions, making it well-suited for GHz chips.

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