

# An External Capacitorless Low-Dropout Regulator With High PSR at All Frequencies From 10 kHz to 1 GHz Using an Adaptive Supply-Ripple Cancellation Technique

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**Abstract**—Herein is presented an external capacitorless low-dropout regulator (LDO) that provides high-power-supply rejection (PSR) at all low-to-high frequencies. The LDO is designed to have the dominant pole at the gate of the pass transistor to secure stability without the use of an external capacitor, even when the load current increases significantly. Using the proposed adaptive supply-ripple cancellation (ASRC) technique, in which the ripples copied from the supply are injected adaptively to the body gate, the PSR hump that appears in conventional gate-pole-dominant LDOs can be suppressed significantly. Since the ASRC circuit continues to adjust the magnitude of the injecting ripples to an optimal value, the LDO presented here can maintain high PSRs, irrespective of the magnitude of the load current  $I_L$ , or the dropout voltage  $V_{DO}$ . The proposed LDO was fabricated in a 65-nm CMOS process, and it had an input voltage of 1.2 V. With a 240-pF load capacitor, the measured PSRs were less than  $-36$  dB at all frequencies from 10 kHz to 1 GHz, despite changes of  $I_L$  and  $V_{DO}$  as well as process, voltage, temperature (PVT) variations.

**Index Terms**—External capacitorless, low-dropout regulator (LDO), power-supply rejection (PSR), stability, supply-ripple cancellation (SRC).

## I. INTRODUCTION

TO MEET the requirements of high data rates of advanced wireless standards, the bandwidth of RF transceivers must increase significantly. As a representative example, to support data rates more than 10 Gb/s, transceivers for 5G systems

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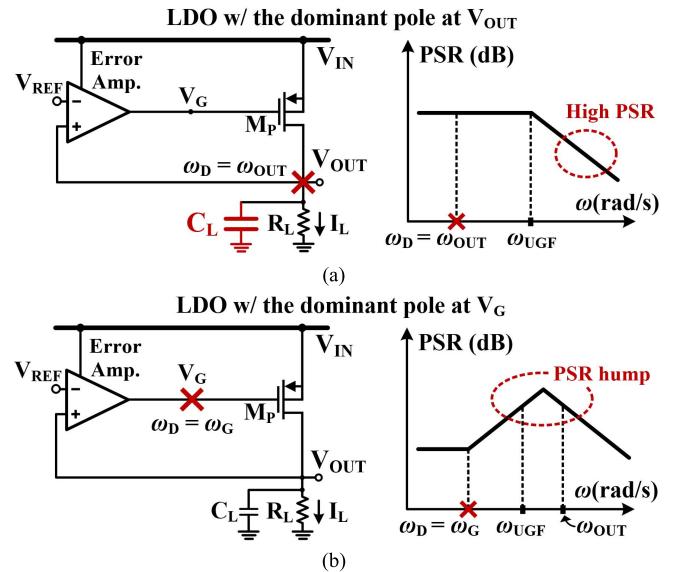


Fig. 1. LDOs with the dominant pole at (a) output, i.e.,  $\omega_D = \omega_{OUT}$  and (b) gate, i.e.,  $\omega_D = \omega_G$ .

are asked to have a wide channel bandwidth, such as more than 100 MHz [1], [2]. RF transceivers for IEEE 802.11ad standards need to have even a wider bandwidth, which is more than several hundred megahertz [3], [4]. Since modern-mobile system-on-chips (SoCs) demand the increase in the degree of integration, to protect sensitive analog/RF-building circuits of transceivers from internal aggressors, i.e., spurious tones and the noise of digital circuits, is a critical task. For the protection of RF and analog circuits, one of the most effective solutions is to use on-chip low-dropout regulators (LDOs) that provide high-power-supply rejection (PSR) over the bandwidth of the circuits to be protected [5]. In recent years, a key trend has been to remove the use of external components and fully integrate LDOs in silicon, thereby reducing the manufacturing cost and the sizes of printed circuit boards (PCBs).

In general, LDOs can be divided into two categories according to the location of the dominant pole  $\omega_D$  of the regulating loop [6]. In the first category, as shown in Fig. 1(a), LDOs have the dominant pole at the output  $V_{OUT}$ , i.e.,  $\omega_D = \omega_{OUT}$ ,

where  $\omega_{\text{OUT}}$  is the frequency of the output pole [7]–[12]. In the second category, as shown in Fig. 1(b), LDOs have the dominant pole at the gate of the pass transistor  $M_P$ , i.e.,  $\omega_D = \omega_G$ , where  $\omega_G$  is the frequency of the gate pole of  $M_P$  [13]–[20]. According to the location of the dominant pole, these two types of LDOs have very different PSR characteristics. First, as shown in Fig. 1(a), when the dominant pole is at  $V_{\text{OUT}}$ , LDOs easily can achieve high PSR at a high-frequency region. This is because the large capacitor at the output  $C_L$  forms a bypass path to the ground for supply ripples at high frequencies that are greater than the unity-gain frequency ( $\omega_{\text{UGF}}$ ) of the loop [6]. However, despite the advantage of high PSR at high frequencies, these LDOs could have stability problems when the load current  $I_L$  is large, since the dominant pole ( $\omega_{\text{OUT}}$ ) moves toward  $\omega_G$  as  $I_L$  increases. Thus, to ensure stability, the size of  $C_L$  must increase significantly; in practice, the size of  $C_L$  is increased to a range of several microfarads, thereby necessitating the use of an expensive external capacitor. To reduce the size of  $C_L$  to an integration-available level, an LDO has been presented that uses a wideband error amplifier (EA) to push  $\omega_G$  far from  $\omega_{\text{OUT}}$  [12]. However, the reduced gain of the EA  $A_{\text{EA}}$  degraded the PSR at frequencies below  $\omega_{\text{UGF}}$ . On the other hand, for the LDOs in the second category ( $\omega_D = \omega_G$ ), as shown in Fig. 1(b), the size of  $C_L$  can be minimized because the increase in  $I_L$  pushes  $\omega_{\text{OUT}}$  from  $\omega_G$ . However, as a tradeoff for a small  $C_L$ ,  $\omega_G$ -dominant LDOs have an intrinsic problem, i.e., the presence of a PSR hump. At frequencies above  $\omega_G$ , the gate of  $M_P$  is shunted down to the ground, so the PSR is degraded continuously until supply ripples are suppressed by  $C_L$ . Consequently, a hump-shaped zone having the worst PSR is supposed to appear around  $\omega_{\text{UGF}}$  [6]. The simplest method to alleviate this PSR hump problem is to increase  $\omega_G$  to a higher frequency, but this could cause the potential stability problem as  $\omega_G$  approaches  $\omega_{\text{OUT}}$  [20].

Based on the foregoing discussion regarding the two types of LDOs, it is obvious that a gate-pole-dominant architecture is suitable for designing fully integrated LDOs without the use of external capacitors. Then, the question is how to remove the PSR hump of this type of LDOs. Recently, supply-ripple cancellation (SRC) techniques [21]–[26] have been presented to suppress this PSR hump using a feed-forward path. The supply ripples with the amplitude of  $v_R$  are amplified by the SRC, and then, the amplified version of the ripples is injected to the gate of  $M_P$ ,  $V_G$ . At this moment, if the magnitude of the ripples injected by the SRC circuit  $v_{\text{SRC}}$  is optimal, the supply ripples can be cancelled out completely at  $V_{\text{OUT}}$  so that the LDO can achieve very high PSR in a high-frequency region. Based on the same mechanism, it is also possible to implement an SRC to inject the ripples to the body-gate  $V_B$ . However, the conventional SRC techniques have a critical problem, which stems from the fact that the optimal  $v_{\text{SRC}}$  is not stationary but varies across different  $I_L$ s and dropout voltages,  $V_{\text{DOS}}$ . Since the effectiveness of the PSR suppression is easily degraded as  $v_{\text{SRC}}$  deviates from the optimal value, conventional SRC techniques that use ripples with a fixed  $v_{\text{SRC}}$  hardly achieve a robust PSR performance.

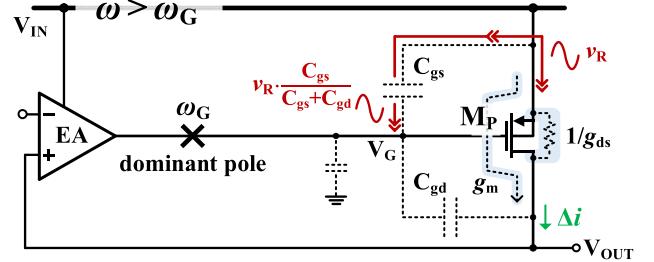


Fig. 2. Supply-noise coupling paths of gate-pole-dominant LDOs.

The architectures and the problems of conventional SRC techniques are discussed in Section II.

In this paper, we present an external capacitorless, gate-pole-dominant LDO, providing high PSR at all low-to-high frequencies. By using the proposed adaptive SRC (ASRC) technique that can continuously calibrate  $v_{\text{SRC}}$  close to the optimal value [27], the supply ripples at  $V_{\text{OUT}}$  can be cancelled out effectively by the injected SRC ripples; thus, the LDO of this paper can maintain high PSRs over wide frequencies, regardless of the changes of  $I_L$  and  $V_{\text{DO}}$  and variations in the process, voltage, and temperature (PVT) variations.

The rest of this paper is organized as follows. Section II presents the study of the SRC mechanism and the limits of conventional architectures. Section III presents the concept and the design of the proposed ASRC, and Section IV shows the implementation of the LDO in this paper. Section V presents the analysis and the simulation results of the PSR of the proposed LDO. Experimental results and conclusions are presented in Sections VI and VII, respectively.

## II. STUDY OF THE SRC TECHNIQUE AND PROBLEMS OF CONVENTIONAL ARCHITECTURES

### A. Analysis of the Optimal Gain of SRC Circuits

To calculate the optimal value of  $v_{\text{SRC}}$ , the analysis of noise coupling from the supply to  $V_{\text{OUT}}$  is required for gate-pole-dominant LDOs. In this analysis, we need to focus on the supply-noise coupling in a high-frequency region, where the PSR hump is present. Since the frequencies of interest in this analysis are sufficiently high, the effects of gate-source capacitance ( $C_{\text{gs}}$ ) and the gate-drain capacitance ( $C_{\text{gd}}$ ) of  $M_P$  should be considered carefully. A parasitic capacitance between  $V_G$  and dc ground can be ignored, since in general, it is much smaller than  $C_{\text{gs}}$  and  $C_{\text{gd}}$  [26]. As shown in Fig. 2, there are two major supply-noise coupling paths. The first path is through the transconductance ( $g_m$ ) of  $M_P$ . Through this path, the relative magnitude of the ripples at  $V_{\text{IN}}$  with respect to those at  $V_G$  is multiplied by  $g_m$ , finally causing the current ripple  $\Delta i$  at the load line. Therefore, the magnitude of  $\Delta i$  depends on the ratio of  $C_{\text{gs}}$  to  $C_{\text{gd}}$  [26] that determines the magnitude of the supply ripples coupled to  $V_G$ . We ignore possible ripples, which could be coupled to  $V_G$  through the supply line of the EA, since they must be suppressed significantly at the frequencies of interest due to the low-frequency pole at  $\omega_G$ . The second path is via the drain-source conductance ( $g_{\text{ds}}$ ) of  $M_P$ , through which supply ripples are directly converted into  $\Delta i$  [21].

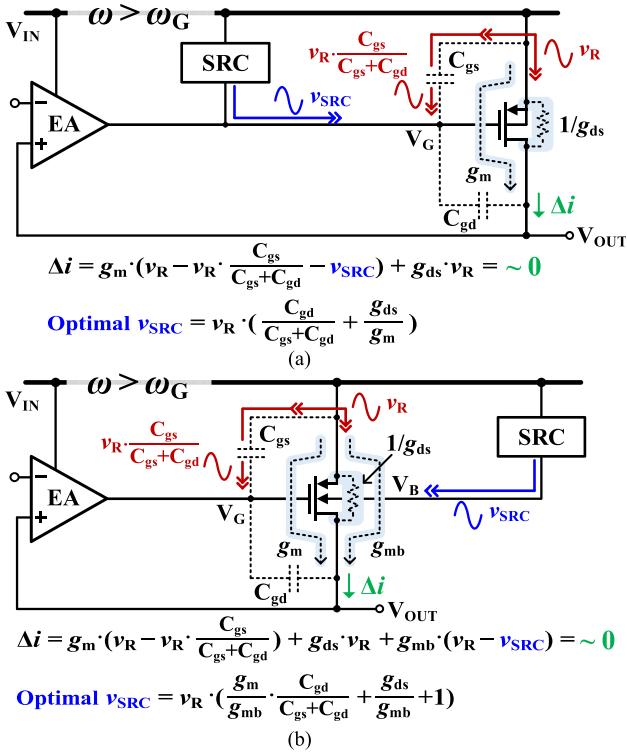


Fig. 3. Optimal  $v_{SRC}$  for (a) gate-injection SRCs and (b) body-gate-injection SRCs.

Fig. 3(a) and (b) shows two possible ways to inject SRC ripples to  $M_P$  to eliminate  $\Delta i$ . Fig. 3(a) shows the LDOs in [21], [22], and [24]–[26] that use the gate of  $M_P$ , through which the SRC ripple is injected. Since the purpose of an SRC technique is to suppress the PSR hump, which is present at high frequencies above  $\omega_G$  as shown in Fig. 1(b), we assume this high-frequency region for the following analysis. (Up to  $\omega_G$ , the EA itself can provide the LDO with sufficiently high PSR.) When the SRC ripple with the amplitude of  $v_{SRC}$  is injected to  $V_G$ ,  $\Delta i$  can be represented as

$$\Delta i = g_m \left( v_R - v_R \cdot \frac{C_{gs}}{C_{gs} + C_{gd}} - v_{SRC} \right) + g_{ds} v_R. \quad (1)$$

According to (1), the optimal value of  $v_{SRC}$  to eliminate  $\Delta i$  can be represented as

$$v_{SRC} = v_R \left( \frac{C_{gd}}{C_{gs} + C_{gd}} + \frac{g_{ds}}{g_m} \right). \quad (2)$$

One advantage of this type of SRC implementation is that the optimal  $v_{SRC}$  can be reduced to a small value, since  $g_m$  is larger than  $g_{ds}$ . However, these SRC techniques require an additional summing circuit to combine the signal from the SRC path with the signal from the original LDO path at  $V_G$ , and it increases the power consumption and the complexity of the design. Second, Fig. 3(b) shows the LDOs that use the body gate of  $M_P$  to inject the SRC ripple [23]. Since in this topology the feed-forward SRC path is isolated from the LDO's feedback loop, SRC ripples can be injected directly to  $V_B$  without the use of an additional summing circuit. In addition, the body gate has a much smaller parasitic

capacitance than the gate [13], [23]. Thus, the frequency bandwidth of an SRC circuit can be extended significantly without a large consumption of power. For LDOs that include an SRC technique at  $V_B$ , as shown in Fig. 3(b),  $\Delta i$  and the value of optimal  $v_{SRC}$  can be represented as the following equations:

$$\begin{aligned} \Delta i &= g_m \left( v_R - v_R \cdot \frac{C_{gs}}{C_{gs} + C_{gd}} \right) \\ &\quad + g_{ds} v_R + g_{mb} (v_R - v_{SRC}) \end{aligned} \quad (3)$$

and

$$v_{SRC} = v_R \left( \frac{g_m}{g_{mb}} \cdot \frac{C_{gd}}{C_{gs} + C_{gd}} + \frac{g_{ds}}{g_{mb}} + 1 \right). \quad (4)$$

One drawback of these SRCs is the optimal value of  $v_{SRC}$  in (4) is larger than that in (2), since  $g_m$  is much larger than  $g_{mb}$ . A  $v_{SRC}$  value that is too large could turn on the source-body diode of  $M_P$ ; thus, we must pay attention to ensure that the source-body voltage ( $V_{SB}$ ) does not exceed the forward voltage of the diode. We note that  $v_{SRCs}$  in (2) and (4) are independent of the output impedance of the EA. This is because we have limited the frequency of interest in the analysis to the frequencies above  $\omega_G$ , where the PSR hump is present. We also note that the optimal  $v_{SRC}$  either in (2) or (4) can be changed sensitively due to PVT variations as well as the changes of  $I_L$  and  $V_{DO}$ .

### B. Problems of Conventional SRC Techniques

Recently, many efforts have been made to design SRC techniques to improve the PSR performance of LDOs [21]–[26]. El-Nozahi *et al.* [21] and Yuk *et al.* [22] used the gate terminal to inject SRC ripples, while Izadpanahi and Maymandi-Nejad [23] used the body-gate terminal. However, since they have no functions to adjust  $v_{SRC}$  optimally, the PSR performance can fluctuate due to variations of  $I_L$ ,  $V_{DO}$ , and PVT. To ensure the improvement of PSR by SRC techniques, the LDOs in [24]–[26] included a scheme that can adjust  $v_{SRC}$ . Fig. 4(a) shows the LDO architecture in [24], where the gain of the amplifier can be selected between a high value and a low value with respect to the value of  $I_L$ . However, the level of adaptability is too low to guarantee the high performance of PSR. Moreover, since this method does not consider the coupling of supply ripples to the gate through  $C_{gs}$ , the value of  $v_{SRC}$  deviates from the optimal value in (2), thereby limiting the improvement of PSR. Fig. 4(b) describes the  $v_{SRC}$ -adjusting technique presented in [25], which uses the correlation of the supply ripples at  $V_{IN}$  and the ripples at  $V_{OUT}$  to adjust the gain of the amplifier that injects SRC ripples. However, this architecture also did not consider the coupling of supply ripples through  $C_{gs}$ ; thus, the PSR improvement was restricted to less than 10 dB at frequencies above 20 MHz, at which the effect of  $C_{gs}$  was considerable. Park *et al.* [26] present an SRC technique that can address the effects of  $C_{gs}$  and  $C_{gd}$  at high frequencies. As shown in Fig. 4(c), the LDO of [26] used a replica of  $M_P$ , i.e.,  $M_{PR}$ , which was scaled down by a factor of 100. In this architecture, the supply ripples through  $C_{gd}$  of  $M_{PR}$  ( $C_{gdr}$ ) are amplified 100 times by the following amplifier, and then, they are injected to  $V_G$ .

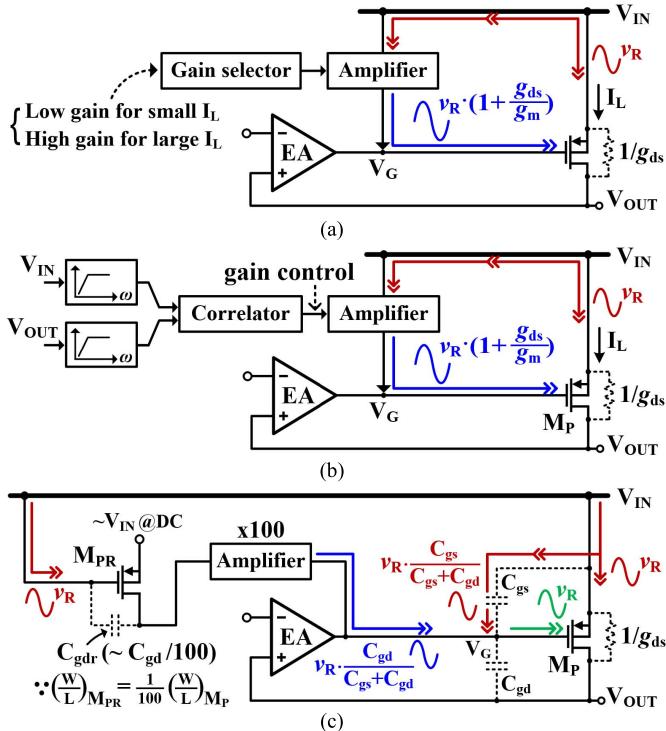


Fig. 4. Conventional adaptive SRC techniques using (a) gain selector, (b) correlator-based gain controller, and (c) scaled-down replica-MP.

Fig. 4(c) shows that the ripple at  $V_G$  effectively becomes  $v_R$  when this SRC ripple is combined with the ripple through  $C_{gs}$  of  $M_P$ ; thus, theoretically,  $\Delta i$  can be removed completely. Since  $C_{gdr}$  can track the change of  $C_{gd}$  of  $M_P$ ,  $v_{SRC}$  can be kept adjusted. However, it cannot prevent the coupling of supply ripples through  $g_{ds}$  of  $M_P$ , which is one of major coupling paths in a deep sub-micrometer technology [24].

### III. CONCEPT AND DESIGN OF THE PROPOSED ASRC TECHNIQUE

#### A. Proposed ASRC Technique

Fig. 5 shows a conceptual diagram of the proposed LDO. In this paper, we used the body gate as an injection terminal, considering the two advantages in Section II-A, i.e., no need of signal-summing circuits and the potentially wide bandwidth of an SRC technique. To address the drawback of body-gate SRCs, i.e., the need of a large  $v_{SRC}$ , the proposed LDO includes a coupling capacitor  $C_C$  between  $V_{IN}$  and  $V_G$ . When the capacitance of  $C_C$  is sufficiently larger than  $C_{gd}$ , the first term of (4) becomes zero, and (4) is reduced to

$$v_{SRC} = v_R(1 + g_{ds}/g_{mb}). \quad (5)$$

Comparing (5) to (4), we can find that the use of  $C_C$  reduces the optimal  $v_{SRC}$  to a far smaller value.

The key word of the proposed SRC technique is “Adaptivity.” To keep optimizing  $v_{SRC}$ , the proposed ASRC includes two building blocks, i.e., a  $g_{ds}$ -to- $g_{mb}$  sensor (GTGS) and a body-ripple injector (BRI). The role of the GTGS is to determine the optimum ratio of  $v_{SRC}$  to  $v_R$ ,  $k$ , which is the gain of the ASRC. According to (5), the optimal  $k$  is  $1 + g_{ds}/g_{mb}$ .

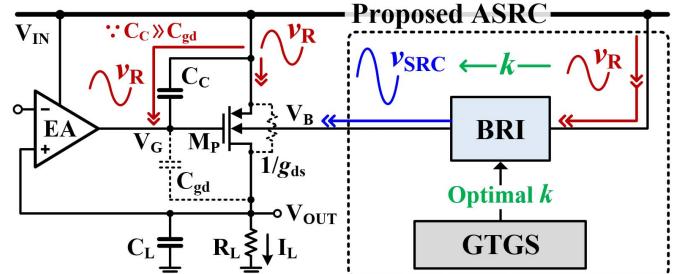


Fig. 5. Conceptual block diagram of the LDO with the proposed ASRC.

As indicated in its name, the GTGS can track the ratio of  $g_{ds}$  to  $g_{mb}$  and use it to determine the optimal  $k$ , as detailed in Section III-B. According to the optimal value of  $k$  from the GTGS, the BRI scales  $v_R$  to  $v_{SRC}$  precisely and injects the ripple to  $V_B$ . The proposed ASRC technique has three major advantages. First, the performance of PSR is robust, since it can continue to optimize the value of  $k$  by the GTGS. Second, it can cancel supply ripples concurrently through the paths of  $C_{gs}$  and  $g_{ds}$  of  $M_P$ . Finally, since the ripples are injected to the body gate, the bandwidth of the SRC can be extended significantly.

#### B. Design of the $g_{ds}$ -to- $g_{mb}$ Sensor (GTGS)

As mentioned in Section III-A, the role of the GTGS is to track the ratio of  $g_{ds}$  to  $g_{mb}$  in (5) in a real-time fashion. Fig. 6 shows the schematics of the GTGS, which consists of three stages. Each stage includes a sensing amplifier ( $SA_N$ ), where  $N$  is the stage number. Since the GTGS obtains the ratio of  $g_{ds}$  to  $g_{mb}$  from dc operations, each  $SA_N$  consumes very little power, which is detailed in Section IV-B. To reproduce the ratio of  $g_{ds}$  to  $g_{mb}$  of  $M_P$ , the first stage includes a replica transistor of  $M_P$  with a scaled-down size  $M_{PR1}$ . The aspect ratio of  $M_{PR1}$  is 1/500 of  $M_P$ , and it shares  $V_G$  of  $M_P$ . Since the drain voltage of  $M_{PR1}$  is fixed to be  $V_{OUT}$  of  $M_P$  (i.e.,  $V_{REF}$  at dc) by the  $SA_1$ , the drain current of  $M_{PR1}$ , i.e.,  $I_{D1}$ , is scaled to  $I_L/500$ . Thus, the absolute values of  $g_{ds}$  and  $g_{mb}$  of  $M_{PR1}$  are reduced to 1/500, but the ratio of  $g_{ds}$  to  $g_{mb}$  of  $M_{PR1}$  is still identical to that of  $M_P$ . The second stage of the GTGS has another scaled-down-sized replica transistor,  $M_{PR2}$ , which is identical to  $M_{PR1}$ . Due to the regulation by  $SA_1$  and  $SA_2$ , the drain current of  $M_{PR2} I_{D2}$  is fixed to be  $I_{D1}$ , and thus,  $I_L/500$ . Different from the first stage, the second stage includes a series resistor  $R_1$ , which causes a slight increase in the drain voltage of  $M_{PR2}$  by  $\Delta V_D$ . Despite the difference of the bias point, since  $I_{D2}$  is forced to be the same as  $I_{D1}$ ,  $SA_2$  should lower the body voltage of  $M_{PR2}$ ,  $V_{B2}$ , by  $\Delta V_B$  to compensate for the effect of the channel-length modulation due to  $R_1$ . Since  $\Delta V_D$  is very small because of a small  $I_{D2}$ , we can assume the ratio of  $g_{ds}$  to  $g_{mb}$  of  $M_{PR2}$  is sufficiently close to that of  $M_{PR1}$ . Based on this process of the second stage, we can represent the ratio of  $g_{ds}$  to  $g_{mb}$  as

$$\Delta I_{D2} = g_{ds} \Delta V_D - g_{mb} \Delta V_B = 0 \quad (6)$$

and, thus

$$g_{ds} : g_{mb} = \Delta V_B : \Delta V_D. \quad (7)$$

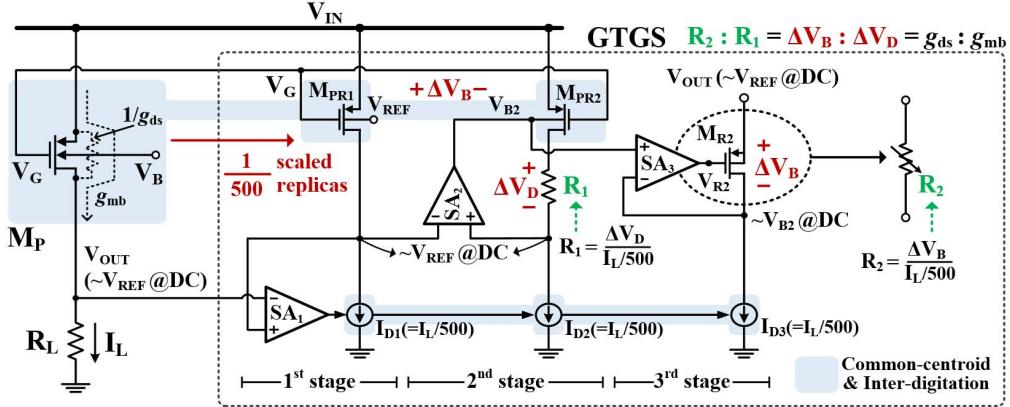
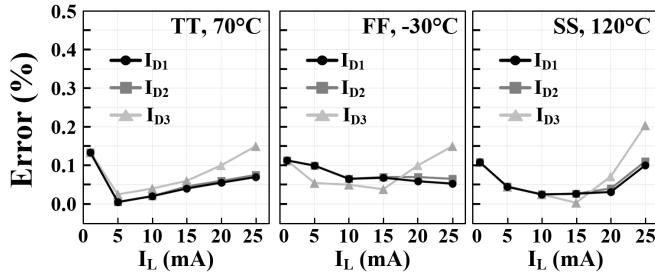


Fig. 6. Schematics and operation of the GTGS.

Fig. 7. Errors in  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$  from post-layout corner simulations.

The third stage has a transistor  $M_{R2}$ . Since  $M_{R2}$  operates in the deep-triode region, it is supposed to function as a variable resistor, of which the effective resistance is  $R_2$ . The source of  $M_{R2}$  is connected to  $V_{OUT}$ , i.e.,  $V_{REF}$  at dc, and its drain voltage is regulated by the  $SA_3$  as  $V_{B2}$ , i.e.,  $V_{REF} - \Delta V_B$  at dc. Thus, the value of  $R_2$  near dc can be represented as  $\Delta V_B / I_{D3}$ . As a result, the ratio of  $g_{ds}$  to  $g_{mb}$  in (7) can be expressed with the ratio of  $R_2$  to  $R_1$  as

$$R_2 : R_1 = \Delta V_B / I_L / 500 : \Delta V_D / I_L / 500 = g_{ds} : g_{mb}. \quad (8)$$

Even though the drain voltage of  $M_{R2}$  is slightly lower than  $V_{REF}$ ,  $I_{D3}$  is almost the same as  $I_L / 500$ , since the current mirrors for  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$  have very high output impedances (i.e., approximately  $10 \text{ M}\Omega$ ) by using cascode configurations with a large gate length (i.e.,  $1 \mu\text{m}$ ). To estimate possible errors of  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$ , post-layout simulations were performed in different corners. As shown in Fig. 7, while  $I_L$  changed from 1 to 25 mA, the errors in  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$ , i.e., the deviations from  $I_L / 500$ , were restricted to less than 0.2%.

Since the scaled-down-sized replica transistors and the sensing amplifiers can track the changes in the operating points of  $M_P$  in a real-time fashion, the GTGS can continue to obtain the updated ratio of  $g_{ds}$  to  $g_{mb}$  despite PVT variations and changes in  $I_L$  and  $V_{DO}$ .

### C. Design of the BRI

Fig. 8 shows the schematics of the BRI, which is based on a non-inverting amplifier with an  $RC$ -network consisting of

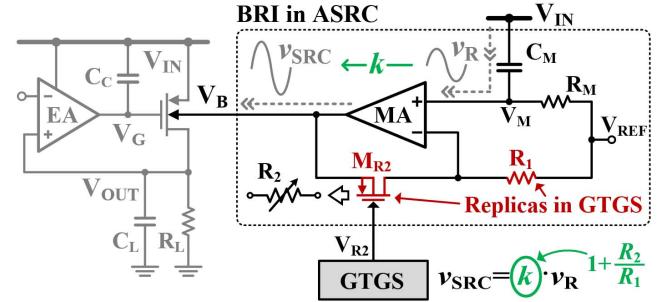


Fig. 8. Schematics and operation of the BRI.

$R_M$  and  $C_M$ . The non-inverting amplifier included a mixing amplifier (MA) and a feedback network  $R_1$  and  $R_2$ . Through the  $RC$ -network, the positive input of the MA  $V_M$  has an ac component of  $v_R$  on a dc-bias voltage of  $V_{REF}$ . The non-inverting amplifier amplifies  $v_R$  coupled through  $V_M$  by  $1 + R_2 / R_1$ , and injects it to  $V_B$ . The dc voltage of the SRC ripple is regulated as  $V_{REF}$ . The feedback network consists of the replicas of  $R_1$  and  $M_{R2}$  of the GTGS, and the replica- $M_{R2}$  shares the gate voltage  $V_{R2}$  from the GTGS. Therefore,  $v_R$  always can be amplified by the optimal  $k$ ,  $1 + g_{ds} / g_{mb}$ , according to (8). As explained in Section III-A, due to the use of  $C_C$ , the maximum  $k$  is reduced to less than four. Thus, in normal cases, the source-body diode of  $M_P$  should not be turned on by injected ripples (or  $v_{SRC}$ ) [13]. However, if the amplitude of supply ripples (or  $v_R$ ) increased abnormally, such as more than 200 mV, the amplitude of  $v_{SRC}$  would grow theoretically to a level that could turn on the diode. However, since the MA has a limited range of the output swing, such a large  $v_{SRC}$  cannot be injected to the body of  $M_P$ . In this case, although the effect of the ASRC technique could be degraded due to the deviation of  $k$  from the optimal value, the source-body diode of  $M_P$  can be ensured not to be turned on. The design of the MA is detailed in Section IV. The swing of  $v_{SRC}$  also can cause ac current between  $V_B$  and  $V_{REF}$ . This ac current can be minimized by increasing the resistance of  $R_1$  and  $M_{R2}$  in the BRI in the same proportion. To mitigate the non-linearity of the on-resistance of  $M_{R2}$  caused by the swing of  $v_{SRC}$ ,  $M_{R2}$  was designed using a low threshold voltage device having a small aspect ratio.

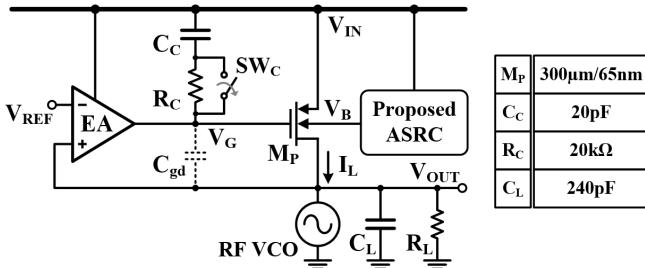


Fig. 9. Overall architecture of a prototype LDO.

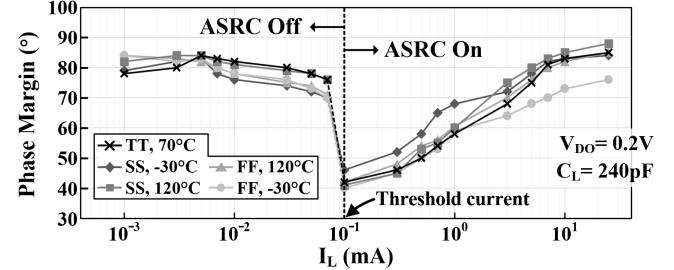
As shown in Fig. 8, the effect of the ASRC is valid at frequencies above the cutoff frequency of the  $RC$ -network  $\omega_M$ . As mentioned in Section I, the objective of the ASRC technique is to improve the PSR at frequencies above  $\omega_G$  and suppress the PSR hump of typical gate-pole-dominant LDOs. Thus,  $\omega_M$  must be smaller than the minimum  $\omega_G$ . In this paper,  $\omega_M$  was designed as approximately 6.5 kHz. Corner simulations confirmed this value was smaller than the minimum  $\omega_G$ , which occurred when the output impedance of the EA was the largest.

Not to use an additional reference voltage, the BRI was designed to share the same reference voltage, i.e.,  $V_{REF}$ , with the EA. However, this design could limit the valid range of  $V_{DO}$ ; if  $V_{DO}$  increased over 0.5 V, a too low dc voltage of  $V_B$  would turn on the body diode. This concern can be removed using an additional reference voltage, because the reference voltage used for the BRI should not be fixed at  $V_{REF}$ . If the design is modified to use another reference voltage, for example, 1.0 V, the dc voltage of  $V_B$  must be fixed at 1.0 V, independent of  $V_{REF}$  and  $V_{DO}$ ; thus, the foregoing issue can be resolved. Since the use of this additional voltage does not affect the capability of the ASRC technique, the proposed LDO can maintain almost the same PSR performance.

#### IV. IMPLEMENTATION OF AN LDO USING THE PROPOSED ASRC

##### A. Overall Architecture of the LDO With the Proposed ASRC

Fig. 9 shows the overall architecture of a prototype LDO in which the proposed ASRC is used. The 20-pF  $C_C$  is implemented using a metal-insulator-metal (MIM) capacitor. A switchable 20-k $\Omega$  resistor  $R_C$  is placed between  $C_C$  and  $V_G$  in parallel with a pass-gate switch  $SW_C$ . In the normal operation,  $R_C$  is bypassed due to the switch, and supply ripples are transferred directly to  $V_G$  through  $C_C$ .  $R_C$  becomes effective only when  $I_L$  is very small, such as less than 100  $\mu$ A. The role of  $R_C$  is explained later in this section. The increase in the capacitance of  $C_C$  due to the proposed ASRC technique causes the degradation in the transient response of the LDO (as well as the increase in the silicon area). This degradation is mainly because the  $\omega_{UGF}$  of the LDO and the slew rate of the EA are reduced by the increase in the capacitance of  $C_C$ . However, the overshoot/undershoot and the settling time of the LDO in this paper are still small enough to be used for target applications, i.e., some RF and analog circuits, which do not require such a fast turning on and off [28]. The measured values of the transient response are presented

Fig. 10. Simulated phase margins with respect to  $I_L$  in different corners.

in Section VI. In case some improvement of the transient response is demanded, the use of an additional technique, such as a super-source follower [8] in the EA, an overshoot reduction technique [18], or a slew-enhancement technique [26] can be considered.

At the output of the LDO, a 240-pF MOS capacitor of  $C_L$  is used to suppress supply ripples at very high frequencies above the bandwidth of the ASRC  $\omega_{BW,ASRC}$ . The value of 240 pF is the maximum capacitance of  $C_L$ , to ensure the phase margin more than 40°, when  $I_L$  is 100  $\mu$ A and the ASRC is used. When  $I_L$  is 1 mA, the maximum  $C_L$  can be increased up to 540 pF. Fig. 10 shows the phase margins of the LDO's regulating loop in different corners, which were obtained from post-layout simulations. When  $I_L$ s were 0.1, 1, and 25 mA with 0.2-V  $V_{DO}$  and 240-pF  $C_L$ , the worst-case phase margins were 40°, 58°, and 76°, respectively. For gate-pole-dominant LDOs, in general, the degree of the stability is degraded as  $I_L$  becomes very small, such as approaching zero [18]. To resolve this problem, a general method is to activate an additional LHP zero, when  $I_L$  is smaller than a predefined threshold current [19]. In this paper, we set the threshold current as 100  $\mu$ A. In this case,  $SW_C$  is turned off so that  $R_C$  becomes effective, generating a 400-kHz LHP zero  $\omega_Z$ . Due to this LHP zero, the LDO can have a sufficient phase margin until  $I_L$  decreases to 1  $\mu$ A. Since  $R_C$  limits the effect of the ASRC, it would be better to turn off the ASRC to minimize the quiescent current. Note that, when  $I_L$  is very small,  $\omega_{OUT}$  is also located at a very low frequency. Since this low-frequency  $\omega_{OUT}$  can naturally suppress the PSR hump, the LDO can achieve high PSR at high frequencies without the use of the ASRC. When  $I_L$  was 1  $\mu$ A, the phase margin was 78° at the worst corner. Even without the use of the ASRC, the LDO still achieved a PSR of more than  $-24$  dB around  $\omega_{UGF}$ . The design of this paper did not include a circuit to detect whether  $I_L$  is smaller or larger than the threshold current, but an on-chip replica- $M_P$ -based load-current sensor [18] can be easily designed with minimal increases in silicon area and power consumption. To evaluate the effectiveness of the ASRC for a practical RF circuit, a test voltage-controlled oscillator (VCO) is integrated as the load of the LDO.

##### B. Operational Amplifiers

The proposed LDO included one EA, three SAs, and one MA. Since the proposed ASRC can improve high-frequency PSR, the requirement of the bandwidth of the EA can be relaxed. The EA was designed based on a negative- $g_m$

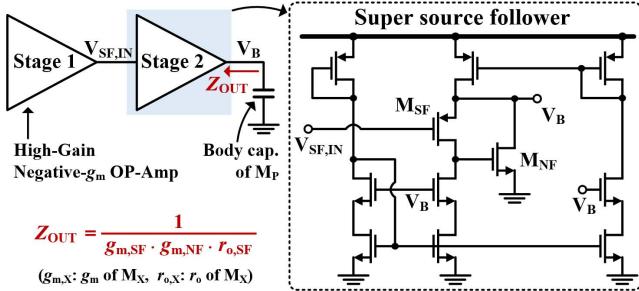


Fig. 11. Schematics of the MA.

operational amplifier (OP-Amp) architecture [29] that can achieve a high dc gain rather than a wide bandwidth. According to post-layout simulation, the EA had a 60-dB voltage gain within a 10-kHz bandwidth, when the current consumption was 8  $\mu\text{A}$ . As mentioned in Section III, since the role of the SAs is to fix the dc-operation points of  $M_P$ ,  $M_{\text{PR}1}$ ,  $M_{\text{PR}2}$ , and  $M_{\text{R}2}$ , they also must have a high voltage gain near dc rather than a wide bandwidth. The SAs have a folded-cascode topology with a gain-boosting technique. Each SA consumed 1.5  $\mu\text{A}$  and had a dc gain of 70 dB and a bandwidth of 1 kHz. The input offsets of the SAs could affect the accuracy of the GTGS. Among the three SAs in Fig. 6, the input offset of SA<sub>2</sub> is the most critical, since it can cause a direct impact on the mismatch between the ratios of  $g_{\text{ds}}$  to  $g_{\text{mb}}$  and  $\Delta V_B$  to  $\Delta V_D$ . To minimize the input offset, the input pair of SAs was designed to have a large dimension. According to Monte Carlo simulations, one-signal value of the input offset was approximately 0.6 mV. The impact of this input offset increases, as the value of  $I_L$  decreases. So, the mismatch caused by the 1-sigma input offset is less than 3% when  $I_L$  is more than 1 mA, but it increases to 30% when  $I_L$  is reduced to 0.1 mA. However, since the PSR hump is originally small when  $I_L$  is small (as explained in Section I), the PSR can be still high even if the accuracy of the GTGS is degraded due to the input offset of the SAs. The measured PSR when  $I_L$  is 0.1 mA is provided in Section VI.

Different from the EA and the SAs, the MA must achieve a high-gain-bandwidth product (GBW) to maximize the frequency range, in which the ripple cancellation effect of the ASRC is valid. Fig. 11 shows that the MA has two cascaded stages. The first stage of the MA has a negative- $g_m$  OP-Amp to achieve a high dc gain. Then, to prevent the output impedance from generating a low-frequency pole along with the capacitance of  $V_B$  of  $M_P$ , the second stage was designed to have a super-source follower that can greatly reduce the output impedance without consuming large power [30]. Also, since the parasitic capacitance of  $V_B$  is smaller than that of the  $V_G$ , the GBW of the MA can be extended further. According to the simulation, the MA achieved a dc gain of 60 dB and a GBW of 1 GHz when it consumed 135  $\mu\text{A}$ . The power consumption of the MA takes a significant portion of the entire quiescent power of the LDO. Especially when  $I_L$  is a relatively small, such as less than 1 mA, it can be a burden. However, since we do not need a large improvement of the PSR when  $I_L$  is small (due to an originally small PSR hump), by controlling the bias of the MA adaptively, we can reduce the power consumption of

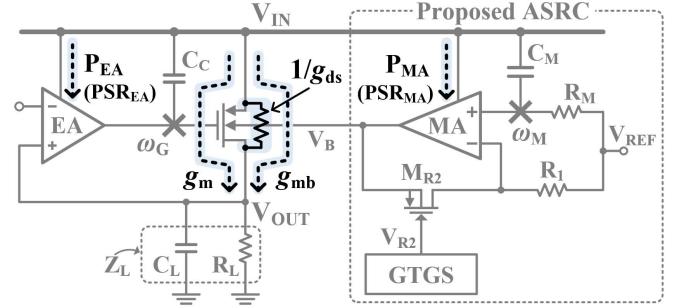


Fig. 12. Supply-noise coupling paths of the proposed LDO.

the MA at the expense of the decrease in the GBW. According to simulation, when  $I_L$  is 1 mA and the quiescent current is reduced to 50  $\mu\text{A}$ , the degradation in PSRs at frequencies over 10 MHz are less than 5 dB. (PSRs at frequencies less than 10 MHz are almost unaffected.)

Due to the multiple transistor stack between the  $V_B$  and the ground, the dc level of  $V_B$  cannot go below 0.5 V. However, this limited range of the output swing even can help prevent too large  $v_{\text{SRC}}$  from being injected into the body gate and turning on the source-body diode of  $M_P$  in abnormal cases.

## V. ANALYSIS OF PSR AND NOISE OF THE LDO

Fig. 12 shows the coupling paths of supply noise to  $V_{\text{OUT}}$  in the proposed LDO, through the  $g_{\text{ds}}$  of  $M_P$  and additional paths from amplifiers ( $P_{\text{EA}}$  and  $P_{\text{MA}}$ ). As mentioned in Section III-A, the coupling path through  $C_{\text{gs}}$  can be ignored due to  $C_C$ . PSR<sub>X</sub> denotes the PSR of each amplifier. Since the proposed ASRC injected the scaled supply ripples to  $V_B$ , we also must consider the coupling path through  $g_{\text{mb}}$ . By superposing the transfer functions of all of the paths from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$ , the overall PSR of the LDO in a frequency range from  $\omega_M$  to  $\omega_{\text{BW},\text{ASRC}}$ , PSR<sub>LDO</sub>, can be represented as [20], [21]

$$\text{PSR}_{\text{LDO}}(s) = \frac{V_{\text{OUT}}(s)}{V_{\text{IN}}} \approx \frac{g_{\text{mb}}(1 - k_{\text{REAL}}) + g_{\text{ds}} - \varepsilon_{\text{PSR}}}{g_m \cdot \frac{A_{\text{EA}}}{1+s/\omega_G} + g_{\text{ds}} + 1/Z_L} \quad (9)$$

where

$$\begin{aligned} k_{\text{REAL}} &= k_{\text{OPT}}(1 \pm \varepsilon_D) \\ &= (1 + g_{\text{ds}}/g_{\text{mb}}) \cdot (1 \pm \varepsilon_D) \quad (\varepsilon_D > 0) \end{aligned} \quad (10)$$

and

$$\varepsilon_{\text{PSR}} = \frac{g_m \cdot \text{PSR}_{\text{EA}}}{1 + s/\omega_G} + g_{\text{mb}} \cdot \text{PSR}_{\text{MA}} \quad (11)$$

where  $k_{\text{OPT}}$  is the optimal  $k$ , i.e.,  $1 + g_{\text{ds}}/g_{\text{mb}}$ .  $k_{\text{REAL}}$  is the practical gain of the ASRC, which includes an error  $\varepsilon_D$ .  $\varepsilon_{\text{PSR}}$  represents an error caused by limited PSRs of the EA and the MA. According to (9), when  $k_{\text{REAL}}$  is equal to  $k_{\text{OPT}}$  (i.e.,  $\varepsilon_D$  is zero) and  $\varepsilon_{\text{PSR}}$  is zero, ideally,  $\text{PSR}_{\text{LDO}}$  in (9) approaches zero. However, as  $\varepsilon_D$  and  $\varepsilon_{\text{PSR}}$  increase due to non-idealities of the ASRC and the amplifiers, the improvement of  $\text{PSR}_{\text{LDO}}$  by the proposed ASRC becomes less effective. To minimize  $\varepsilon_{\text{PSR}}$ , the EA was designed to have  $\text{PSR}_{\text{EA}}$  less than -40 dB near dc when  $\omega_G$  was 10 kHz. This  $\text{PSR}_{\text{EA}}$

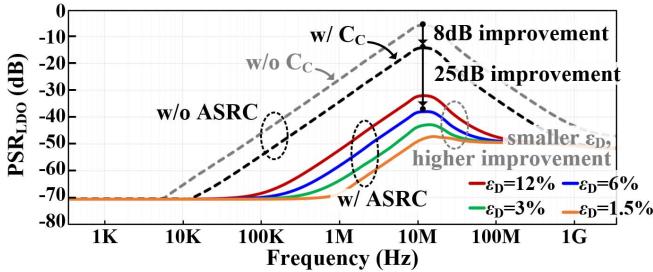


Fig. 13. PSR without the ASRC and PSRs with the ASRC from (9) when the values of  $\epsilon_D$ s were between 1.5% and 12% (and  $\epsilon_{PSR}$  was zero).

degrades, as the frequency increases over the unity-gain bandwidth (UGB) of the EA, which is approximately 40 MHz. According to (11), however, since a 10-kHz pole of  $\omega_G$  is capable of suppressing the supply ripples through the supply of the EA at these high frequencies, no degradation of the overall PSR due to the EA is observed even after the 40-MHz offset. In addition, the MA was designed to have  $PSR_{MA}$  less than  $-50$  dB up to 1 GHz. Thus, the impact of  $\epsilon_{PSR}$  on  $PSR_{LDO}$  in (9) is insignificant with respect to  $\epsilon_D$ .

Fig. 13 shows the plot of (9) using MATLAB, when  $\epsilon_D$  changes between 1.5% and 12.0% and  $\epsilon_{PSR}$  is fixed at zero.  $V_{DO}$ ,  $I_L$ , and  $C_L$  are 0.2 V, 10 mA, and 240 pF, respectively. Small signal parameters of  $A_{EA}$  and  $\omega_G$  in (9) were obtained from post-layout simulations at the typical corner of [TT, 70 °C]. In Fig. 13, the two dashed lines in gray and black indicate  $PSR_{LDO}$ s, without and with  $C_C$ , respectively, when the ASRC is turned off. They show the use of  $C_C$  results in 8-dB improvement of PSR. In these cases,  $k_{REAL}$  is represented as 1, implying the case when the body gate is tied to the source. When  $\epsilon_D$  is 1.5% (orange line),  $PSR_{LDO}$  is improved dramatically. Around 10 MHz, near  $\omega_{UGF}$ , the amount of the improvement in  $PSR_{LDO}$  is more than 35 dB. As shown in Fig. 13, the PSR improvement is reduced as  $\epsilon_D$  increases, but it is still 25 dB even when  $\epsilon_D$  is as high as 6%. The major cause of  $\epsilon_D$  is a mismatch between the ratio of  $g_{ds}$  to  $g_{mb}$  of  $M_P$  and those of  $M_{PRS}$  in the GTGS. Other causes are local mismatches between resistors in the GTGS and their replicas in the BRI. In this paper, as shown in Fig. 6, common-centroid and inter-digitation techniques were used in the layout to alleviate the above causes of  $\epsilon_D$ . A mismatch between  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$  is another cause that is generated by a drain voltage mismatch between  $M_{PR1}$ ,  $M_{PR2}$ , and  $M_{R2}$  in the GTGS. However, the current mirrors at the drains of  $M_{PR1}$ ,  $M_{PR2}$ , and  $M_{R2}$  have very high output impedances (i.e., approximately 10 MΩ) due to cascode configurations. Thus, the current mismatch between  $I_{D1}$ ,  $I_{D2}$ , and  $I_{D3}$  was reduced to less than 0.2% even in the worst case, and it provides a negligible impact on the increase in  $\epsilon_D$ . Fig. 14 shows the results of Monte Carlo simulations to estimate  $\epsilon_D$ s in different corners. For each set of five different corners, [TT, 70 °C], [SS, 120 °C], [FF, -30 °C], [SS, -30 °C], and [FF, 120 °C], we obtained 1000 samples (i.e., the total of 5000 samples). Fig. 14 shows that the standard deviation was 1.63% from the average of 5.21%, when  $V_{DO}$ ,  $I_L$ , and  $C_L$  were 0.2 V, 10 mA, and 240 pF, respectively. Fig. 14 shows

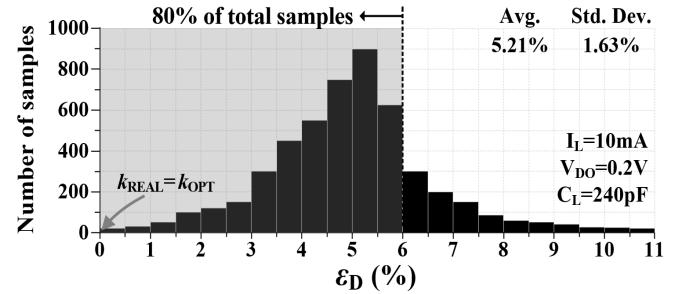


Fig. 14. Variation of  $\epsilon_D$  from Monte Carlo simulations.

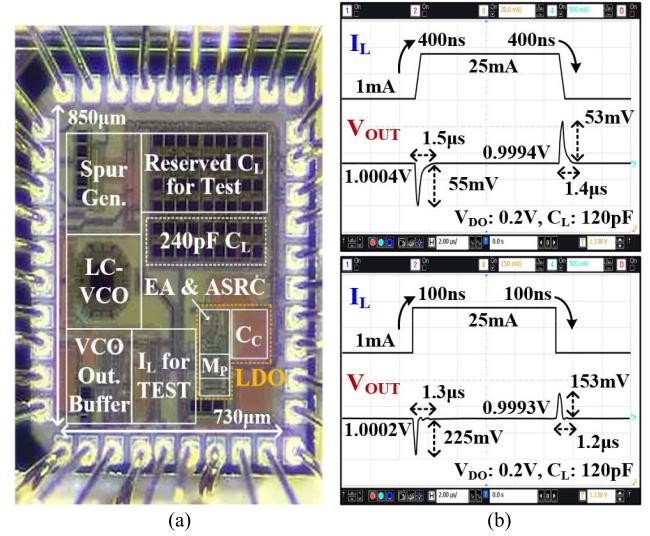
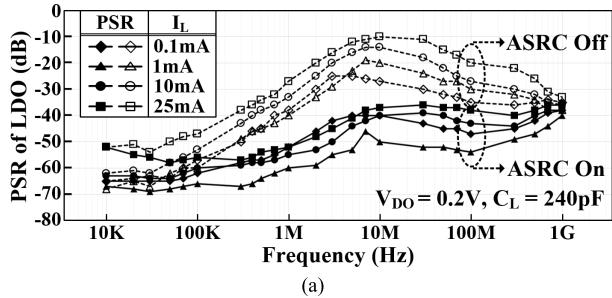


Fig. 15. (a) Chip micrograph. (b) Measured load-transient responses.

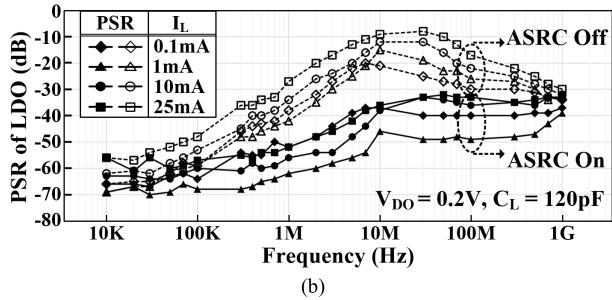
that more than 80% of the samples had an  $\epsilon_D$  less than 6%, which corresponds to an improvement of 25 dB in the PSR.

## VI. EXPERIMENTAL RESULTS

The LDO was fabricated in a 65-nm CMOS process. As shown in Fig. 15(a), the active area was 0.087 mm<sup>2</sup>, including the 240-pF  $C_L$ . The LDO had the  $V_{IN}$  of 1.2 V. The quiescent current  $I_Q$  was proportional to the amount of  $I_L$  due to the scaled-down-sized replica transistors of  $M_P$ . It changed between 153.5 and 297.5 μA, as  $I_L$  increased from 1 to 25 mA. When  $I_L$  was less than 100 μA,  $I_Q$  decreased to 8 μA, since the ASRC was deactivated. Fig. 15(b) shows the transient responses of  $V_{OUT}$ , when the transition of  $I_L$  occurred between 1 and 25 mA. When the transition time  $T_{TR}$  was 400 ns, undershoot and overshoot were measured as 55 and 53 mV, respectively. When  $T_{TR}$  was 100 ns, they were 225 and 153 mV, respectively. In this paper, we used 20-pF  $C_C$ , but to reduce the magnitude of undershoot and overshoot, the value of  $C_C$  can be decreased at the expense of PSR around 10 MHz. To measure the PSR of the LDO, we applied the supply voltage with ac ripples to  $V_{IN}$ . The test ripples had an amplitude of 80 mV, and the frequency changed from 10 kHz to 1 GHz. Fig. 16(a) shows the measured PSRs, when  $I_L$  changed from 0.1 to 25 mA while  $V_{DO}$  and  $C_L$  were fixed at 0.2 V and 240 pF, respectively. When the ASRC was turned off, PSR humps were found at the frequencies

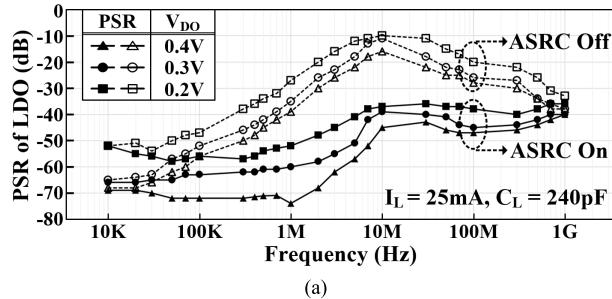


(a)

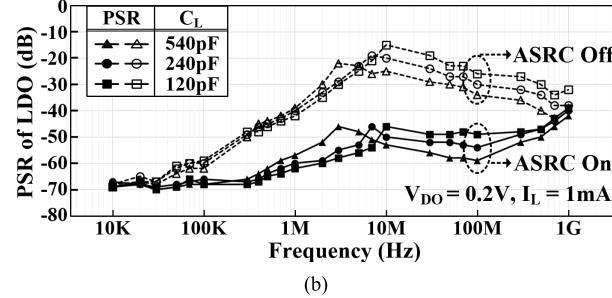


(b)

Fig. 16. Measured PSRs while  $I_L$  changed from 0.1 to 25 mA, when the ASRC was turned on or off. (a)  $C_L$  was 240 pF. (b)  $C_L$  was 120 pF.



(a)



(b)

Fig. 17. Measured PSRs when the ASRC was turned on or off as (a)  $V_{DO}$  decreased from 0.4 to 0.2 V and (b)  $C_L$  decreased from 540 to 120 pF.

around 10 MHz. However, when the ASRC was turned on, PSRs were improved significantly, especially at frequencies between 100 kHz and 1 GHz; thus, the LDO achieved PSRs less than  $-36$  dB at all frequencies from 10 kHz to 1 GHz. We note that when  $I_L$  was  $100 \mu\text{A}$ , PSRs were less than  $-26$  dB at all frequencies, even when the ASRC was turned off to reduce  $I_Q$ . Fig. 16(b) shows the measured PSRs, when  $C_L$  was reduced to 120 pF. Due to the ASRC, the PSRs were maintained to be less than  $-31$  dB at all frequencies. As shown in Fig. 17(a), even for different  $V_{DOS}$  the ASRC constantly achieved the significant improvement of PSR by suppressing PSR humps. Fig. 17(b) shows the measured PSRs for different  $C_L$ s from 120 to 540 pF, when  $I_L$  and  $V_{DO}$  were fixed at

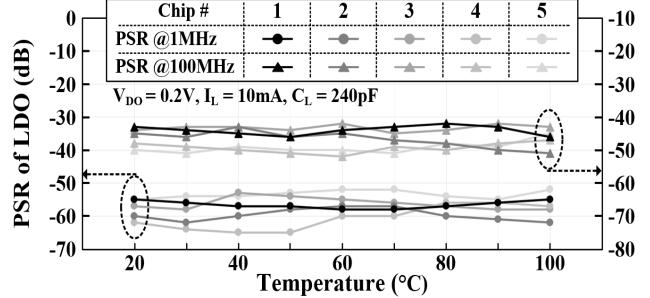


Fig. 18. Measured PSRs across temperatures for five different chips.

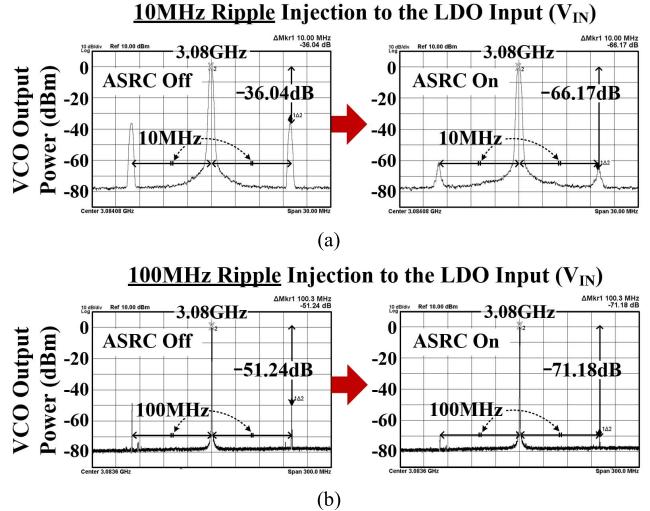


Fig. 19. Measured spurs of the output of the test VCO, when the ASRC was turned on or off. (a) 10-MHz ripple was injected to  $V_{IN}$ . (b) 100-MHz ripple was injected to  $V_{IN}$ .

1 mA and 0.2 V, respectively. (540 pF is the maximum  $C_L$ , when  $I_L$  is 1 mA.) When the ASRC was disabled, the PSR at the 10-MHz offset was  $-14$  dB, when  $C_L$  was 120 pF. However, when the ASRC was turned on, the PSR at the same offset was improved by more than 30 dB. However, when the ASRC was turned on, the PSR at the same offset was improved by more than 30 dB. Fig. 16(a) and (b) shows the PSR at low frequencies, such as 10 kHz, is degraded as  $I_L$  increases. A similar trend is observed also in Fig. 17(a), when  $V_{DO}$  decreases. This reduction in the low-frequency PSR is because the loop gain at low frequencies decreases due to the reduction of the intrinsic gain of  $M_P$ . Figs. 16(a) and (b) and 17(b) also show that the PSR at high frequencies above 10 MHz is better for a smaller  $I_L$  or a larger  $C_L$ . This is because the location of  $\omega_{OUT}$  is pulled toward a lower frequency, as  $I_L$  decreases or  $C_L$  increases. Fig. 18 shows the variations of PSRs measured on five different chips, when the temperature changed from 20 °C to 100 °C. In these measurements,  $I_L$  and  $V_{DO}$  were 10 mA and 0.2 V, respectively. Across temperatures, the PSRs at two different offsets were relatively constant in all test chips, which verified the robust operation of the proposed ASRC technique. To verify the feasibility of the proposed idea in a more practical situation, the LDO was tested to supply power to the VCO, integrated in the same die. Fig. 19(a) and (b) shows the suppression of the sideband spurs of the VCO due to the proposed ASRC. As shown

TABLE I  
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART EXTERNAL CAPACITORLESS LDOs

		This work	CICC'11 [25]	TCAS2'12 [24]	JSSC'14 [26]	TVLSI'17 [20]	TCAS1'16 [12]
Process (nm)		65	180	130	180	40	65
Dominant pole		Gate dominant					Output dominant
Technique		ASRC		SRC	SRC	Gain stabilizer	Wideband EA
$V_{IN}$ (V) / $V_{DO}$ (V)		1.2 / 0.2		1.8 / 0.3	1.2 / 0.2	1.8 – 2.6 / 0.2	1.1 / 0.1
$I_{L,MAX}$ (mA)		25		25	50	50	200
Worst PSR(dB)	$I_L$ (mA)	0.1 – 25		5 – 20	0.05 – 50	1 – 50	0 – 200
	$C_L$ (pF)	120	240	25	20	100	130
	1 MHz	-52	-52	-40	-40	-70	-60
	10 MHz	-36	-37	-22	-15	-37	-35
	100 MHz	-33	-37	-12	NA	NA	-23
1 GHz		-31	-36	NA	NA	NA	-16
Adaptability for PSR improvement		Y		N	N	Y	Y
Amplitude of test ripples (mV)		80		30	20	100	80
Load reg. ( $\mu$ V/mA) / Line reg. (mV/V)		42 / 3.8		NA / NA	55 / 8.1	140 / NA	19 / 0.75
$I_Q$ ( $\mu$ A)		8 – 297.5		300	37	55 – 555****	275
$T_{TR}$ (ns) / $K^*$		100 / 500		NA	200 / 1000	100 / 500	100 / 500
$T_{SETTLE}$		1.5		NA	0.4	6	0.8
Undershoot or overshoot, $\Delta V_{OUT}$ (mV) @ $T_{TR}$ (ns)		225 @100 (55 @400)		NA	56 @200	120 @100	124 @100
$FOM_{TR1}^{**}$ (V)		1.39		NA	0.041	0.68	0.085
$FOM_{TR2}^{***}$ (ns)		13.9m		NA	16.6 $\mu$	2.67m	85.25 $\mu$
Active area ( $\text{mm}^2$ )		0.087****		0.041	0.018	0.14	0.008
							0.023

\*K:  $T_{TR}$  used in the measurement /the smallest  $T_{TR}$  among the designs for comparison. \*\* $FOM_{TR1}$ :  $K \cdot \Delta V_{OUT} \cdot I_Q / \Delta I_L$  [18].

\*\*\* $FOM_{TR2}$ :  $C_L \cdot \Delta V_{OUT} \cdot I_Q / \Delta I_L^2$  [31]. \*\*\*\*Including the area of 240-pF  $C_L$ . \*\*\*\*\*Including quiescent current of a scale-down-sized replica-pass-transistor in the PSR enhancer, where the drain current was approximately equal to  $I_L / 100$ .

in Fig. 19(a), when a 10-MHz ripple (-30 dBm) was applied to  $V_{IN}$ , the ASRC improved the PSR by more than 30 dB. As shown in Fig. 19(b), it also provided almost 20-dB PSR improvement at the 100-MHz offset. The amounts of the decrease in the level of the spurs by the ASRC in Fig. 19(a) and (b) precisely correspond to those of PSR improvement in Fig. 16. Table I compares the performance of the LDO in this paper with those of the state-of-the-art external capacitorless LDOs. As shown in Table I, different from other LDOs, the proposed LDO obtained high PSRs up to a 1-GHz offset. The LDOs in [20] and [26] had higher PSRs at a relatively low offset, i.e., 1 MHz, but they are not appropriate to applications, such as RF transceivers that require PSRs up to high-frequency offsets. Moreover, the proposed ASRC LDO has a unique capability to maintain such high PSR robustly, despite the changes in  $I_L$  and  $V_{DO}$  as well as PVT variations. The measurement data used for  $FOM_{TR1}$  and  $FOM_{TR2}$  were obtained when  $C_L$  and  $T_{TR}$  were 120 pF and 100 ns.

## VII. CONCLUSION

In this paper, we proposed an external capacitorless gate-pole-dominant LDO that provided high PSRs at all low-to-high frequencies. Using the ASRC technique, the PSR hump of conventional gate-pole-dominant LDOs can be suppressed significantly. The proposed ASRC technique is capable of cancelling

supply ripples through  $g_{ds}$  as well as through  $g_m$  of  $M_P$ . Since the ASRC continues to optimize the magnitude of the injecting ripples, high PSR can be maintained firmly, despite PVT variations as well as during the changes of  $I_L$  and  $V_{DO}$ . In the measurements, the proposed LDO achieved PSRs less than -36 dB at all frequencies from 10 kHz to 1 GHz.

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