High Power-Supply-Rejection (PSR) Current-Mode Low-Dropout (LDO) Regulator

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***Abstract*—Modern system-on-a-chip (SoC) solutions suffer from limited on-chip capacitance, which means that the switching events of functionally dense ICs induce considerable noise in the supplies. This ripple worsens the accuracy of sensitive analog electronics, such as ADCs, PLLs, and VCOs, etc. Without dropping a substantial voltage, point-of-load (PoL) low-dropout (LDO) regulators reduce (filter) this noise but only as much as their loop gains and bandwidths allow. This brief presents a 5-mA 1.5-μm bipolar current-mode LDO regulator that, with a higher bandwidth current loop, suppresses higher frequency noise by 49 dB (i.e., power-supply rejection) up to 10 MHz with only 68 nF at the output, which is 20 dB better than its voltage-mode counterpart.**

***Index Terms*—Current mode, dual loops, low-dropout (LDO) regulator, power-supply rejection (PSR), supply noise ripple.**

I. LDO Regulators in Power Management

With the increasing sophistication of portable electronics, the demand for good power supplies is expanding. Supply systems must be accurate and power-efficient to conserve energy and extend battery life, which is why inductor-based converters are so popular. Switching supplies, however, introduce systematic noise that state-of-the-art data converters, radio frequency radios, phase-locked loops, and others cannot sustain, so low-dropout (LDO) linear regulators often postregulate a switched supply to suppress noise without dropping appreciable power [1]–[6], [9]. What noise frequencies an LDO is capable of suppressing depends on its bandwidth, which stability requirements under unpredictable loads (e.g., I_L, R_L, R_{ESR}, and C_O in Fig. 1) constrain to below 0.5–1 MHz [2], [7], [8].

This brief presents, discusses, and evaluates a prototyped 1.5-μm bipolar current-mode (dual-loop) LDO that further attenuates the high-frequency ripple switching supplies generate. To that end, Section II reviews power-supply rejection (PSR) performance and summarizes the state of the art in high-PSR LDOs. While Section III introduces and details the stability and the PSR performance of the proposed LDO, Section IV evaluates its achieved experimental performance, and Section V draws relevant conclusions.

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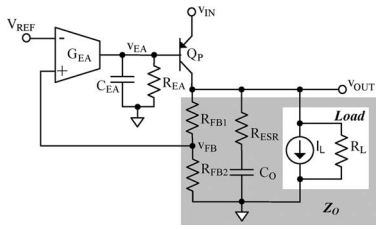

Fig. 1. Typical p-n-p bipolar junction transistor LDO voltage-mode regulator.

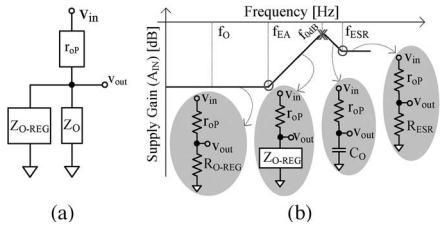

Fig. 2. (a) LDO's PSR model and (b) its corresponding response.

II. Power-Supply Rejection

A. Voltage-Mode Performance

The fraction of supply ripple v_{IN} that reaches v_{OUT} is the voltage-divided (suppressed) translation of v_{IN}, which is supply gain A_{IN} (i.e., v_{OUT}/v_{IN}). Modeling the supply and ground impedance of an LDO, as Fig. 2(a) shows, describes how v_{IN} affects v_{OUT}, which is how PSR manifests in v_{OUT} because PSR is the reciprocal of this v_{IN}/v_{OUT} translation (i.e., PSR is $1/A_{IN}$) [2], [7]. Notice that the impedance from v_{IN} to v_{OUT} is Q_P's small-signal output resistance r_{oP} (from Fig. 1), and v_{OUT}'s ground impedance is (in part) output filter Z_O, which consists of load resistance R_L, output capacitance C_O and its equivalent series resistance R_{ESR}, and feedback resistors R_{FB1} and R_{FB2}. The shunt-feedback loop that an LDO employs to regulate v_{OUT} introduces the other impedance to ground (as $Z_{O\text{-}REG}$) that decreases with increasing loop gains. In other words, the LDO's ability to suppress noise rests on the noise that $Z_{O\text{-}REG}$ shunts to ground, that is, on how low $Z_{O\text{-}REG}$ is (or how high the loop gain is) across frequency.

As a result, supply gain A_{IN} is voltage-divided translation

$$A_{IN} \equiv \frac{v_{OUT}}{v_{IN}} = \frac{Z_O \| Z_{O\text{-}REG}}{r_{oP} + (Z_O \| Z_{O\text{-}REG})}, \tag{1}$$

output filter Z_O is

$$Z_O = (R_{FB1} + R_{FB2}) \| \left(R_{ESR} + \frac{1}{sC_O} \right) \| R_L, \tag{2}$$

and shunt-feedback resistance $Z_{O\text{-}REG}$ is

$$Z_{O\text{-}REG} = \frac{Z_O \| r_{oP}}{LG_V}, \tag{3}$$

where loop gain LG_V is the gain across the feedback loop (i.e., across G_{EA}, Q_P, and $R_{FB1}-R_{FB2}$). A_{IN} is, therefore, low at low frequencies (because LG_V is high) and increases (i.e., deteriorates) past the LDO's internal pole f_{EA} (when LG_V drops). This degradation in PSR continues until LG_V reaches the unity-gain frequency (f_{0dB}) beyond which point C_O and its R_{ESR} dictate how much supply noise shunts to ground [7]. C_O is typically high to shunt more of the noise produced by 1) the supply (for PSR) and 2) sudden load dumps (for accuracy).

B. State of the Art in High-PSR LDOs

While a low-pass filter can attenuate high-frequency noise in v_{IN}, the series filter resistor dissipates considerable power [2], and adding a second LDO in series (which also dissipates considerable power) only helps suppress noise at low frequencies [6]. A common-gate cascode transistor can decouple v_{OUT} from v_{IN} across frequency, but again, the cascode also consumes power [1]. Feed forwarding the supply ripple to Q_P's base (to ensure Q_P's emitter–base terminals sustain the same common-mode ripple) can restrain Q_P's current variations, but tuning it to account for r_{oP} variations requires both considerable real estate and quiescent power [3].

III. Proposed Current-Mode LDO

Improving the PSR at high frequencies, where emerging dc–dc converters typically switch, without losing additional ohmic (dropout) power, amounts to increasing the impedance to the supply [between v_{IN} and v_{OUT} in Fig. 2(b)] and/or decreasing the impedance (from v_{OUT}) to ground near these frequencies. LDOs achieve good low-frequency PSR because shunt feedback reduces ground impedance $Z_{O\text{-}REG}$ at low-to-moderate frequencies. Extending the frequencies for which $Z_{O\text{-}REG}$ remains low without compromising stability, however, is difficult [2], [7], [8]. This brief instead proposes to insert a higher frequency series (current) sampling loop that, without increasing dropout voltage, increases the impedance to the supply at higher frequencies, where the state of the art fails. In other words, series feedback regulates output transistor Q_P's current and increases its (supply) impedance just like shunt feedback regulates v_{OUT} and decreases ground impedance.

The aim of the series-sampling loop is to transform Q_P into a current source only at higher frequencies (because shunt feedback already performs well at lower frequencies). The proposed circuit shown in Fig. 3 achieves this by 1) sampling Q_P's current with sense transistor Q_S's current i_S (via g_{mS}), 2) high-pass-filtering i_S with transconductor $G_I(s)$, and 3) shunt-mixing $G_I(s)$'s output i_{FB} into the voltage loop (with i_{REF}). As a result, because i_{FB} is negligibly small at low frequencies, the voltage loop alone defines v_{EA} to control Q_P. At higher frequencies, the voltage loop sets dynamic current reference i_{REF} against which the faster current loop regulates i_{FB} to control Q_P's current i_P to supply the load. Notice that transconductor G_V samples v_{OUT}, and amplifier A_D buffers v_{EA} (to decouple Q_P's large parasitic capacitance from v_{EA}).

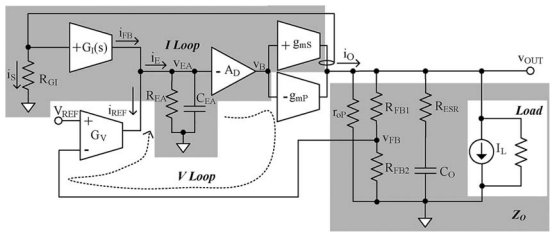

Fig. 3. Small-signal model of the proposed high-PSR current-mode LDO.

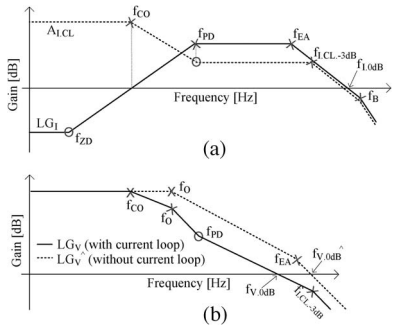

Fig. 4. Frequency response of the proposed (a) current and (b) voltage loops.

A. Stability

Current Loop: Since the voltage loop mixes the system's input reference V_{REF} and samples the system's output v_{OUT}, the current loop is within the voltage loop and must, therefore, remain stable past the voltage loop's unity-gain frequency $f_{V.0dB}$. From Fig. 3, the gain across the current loop is

$$LG_I = \frac{R_{GI}G_I(s)R_{EA}A_D g_{mS}}{\left(1+\frac{s}{2\pi f_{EA}}\right)} \equiv \frac{R_{GI}G_I(s)R_{EA}A_D g_{mS}}{(1+R_{EA}C_{EA}s)}, \tag{4}$$

where C_{EA} produces pole f_{EA} at v_{EA}, and R_{GI} is $G_I(s)$'s input resistance. As a high-pass filter, $G_I(s)$ incorporates a zero–pole pair at f_{ZD} and f_{PD} (before f_{EA}), i.e.,

$$G_I(s) = \frac{G_{I0}\left(1+\frac{s}{2\pi f_{ZD}}\right)}{\left(1+\frac{s}{2\pi f_{PD}}\right)}, \tag{5}$$

where f_{ZD} precedes f_{PD}, and the low-frequency gain G_{I0} is substantially low. Because of $G_I(s)$, as Fig. 4(a) illustrates, loop gain LG_I is low at low frequencies at

$$LG_{I0} = R_{GI}G_{I0}R_{EA}A_D g_{mS} \tag{6}$$

and rises with frequency past f_{ZD} to level at f_{PD} to

$$LG_I|_{f_{PD}<f<p_{EA}} \approx R_{GI}G_{I0}R_{EA}A_D g_{mS}\left(\frac{f_{PD}}{f_{ZD}}\right). \tag{7}$$

C_{EA} then lowers LG_I past f_{EA} at -20 dB/dec. Setting the parasitic pole at Q_P's base v_B (f_B) above current-loop's unity-gain frequency $f_{I.0dB}$ or canceling its effects with another zero ensures that LG_I crosses 0 dB with a single-pole rolloff (at -20 dB/dec), that is with adequate phase margin.

From the perspective of the voltage loop, current gain i_S/i_{REF} is the current loop's closed-loop gain $A_{I.CL}$,

$$A_{I.CL} \equiv \frac{i_S}{i_{REF}} = \frac{A_{I.OL}}{1+LG_I}, \tag{8}$$

where open-loop current gain $A_{I.OL}$ is given by

$$A_{I.OL} \equiv \frac{i_S}{i_{FB} - i_{REF}} = R_{EA}A_D g_{mS}. \quad (9)$$

At low frequencies, LG_I is considerably below unity, so $A_{I.CL}$ reduces to $A_{I.OL}$ or $R_{EA}A_D g_{mS}$. $A_{I.CL}$ decreases once LG_I rises above 0 dB, and LG_I at the crossover frequency f_{CO} is

$$LG_I|_{f_{ZD}<f<f_{PD}} \approx R_{GI}G_{I0}R_{EA}A_D g_{mS} \times \left(1 + \frac{s}{2\pi f_{ZD}}\right)\Bigg|_{f_{CO}\approx \frac{f_{ZD}}{R_{GI}G_{I0}R_{EA}A_D g_{mS}}} \equiv 1. \quad (10)$$

Once $G_I(s)$, and, thus, LG_I flatten (past f_{PD}), $A_{I.CL}$ levels to

$$A_{I.CL}|_{f_{PD}<f<p_{EA}} \approx \frac{R_{EA}A_D g_{mS}}{R_{GI}G_{I0}R_{EA}A_D g_{mS}\left(\frac{f_{PD}}{f_{ZD}}\right)} = \frac{f_{ZD}}{R_{GI}G_{I0}f_{PD}}, \quad (11)$$

and falls again at -20 dB/dec past $A_{I.CL}$'s -3-dB bandwidth $(f_{I.CL.-3dB})$, which equates to a moderate-frequency gain-bandwidth product of

$$f_{I.CL.-3\,dB} \approx (LG_I|_{f_{PD}<f<p_{EA}})f_{EA} = \left(\frac{R_{GI}G_{I0}R_{EA}A_D g_{mS}f_{PD}}{f_{ZD}}\right)f_{EA}. \quad (12)$$

In other words, the current loop effectively introduces poles at f_{CO} and $f_{I.CL.-3dB}$ and a zero at f_{PD} to the voltage loop.

Voltage Loop: From Fig. 3, both Q_P and Q_S's currents i_P and i_S (from g_{mP} and g_{mS}) flow to the output as i_O to set v_{OUT}, which means that $A_{I.CL}$ alone does not describe i_O/i_{REF}. Instead, since i_P is a mirror-ratio translation (M_I) of i_S, i_O/i_{REF} is

$$\frac{i_O}{i_{REF}} = \frac{i_P + i_S}{i_{REF}} = A_{I.CL}\left(1 + \frac{i_P}{i_S}\right) = A_{I.CL}(1 + M_I). \quad (13)$$

As such, the gain across the voltage loop is

$$LG_V = G_V A_{I.CL}(1 + M_I)Z_O\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right), \quad (14)$$

where Z_O is the impedance at v_{OUT}, and $R_{FB1} - R_{FB2}$ voltage–divides v_{OUT} to G_V's input v_{FB}. As a result, as Fig. 4(b) shows, LG_V first drops past $A_{I.CL}$'s crossover frequency f_{CO}, and more rapidly past Z_O's C_O pole f_O (when C_O shunts r_{oP}), until $A_{I.CL}$ levels past f_{PD} (with a zero). LG_V is stable because it reaches $f_{V.0dB}$ below $A_{I.CL}$'s $f_{I.CL.-3dB}$ (i.e., at -20 dB/dec and with an adequate phase margin). Without the current loop, as in conventional LDOs, the loop gain [depicted by $LG_V^{\wedge}$ in Fig. 4(b)] would first drop past Z_O's C_O pole f_O and more rapidly past v_{EA}'s pole f_{EA}, inducing $LG_V^{\wedge}$ to reach unity-gain frequency $f_{V.0dB}^{\wedge}$ at -40 dB/dec (with little to no phase margin). In other words, the current loop helps stabilize the voltage loop. Note that C_O's R_{ESR} zero is above $f_{I.CL.-3dB}$ because R_{ESR} is negligibly small at a few milliohms.

B. PSR Performance

The current loop effectively introduces series (current-sampled) impedance Z_I in the supply path, as Fig. 5(a) illustrates, just like shunt sampling introduces shunt (voltage-sampled) impedance Z_V to ground. Similarly, high LG_I increases Z_I just as high LG_V decreases Z_V

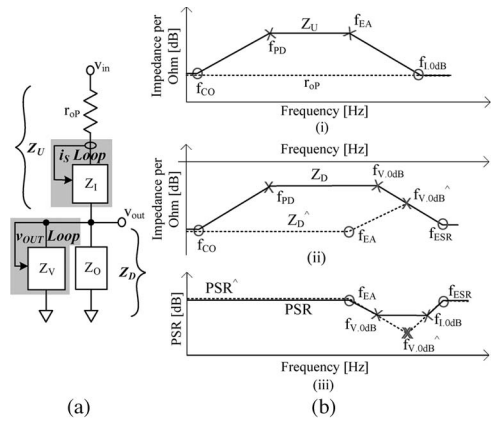

Fig. 5. PSR (a) model and (b) response of the proposed current-mode LDO.

$$Z_I = LG_I Z_{I.OL} \approx LG_I r_{oP} \quad (15)$$

and

$$Z_V \equiv Z_{O-REG} = \frac{Z_{V.OL}}{LG_V} = \frac{Z_O \| (r_{oP} + Z_I)}{LG_V} \approx \frac{Z_O}{LG_V}, \quad (16)$$

except the former does so at high frequencies and the latter at low frequencies in the proposed scheme. In either case, high loop gains improve PSR (i.e., increase Z_I and decrease Z_V).

The fundamental benefit of series feedback is increasing supply impedance Z_U [in Fig. 5(a)] from its r_{oP} base by a $(1 + LG_I)$ factor. Because the current loop is open at low frequencies (i.e., $LG_I < 1$), Z_U is r_{oP} at low frequencies, as shown in (i) in Fig. 5(b). The loop asserts its influence when LG_I rises above 0 dB, past crossover frequency f_{CO}, beyond which point Z_U follows LG_I's response, leveling past f_{PD}, and decreasing after f_{EA}. Z_U, then, falls back to its open-loop value of r_{oP} beyond $f_{I.0dB}$ when LG_I, again, falls below 0 dB.

LG_I also affects total ground impedance Z_D [in Fig. 5(a)] via the closed-loop current gain $A_{I.CL}$. LG_V, for instance, decreases past LG_I's f_{CO}, so Z_V (and, thus, Z_D) increases past f_{CO} in (ii) in Fig. 5(b), leveling after LG_I's f_{PD}. Beyond $f_{V.0dB}$, Z_V surpasses Z_O (so Z_D reduces to Z_O) and C_O shunts v_{OUT} (so Z_O decreases until C_O's impedance is negligible relative to R_{ESR}—past f_{ESR}), beyond which point Z_O (and, therefore, Z_D) flattens to R_{ESR}. Without the current loop, the ground impedance $(Z_D^{\wedge})$ would remain unchanged from its low-frequency value until f_{EA} induces $Z_V^{\wedge}$ to increase, past which point $Z_D^{\wedge}$ rises with $Z_V^{\wedge}$. When $Z_V^{\wedge}$ surpasses Z_O (after the loop's unity-gain frequency $f_{V.0dB}^{\wedge}$), $Z_D^{\wedge}$ follows Z_O, falling as C_O shunts v_{OUT} until C_O completely shorts (past f_{ESR}) and Z_O (and $Z_D^{\wedge}$) reduces to R_{ESR}.

To appreciate LG_I's impact on PSR, recall that supply gain A_{IN} is a voltage-divider translation, and its reciprocal is PSR

$$A_{IN} \equiv \frac{1}{PSR} = \frac{Z_O \| Z_V}{(r_{oP} + Z_I) + Z_O \| Z_V}. \quad (17)$$

At low frequencies, Z_I is negligible relative to r_{oP}, and Z_V is considerably lower than Z_O and r_{oP}, so PSR reduces to r_{oP}/Z_V. Above f_{CO}, LG_I increases Z_I (and Z_U), so PSR

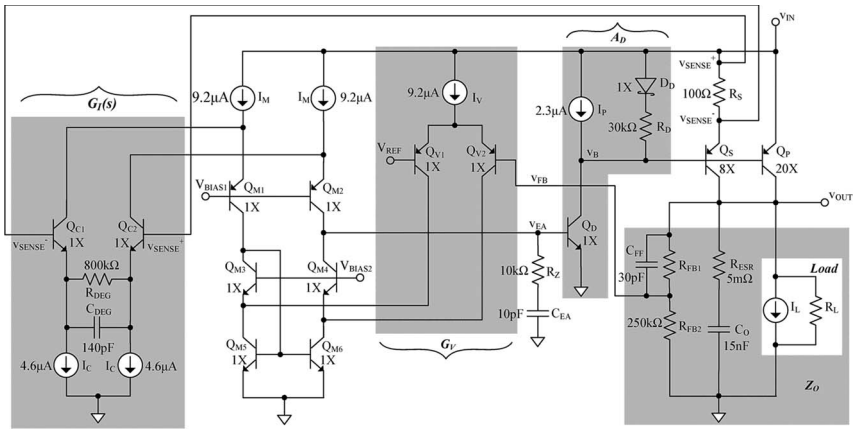

Fig. 6. Transistor-level schematic of the proposed current-mode LDO.

changes to Z_I/Z_V, except both Z_I and Z_V increase beyond this point, which means that PSR remains unchanged past f_{CO}, as (iii) in Fig. 5(b) illustrates. Similarly, Z_I and Z_V both level after f_{PD}, so no changes in PSR occur until f_{EA} decreases Z_I (and Z_U), reducing PSR after f_{EA}.

Above $f_{V.0dB}$, Z_V surpasses Z_O, so Z_D reduces to Z_O and PSR to Z_I/Z_O, where C_O shunts Z_O, again canceling Z_I's decreasing effect and leveling PSR (past $f_{V.0dB}$). PSR remains unchanged until Z_U reduces back to r_{oP} (i.e., PSR is r_{oP}/Z_O) when LG_I falls below 0 dB (past $f_{I.0dB}$). This cessation in Z_I's descent, combined with Z_O's continued fall, causes PSR to increase after $f_{I.0dB}$, until C_O shorts past f_{ESR} (i.e., Z_O reduces to R_{ESR}), and PSR levels to r_{oP}/R_{ESR}. Note that without the current loop, as (iii) in Fig. 5(b) illustrates, $PSR^{\wedge}$ is worse near $f^{\wedge}_{V.0dB}$, at frequencies where emerging dc–dc converters typically switch.

C. IC Design

The prototyped current-mode LDO in Fig. 6 senses i_P with mirror transistor Q_S. Q_S's degenerating resistor R_S (also in Fig. 3 as R_{GI}) then converts sense current i_S into a voltage. R_S and Q_S's emitter area are large enough to ensure that R_S's voltage is discernable and sufficiently small (at 100 Ω and 2/5 of Q_P's area) to keep the power lost in R_S low. Input pairs $Q_{C1}-Q_{C2}$ and $Q_{V1}-Q_{V2}$ implement $G_I(s)$ and G_V in Fig. 3, and cascodes $QQ_{M1}-Q_{M2}-Q_{M3}-Q_{M4}$ fold and combine their respective ac output currents into v_{EA}. R_{DEG} degenerates $Q_{C1}-Q_{C2}$'s gain to G_{I0} or $g_{mC}/(1+0.5R_{DEG}g_{mC})$, which is roughly $1/0.5R_{DEG}$, to keep $G_I(s)$ (and LG_I) low at low frequencies, and C_{DEG} shorts R_{DEG} to increase $G_I(s)$ (and LG_I) past $1/2\pi C_{DEG}R_{DEG}$ [f_{ZD} in Fig. 4(a)]. $G_I(s)$ levels to g_{mC} when the degenerating effect (impedance) disappears past $g_{mC}/4\pi C_{DEG}$, which is f_{PD} in Fig. 4(a). Because LG_I is low and LG_V is high at low frequencies, $G_I(s)$'s output and its impact on dc input-referred offset are low, which means that the LDO regulates v_{OUT} accurately. Although Q_S and Q_D conduct more current when I_O rises, the rise constitutes a small fraction of $I_{O(max)}$, so current efficiency remains high (see Table II).

R_Z limits C_{EA}'s shunt current to introduce a zero at $1/2\pi R_Z C_{EA}$, whose objective is to cancel the effects of the parasitic pole at the bases of Q_P and Q_S. Similarly, C_{FF} feeds forward in-phase signals from v_{OUT} to v_{FB} at moderate to high frequencies to generate a zero that cancels the pole introduced at Q_{V2}'s base. Lastly, because Q_P's current gain β_{PNP} varies widely across load currents, D_D and R_D help ensure a relatively constant current gain from Q_D's collector to the output load to help maintain stability across extreme operating corners.

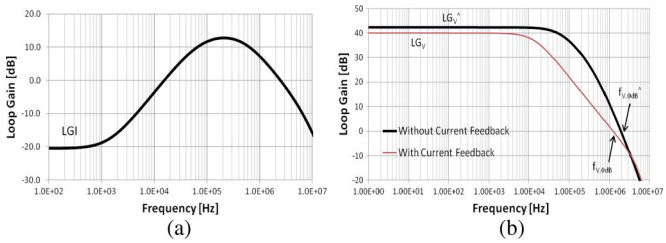

Fig. 7. Simulated loop-gain response of the (a) current and (b) voltage loops when loading the LDO with 5 mA.

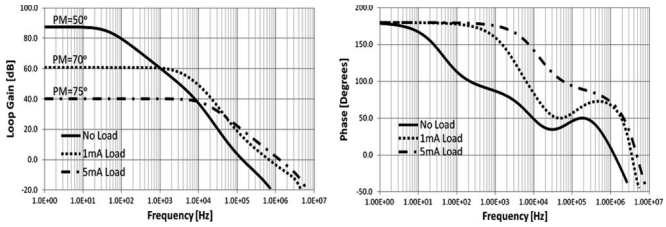

Fig. 8. Frequency response of the LDO under 0, 1, and 5 mA of the load.

In practice, f_{PD} nears f_{EA}, so LG_I's flattening effect in Fig. 4(a) seems absent in the simulated response in Fig. 7(a). Similarly, LG_I's f_{PD} is near f_O, so their opposing effects on LG_V [see Fig. 4(b)] cancel the Bode plot in Fig. 7(b), allowing LG_V to drop past f_{CO} and reach $f_{V.0dB}$ at −20 db/dec. Fig. 7(b) also illustrates how $LG_V^{\wedge}$ (without the current loop) reaches $f^{\wedge}_{V.0dB}$ at −40 dB/dec. The simulation results in Fig. 8 show that the system exhibits no less than 50° of phase margin when loaded with 0, 1, and 5 mA, which indicates that the system is stable as low-frequency gain $LG_{V.DC}$ and f_O (i.e., r_{oP} in Z_O) shift across loads. Notice that r_{oP} and R_{EA} (which is roughly Q_D's r_π or 43 kΩ) both decrease with increasing values of i_P, so $LG_{V.DC}$ generally decreases with higher load currents. For verification, Table I shows that the derived locations of the poles and zeros match reasonably well with their simulated counterparts in Figs. 7 and 8.

IV. Experimental Results

Fig. 9 shows the photograph of the fabricated 1.5-μm bipolar IC and the PCB used to evaluate it. Fig. 10(a) illustrates the

TABLE I
CALCULATED VERSUS SIMULATED LOCATIONS OF POLES AND ZEROS AT 5 mA

Parameter	Calculated	Simulated
f_{ZD}	1.4 kHz	1.3 kHz
f_{CO}	10 kHz	14 kHz
f_{PD}	95 kHz	110 kHz
f_O	88 kHz$^{\Omega}$/1 kHz$^{\Psi}$	95 kHz$^{\Omega}$/1.1 kHz$^{\Psi}$
f_{EA}	369 kHz	405 kHz

$^{\Omega}$Resistive load (R_L is V_{OUT}/I_L) and $^{\Psi}$current-source load (R_L is infinite).

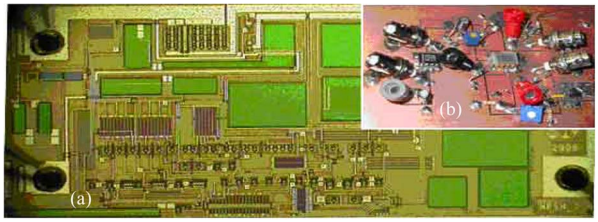

Fig. 9. (a) 1.2 mm^2 die and (b) PCB photographs.

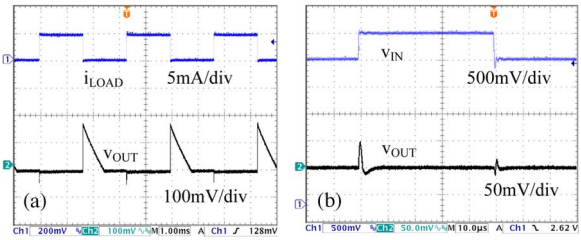

Fig. 10. Transient (a) load-step and (b) input-line responses.

LDO's transient response to 0- to 5-mA 100-ns load steps with 15 nF of output capacitance C_O. Note that v_{OUT} rises to 200 mV when the load suddenly falls, and $R_{FB1}-R_{FB2}$ slew it back to regulation in roughly 0.8 ms. The response shows that the LDO is stable with 15 nF of C_O. Fig. 10(b) further shows that v_{OUT} settles within roughly 0.15 mV of its target in 0.54 μs in response to 1-μs 500-mV input variations (Δv_{IN}), which indicates that the LDO's bandwidth is faster than roughly 1 MHz. Although the time scale in Fig. 10(a) (which was adjusted to accommodate v_{OUT}'s slew-rate response) cannot show it, the LDO also recovers from a rising load step in less than 1 μs.

To measure PSR across frequency, low-amplitude sinusoids of various frequencies were superimposed onto the LDO's input supply v_{IN}, and the resulting ripple at v_{OUT} was recorded. The peak–peak voltage of the input ripple was only 100 mV to avoid disrupting the LDO's biasing point. Because the LDO considerably attenuates the ripple considerably, a low-noise high-bandwidth amplifier (LT6200-10) amplified v_{OUT} to a level that the monitoring oscilloscope could discern.

To appreciate the impact of the current loop on PSR, Fig. 11 shows the response with (PSR) and without (PSR$^{\wedge}$) the current loop (where shorting R_S disables the current loop). To keep the LDO stable in both cases, C_O was 68 nF because the LDO became unstable with 15 nF without the current loop. As Fig. 11 shows, the current loop further suppresses supply ripples in the critical worst case range of 0.5–5 MHz (where dc–dc converters typically switch) by 20 dB when loaded with 5 mA.

Although each application values parameters differently, high PSR LDOs generally trade the PCB area with a larger off-chip C_O (to shunt supply ripple), lower maximum I_O (to raise

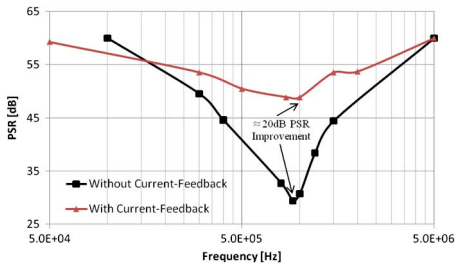

Fig. 11. PSR measurement results with and without the current loop.

TABLE II
STATE-OF-THE-ART COMPARISONS

	Cascode LDO [1]	Feed Forward LDO [3]	TPS719X LDO [10]	Proposed Current-Mode LDO
$V_{IN(min)}$	1.8 V	1.15 V	2.7 V	1.4 V
$I_{O(max)}$	5 mA	25 mA	200 mA	5 mA
V_{DO}	**450 mV**	**150 mV**	**230 mV**	**200 mV**
$C_{O(min)}$	**On Chip**	**4 µF**	**1 µF**	**15 nF**
Load Reg.	1.6 mV/mA	48 µV/mA	75 µV/mA	920 µV/mA
Current Efficiency	98.5%	99.8%	99.95%$^{\lambda}$ 99.90$^{\varphi}$	98.9%$^{\lambda}$ 96.3%$^{\varphi}$
PSR at 100 kHz	61 dB	62 dB	58 dB	57 dB*
$PSR_{(min)}$	**27 dB**	**56 dB**	**24 dB**	**29 dB$^{\wedge,*}$ 32 dB$^{\Omega}$ 49 dB***
$t_{Response}$	**0.30 µs**	**2.4 µs$^{\Psi}$**	–	**0.54 µs**
Technology	0.6 µm CMOS	0.13 µm CMOS	–	1.5 µm Bipolar
FoM	**N/A**	**25M**	**14M**	**10M$^{\wedge,*}$ 66M$^{\Omega}$ 104M***

$^{\lambda}$No load, $^{\varphi}$full load, $^{\Psi}$calculated, $^{\wedge}$without I loop, $^{\Omega}$with 15 & *68 nF of C_O.

r_{ds}), and raise dropout voltage V_{DO} (to reduce early effects) for higher $PSR_{(min)}$. As such, a linear figure-of-merit (FoM) that improves with higher $PSR_{(min)}$ and $I_{O(max)}$ and lower V_{DO} and C_O, although not universally applicable, reasonably reflects LDO tradeoff performance. Accordingly, the FoM in Table II ($PSR_{(min)}I_{O(max)}/V_{DO}C_O$) indicates that the proposed LDO performs 6× and 3× better than itself without the current loop and the state of the art, respectively. This FoM does not include the quiescent current, the bandwidth, or the die area because they depend strongly on the process, which varies across the state of the art.

V. CONCLUSION

Experimental results have shown that the proposed current-mode LDO improves PSR by 20 dB across the critical worst case frequency range of 0.5–5 MHz, where most dc–dc converters switch, and typical LDOs falter. PSR was roughly 3× better than the state of the art in externally compensated LDOs. The prototyped 1.5-μm bipolar LDO achieved this performance by increasing the impedance to the supply with a current-sampling feedback loop. The loop essentially samples the output current with a mirroring sense transistor and mixes it into the main (voltage) loop through a frequency-shaping (RC-degenerated)

differential pair. Further suppressing the supply ripple (by $6\times$) in this way prevents switching converter noise from rendering sensitive analog functions ineffectual.

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