

# A PSR Enhancement Scheme: An Overview of Feed-Forward Ripple Cancellation Technique

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**Abstract**—Power supply rejection (PSR) is a critical performance metric that evaluate the LDO's ability to suppress supply noise. Typical analog low drop-out regulator (A-LDO) achieves high PSR at low-frequency region and light load conditions. However, the PSR performance degrades due to reduced loop gain of an LDO at high frequencies and heavy load currents. Prior works on enhancing the PSR performance include increasing loop bandwidth or loop gain, using cascode structure by stacking transistors on power transistor, cascading two regulators. While these techniques improve the PSR at the cost of increasing design complexity and increasing losses. Compared with the above methods, the feed-forward ripple cancellation (FFRC) technique, being an auxiliary feed-forward path, can effectively improve the PSR performance of the LDOs at the expense of low design complexity and quiescent power and becomes the focus of researchers. In this paper, the injection methods of FFRC and four different FFRC circuit structures are overviewed, compared, and discussed. Then, the design guideline for a high PSR and low quiescent current A-LDO is drawn.

**Keywords**—power supply rejection, analog low drop-out regulator, feed-forward ripple cancellation technique, auxiliary feed-forward path, low quiescent current.

## I. INTRODUCTION

System-On-Chips (SOCs) enables the integration of complex systems into a single chip, reducing power consumption, improving performance, and reducing system cost. The power management units (PMUs) as the core power supply module of the SOCs is shown in Fig.1, which consists of a DC-DC switching power converter and analog low drop-out (A-LDO) regulators. DC-DC usually supply noise-insensitive block, such as processor, due to its relatively fluctuated output voltage. In contrast, A-LDO is usually utilized to drive noise-sensitive blocks, such as sensors, analog and power amplifier blocks, thanks to its clean output voltage. With the development of SOCs, the noise with random frequency from power supply becomes obvious in the noise-sensitive blocks. Therefore, it is necessary for A-LDO to provide high PSR characteristics over a wide frequency range to ensure stable operation of noise-sensitive blocks. Various techniques have been proposed in the past decade to enhance the PSR characteristics of LDOs in the wide bandwidth range. All of these techniques can be broadly divided into four primary classifications: Firstly, increasing loop bandwidth [1] or loop gain [2], but there are often exists stability issues and can consume large static power. Secondly, power supply noise pre-processing by stacking transistors on power transistor to form a cascode structure [3], but additional circuits such as a charge pump is required and will increase the voltage dropout (VOD) between the input and output, reducing the efficiency of the LDO. Thirdly, By adopting a

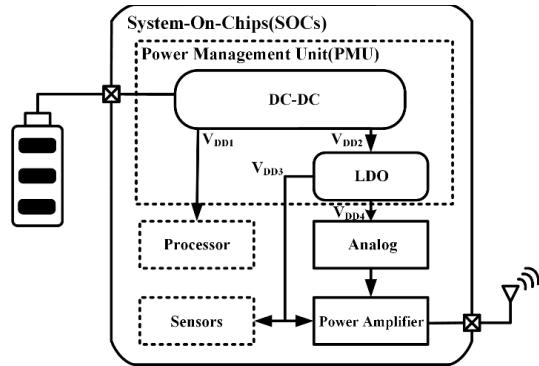


Fig. 1. Power management units

cascaded arrangement of two LDOs [4], the first-stage LDO can weaken the noise in power supply and then the processed noise transfers to the second-stage LDO, thereby improving the overall PSR characteristics of the overall circuit. But, since the two LDOs are connected in series, also increase the VOD. Besides, Due to the poor mid-to-high frequency PSR characteristics of the first-stage LDO, the second-stage LDO is unable to effectively filter out the noise in this frequency range. This results in a poor mid-high frequency PSR performance of the overall LDO circuit. Lastly, By using feed-forward ripple cancellation (FFRC) technique [5-6], compensation values are introduced from the feedforward path to reduce the current fluctuation on the power transistor. FFRC technique has several advantages, including not impacting the stability of the feedback loop, not increasing the VOD, and significantly improving the PSR within a wide bandwidth range [7]. Therefore, FFRC technique is currently considered the most effective and cost-efficient solution for improving the PSR characteristics of LDO.

This paper is organized as follows. Section II discusses different FFRC injection methods. Section III introduces different types of FFRC circuits and provides relevant explanations of their working principles. It also analyzes the advantages and disadvantages of each circuit. Section IV compares and discusses the performance of different FFRC circuits. Finally, Section V presents relevant conclusions and provides the design guidance.

## II. DIFFERENT FFRC INJECTION METHODS

### A. Gate-injection and Body-injection

FFRC technique can be classified into Gate-injection method and Body-injection method based on the injection location. For the Gate-injection method, the FFRC value is injected into the gate terminal of power transistor. Therefore, the power transistor does not exist substrate bias effects and the stability is higher. But, when the gate terminal is used for

current mode summing, the accuracy is generally poor. When used for voltage mode summing, it requires additional summing circuitry, resulting in additional power consumption. For the Body-injection method, the FFRC value can be directly injected into the power transistor body terminal, without the need for additional summing circuit. However, its injection value is generally too larger, which may lead to the conduction of the source-body diode of power transistor, resulting in leakage current.

### B. Voltage-injection and Current-injection

In addition, FFRC technique can be classified into Voltage-injection method and Current-injection method based on the injection variables. The PSR optimization range of the Voltage-injection method is directly determined by the bandwidth of the operational amplifier. Thus, in order to expand the bandwidth of the operational amplifier to obtain PSR optimization within a wide bandwidth range, a large quiescent current will be generated. In contrast, the Current-injection method uses an superposition of current signals by connecting two current branches, so the PSR optimization range is wide and does not require a large power consumption. However, for Current-injection method, the inaccuracy in the current superposition process affects the optimization of PSR, while Voltage-injection method does not have this problem.

### III. DIFFERENT FFRC CIRCUITS

This section provides an introduction to the working principles of four mainstream FFRC circuits, namely Gate-injection adaptive supply-ripple cancellation (ASRC) circuit, Body-injection ASRC circuit, Current-mode FFRC circuit, and Capacitive FFRC circuit. The mechanisms through which these FFRC circuits enhance the PSR characteristics of LDOs are analyzed, and the advantages and disadvantages of each FFRC circuit are summarized.

#### A. Gate-injection ASRC CIRCUIT

Park et al. present an Gate-injection ASRC circuit [8] that can address the power supply noise due to parasitic capacitances  $C_{gs}$  and  $C_{gd}$  of the power transistor. As shown in Fig.2, Gate-injection ASRC circuit consists of a scaled replica of the transistor  $M_{PR}$  and a current amplifier. In order to tracks the change of  $C_{gd}$  of the power transistor under various process-voltage-temperature (PVT) conditions, the transistor  $M_{PR}$  is scaled down 100 times in proportion to the power transistor to create feed-forward ripple current  $sC_{gdr}V_{dd}$ . Then the current amplifier amplifies  $sC_{gdr}V_{dd}$  by a factor of 100 and feeds it into the  $V_{gate}$ . Ultimately, the feed-forward ripple current is converted into a corresponding voltage through the effect of the gate impedance of the pass transistor.  $\Delta V_{gate}$  can be represented as

$$\Delta V_{gate} = \frac{sC_{gd}\Delta V_{dd} + sC_{gs}\Delta V_{dd}}{s(C_{gd} + C_{gs} + C_p)} \approx \Delta V_{dd} \quad (1)$$

According to (1), the fluctuating current  $\Delta i$  on the power transistor caused by power supply noise can be represented as

$$\Delta i = g_m (\Delta V_{dd} - \Delta V_{gate}) + g_{ds} \Delta V_{dd} \quad (2)$$

Theoretically, in any case,  $\Delta V_{gate}$  can be equal to  $\Delta V_{dd}$ . Because of transistor  $M_{PR}$  can track the change of  $C_{gd}$  of power transistor, the feed-forward ripple current  $sC_{gdr}V_{dd}$  can be keep adjusted. Thus, the value of  $\Delta i$  can be reduced. But, the optimization effect of PSR at high frequencies is limited due to the power supply noise coupled through the source-drain

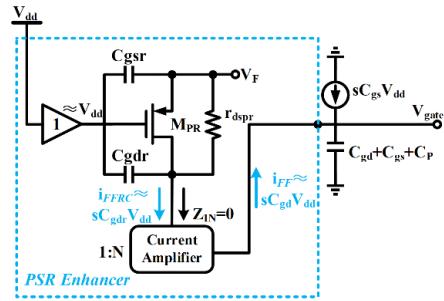


Fig. 2. Gate-injection ASRC Circuit

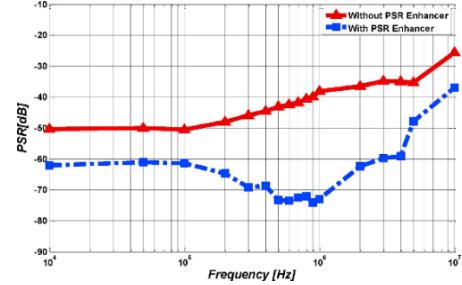


Fig. 3. Gate-injection ASRC Circuit with and without the psr enhancer

resistance  $r_{ds}$  of power transistor is neglected. As shown in Fig.3, the PSR optimization effect reaches its peak at 1MHz, and gradually deteriorates as the frequency increases.

#### B. Body-injection ASRC CIRCUIT

In order to further broaden the high PSR frequency range, Lim et al. present a Body-injection ASRC circuit [9]. As shown in Fig.4, the proposed Body-injection ASRC circuit includes two fundamental components, namely body-ripple injector (BRI) and  $g_{ds}$ -to- $g_{mb}$  sensor (GTGS). The function of GTGS is to accurately obtain the ratio of  $g_{ds}$  to  $g_{mb}$  of the power transistor and convert this ratio into the ratio of  $R_2$  to  $R_1$ .  $M_{R2}$  acts as a variable resistor operating in the linear region with an effective resistance equal to  $R_2$ . The BRI includes a high-pass path composed of  $R_M$  and  $C_M$  and a non-inverting proportional injection circuit consists of a feedback network  $R_2$  and  $R_1$  and a wide-band amplifier. The function of BRI is to amplify the power supply noise  $\Delta V_{dd}$ , which is coupled through a high-pass path, by a factor of  $1+R_2/R_1$ , and then inject the amplified voltage value into  $V_B$ .  $\Delta V_{ASRC}$  can be represented as

$$\Delta V_{ASRC} = \Delta V_{dd} \left( 1 + g_{ds} / g_{mb} \right) \quad (3)$$

In addition, since a coupling capacitor  $C_C$  is used between  $V_{dd}$  and  $V_G$ , if  $C_C$  is significantly larger than  $C_{gd}$ , the power supply noise coupled through the  $C_{gs}$  of the power transistor will be eliminated. According to (3) and the function of  $C_C$ ,  $\Delta i$  can be represented as

$$\Delta i = g_m \left( \Delta V_{dd} - \Delta V_{dd} \frac{C_{gs} + C_c}{C_{gs} + C_{gd} + C_c} \right) + g_{ds} \Delta V_{dd} + g_{mb} (\Delta V_{dd} - \Delta V_{ASRC}) \quad (4)$$

From (4), it can be seen that if  $\Delta V_{ASRC}$  equals  $\Delta V_{dd}$  and  $C_C$  is sufficiently large, then  $\Delta i$  will equal zero. Therefore, Body-injection ASRC circuit ensures that the fluctuating current caused by the  $C_{gs}$  and  $1/g_{ds}$  of the power transistor is approximately zero. Besides, GTGS can adjust the ratio between  $R_2$  and  $R_1$  in real-time according to the variation of

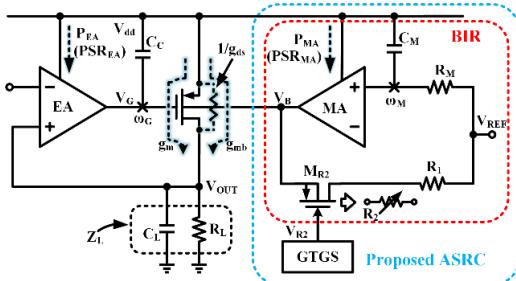


Fig. 4. Body-injection ASRC Circuit

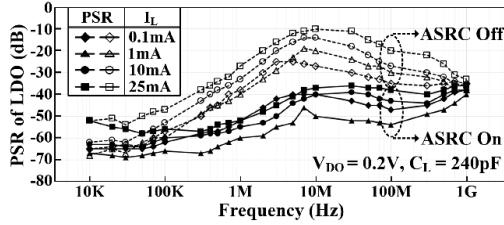


Fig. 5. Body-injection ASRC Circuit with and without the psr enhancer

the power transistor despite PVT variations and all operating conditions. However, this technique is not suitable for low-power applications due to its high quiescent current, which can reach up to  $300 \mu\text{A}$ , in order to extend the PSR optimization bandwidth. Moreover, as shown in Fig.5, the PSR optimization effect is limited in the mid-low frequency range less than 15 dB up to 2 MHz.

### C. Current-mode FFRC CIRCUIT

Joshi et al. present a Current-mode FFRC circuit [10], which is capable of enhancing the PSR characteristics of the LDO without generating vast quiescent current at the same time. As shown in Fig.6, the gate of  $MP_{ff}$  is AC-grounded in comparison to its source due to the negative feedback effect generated by  $A1$ . Thus, power supply noise generates feed-forward ripple current  $g_{mff}\Delta V_{dd}$  through transistor  $MP_{ff}$ . Then, the feed-forward ripple current injects to the gate of power transistor by utilizing current mirror. Since the buffer has been specifically engineered to maintain a low output impedance across a wide range of frequencies. So, power transistor gate impedance is equal to  $1/g_{mbuf}$  till a few MHz of frequency range. If the size and bias of both devices are the same, through proper matching, the  $g_m$  of the two MOSFETs can be made equal. By this way, the gate voltage of power transistor will be equal to its source voltage and guarantees that the enhancement in PSR is stable under various PVT conditions.  $\Delta i$  can be represented as

$$\Delta i = g_m \left( \Delta V_{dd} - \Delta V_{dd} \frac{g_{mff}}{g_{mbuf}} \right) + g_{ds} \Delta V_{dd} \quad (5)$$

Current-mode addition is an inherent feature where no additional circuitry is needed. Therefore, the Current-mode FFRC circuit has a low quiescent current at full load range. But, the same as above, the optimization effect of PSR at high frequencies is limited due to the neglect of the power supply noise coupled through the source-drain resistance  $r_{ds}$  of power transistor. In addition, as shown in Fig.7, this solution has a relatively narrow PSR optimization range, reaching only up to 5MHz. The deterioration trend of PSR for with Current-mode FFRC technique is the same as that of without Current-mode FFRC technique. So, aiming to improve the PSR optimization

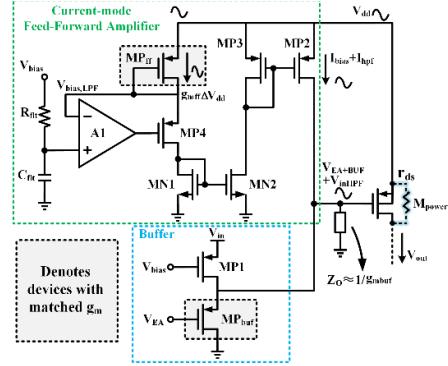


Fig. 6. Current-mode FFRC Circuit

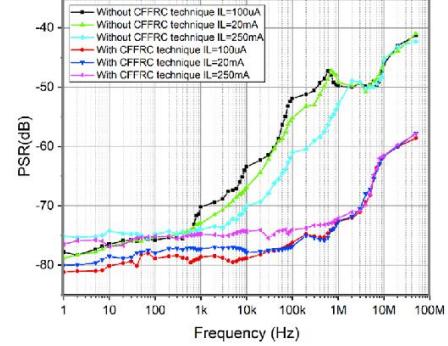


Fig. 7. Current-mode FFRC Circuit with and without the psr enhancer

range, it is necessary to increase the current flowing on the  $MP_{buf}$  to obtain a smaller  $1/g_{mbuf}$ , or use other structures like super source follower as buffer. But, it will increase circuit power consumption and complexity.

### D. Capacitive FFRC CIRCUIT

Aiming to minimize the quiescent current of the overall circuit to below 1uA, Guo et al. present a Capacitive FFRC circuit [11]. As shown in Fig.8, in order to realize minimize chip area and low quiescent bias current, the physical resistors  $R_{b1}$  and  $R_{b2}$  are substituted with MOSFET-based pseudo-resistor. Besides, the DC gain of the feed-forward amplifier (FFA) and the summing amplifier (SA) are the ratio of capacitors instead of the ratio of resistors. Thus, FFA and SA can be designed as low quiescent current amplifiers to reduce power consumption. The proposed LDO features a minimum quiescent current of  $0.9\mu\text{A}$  only. The fluctuation voltage  $\Delta V_G$  caused by the power supply noise at the gate of the power transistor can be represented as

$$\Delta V_G = \frac{C_{FF1} C_{S1}}{C_{FF2} C_{S2}} \Delta V_{dd} \quad (6)$$

According to (6),  $\Delta i$  can be represented as

$$\Delta i = g_m \left( \Delta V_{dd} - \frac{C_{FF1} C_{S1}}{C_{FF2} C_{S2}} \Delta V_{dd} \right) + g_{ds} \Delta V_{dd} \quad (7)$$

Based on (7), it can be observed that if the ratio of  $C_{FF1} C_{S1}$  and  $C_{FF2} C_{S2}$  equal to one, the first term of (7) becomes zero, and  $\Delta i$  can be reduced. However, the high-frequency optimization of PSR in this circuit is limited as it ignores the power supply noise coupled through the source-drain resistance  $r_{ds}$  of power transistor. As shown in Fig.9, the PSR optimization effect gradually deteriorates as the frequency increases. Besides, due to the fixed capacitance  $C_{FF1}$ ,  $C_{FF2}$ ,  $C_{S1}$

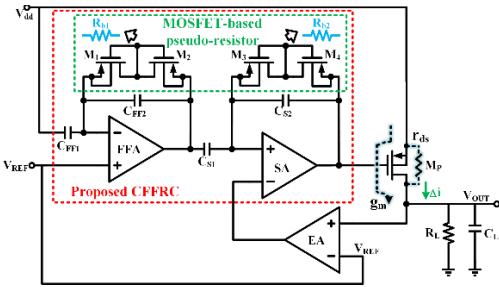


Fig. 8. Capacitive FFRC Circuit

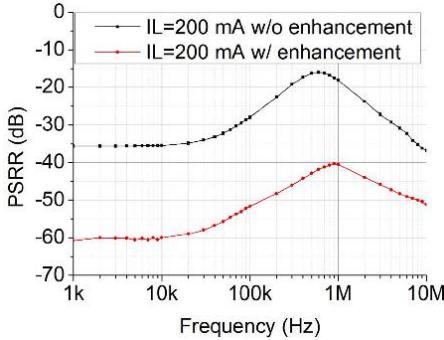


Fig. 9. Capacitive FFRC Circuit with and without the psr enhancer

and  $C_{S2}$ , the PSR optimization effect varies widely under different load currents and PVT conditions.

#### IV. COMPARISON AND DISCUSSION

TABLE I provides a quantitative comparison of various FFRC techniques. It can be seen that most of the FFRC techniques have PSR optimization values that can adaptively change under PVT variations, except for Capacitive FFRC technique. At maximum load current, it can be observed that different types of FFRC techniques have similar PSR optimization values at 1MHz. But after 10MHz, the PSR optimization value of the Body-injection ASRC technique is significantly better than the others, especially at 100MHz where it still has a significant PSR optimization effect. The maximum quiescent current of Gate-injection ASRC technique and Current-mode FFRC technique is less than Body-injection ASRC technique and Capacitive FFRC technique, and the minimum quiescent current of Capacitive FFRC technique is only 0.9uA, which is the smallest in the TABLE I.

TABLE I. COMPARISON AMONG DIFFERENT FFRC CIRCUITS

	<i>Gate-injection ASRC Circuit</i>	<i>Body-injection ASRC Circuit</i>	<i>Current-mode FFRC Circuit</i>	<i>Capacitive FFRC Circuit</i>
Adaptability	Y	Y	Y	N
Process (nm)	180	65	180	180
PSR Values (dB)	34 @1MHz 12 @10MHz / @100MHz	23 @1MHz 30 @10MHz 20 @100MHz	20 @1MHz / @10MHz / @100MHz	22 @1MHz 14 @10MHz / @100MHz
Load current (mA)	50	25	250	200
Quiescent current ( $\mu$ A)	50-90	8-297.5	5.6-35.6	0.9-160

#### V. DESIGN GUIDELINE AND CONCLUSION

FFRC technique has become the mainstream solution in recent years to enhance the PSR characteristics of LDO, due to its can effectively broaden high PSR frequency range without affecting feedback loop stability and increasing the VOD. This paper overviews and analyzes the latest FFRC techniques targeting for high PSR characteristics. It has been

found that some FFRC schemes, while aiming for high PSR characteristics, are also beginning to pursue low quiescent current. Body-injection ASRC circuit is able to realize high PSR optimization within a wide frequency range, but it has a higher quiescent current. On the contrary, Current-mode FFRC circuit has a lower quiescent current, but its PSR optimization bandwidth is smaller, only ranging from 100Hz to 5MHz.

Consequently, to maximize the PSR characteristics across all frequency bands while maintaining a lower quiescent current, it is advisable to use a combination of Body-injection ASRC circuit and Current-mode FFRC circuit. Body-injection ASRC circuit is primarily used to enhance PSR characteristics in the mid-to-high frequency bands. So, the MA gain can be relatively reduced, thereby lowering the quiescent current. On the other hand, Current-mode FFRC circuit is mainly responsible for improving PSR characteristics in the low frequency bands, and it will not generate enormous static power consumption. Besides, MOSFET-based pseudo-resistor can be utilized to reduce chip area compared to physical resistors.

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