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Design and Simulation of a Capless Low Drop Out Voltage Regulator

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***Abstract*—The changing requirements of the industry is directing towards the full integration of SoC. This requires the power management block to have the Low Drop Out(LDO) regulator with reduced external capacitor. This paper proposes the study of behavior of the LDO voltage regulator with an external capacitor and capless low drop out voltage regulator. The regulated voltage of 1.8V is obtained using the typical power supply of 2.2V. The total quiescent current used in the circuit is less than 30uA with the load current variation of 0 to 20mA. The capless LDO architecture is verified in the UMC 180nm technology. The architecture provides a stable regulated voltage of 1.8V with both line and load variations and also for the transient variations. The stability issues are overcome using the compensation techniques which uses a current amplifier and a capacitor in the differentiator configuration. The current amplifier implemented uses current mirror with current copying ratio of unity.**

Keywords—Voltage regulator, Low Drop out, capacitorless, compensation, quiescent current.

I. INTRODUCTION

Battery operated devices such as phones, ipods, laptops, etc., requires the system to have a strong power management block in the SoC. Subsystems like regulators (linear and switching) and control logic are part of power management systems. According to the needs of each block and operation modes, power management system monitors correct and balanced distribution of energy. Efficiency and battery life are the major contributors for the performance of the power management system. Power management block's major role is to supply the system a constant voltage even at the decreased battery voltage. The required regulator must have a small drop of voltage so that the lowest voltage of the battery does not affect the function of other systems on the chip[1][6].

Stable voltage derived from the power supply independent of load current, supply voltage and temperature variations is provided by a linear regulator. The constant output voltage is obtained across the resistance of the regulator which varies in accordance with the load. It is behaves as a variable resistor which adjusts its value to provide a fixed voltage. Difference between the input and regulated voltage is dissipated in the form of heat.

The conventional voltage(linear) regulators use a NMOS Field Effect transistor in the common drain configuration as shown in the figure 1. In a conventional linear voltage regulator, the driver circuit uses the same supply voltage as that of the pass element. The regulation compels the driver circuit to drive the pass element with a large voltage so that the pass element is maintained in the saturation region.

In LDO regulator the difference between the input and the output voltage is very small. The LDO regulators can control their output voltage with much less headroom. The LDO regulators use a PMOS Field Effect transistor as a pass element.

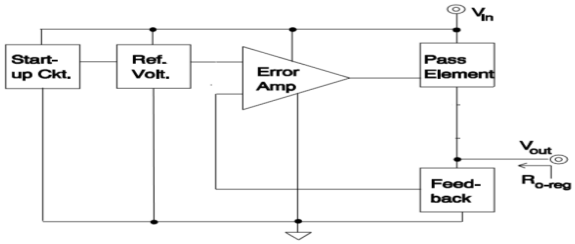

Fig.1: Block diagram of Low drop out voltage regulator [1].

II. LDO DESIGN CONSIDERATION

A. Pass Element

The output current capability of the error amplifier is boosted to the higher level by the series pass element . The pass element used is the PMOS transistor which is capable of operating under very low dropout voltages. The pass element forms the second stage of the LDO, first stage being the error amplifier. The width of the pass element is chosen to be large for the reason that it can source a large amount of load current through it maintaining the low dropout voltage.

$$w/l = (2*I_{load})/(K_p V_{dropout}^2) \quad (1)$$

The pass element can be a NMOS transistor. But the gate drive difficulties of an NMOS transistor make it unsuitable for the low drop out applications. The PMOS can function as pass element for the dropout voltage of 0.1 to 0.2V.

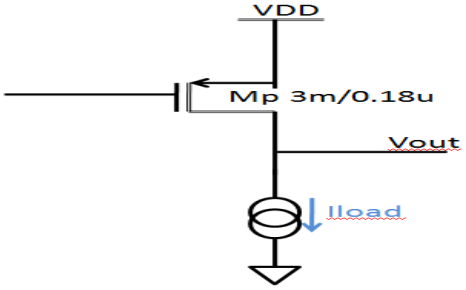

Fig.2: Pass Element with size

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B. *Error Amplifier*

The difference between the output voltage and the reference voltage feeds the error amplifier as an error signal. This forms the negative feedback path. The error amplifier acts as the active correction component in the system. The output of the error amplifier feeds the pass transistor which operates as a common source stage to overcome any voltage headroom. The gate voltage of the pass element is adjusted to meet the required output voltage and current conditions. Error amplifier requires high DC gain to ensure good accuracy, load and line regulation[3].

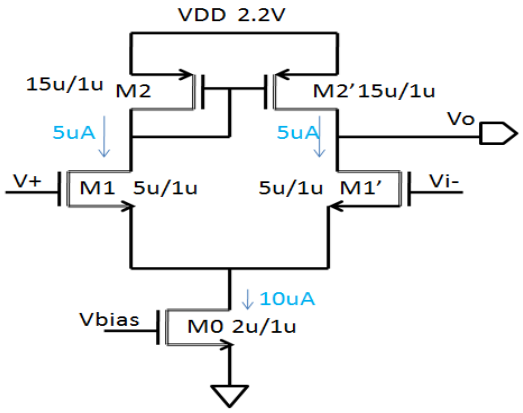

Fig.3: 5pack architecture of Error Amplifier

C. *Feedback Network*

A part of the output voltage provided by the feedback network is compared with the reference voltage by an error amplifier. The output of an error amplifier which controls the gate voltage of the pass transistor regulates the output voltage. The resistor divider network can be used as the feedback network. The resistor ratio is decided by the ratio of the output voltage to the reference voltage.

$$V_{ref} = V_{fb} = V_{out} * R2/(R2+R1) \quad (2)$$

III. Stability Analysis

The stability analysis of a LDO system must be done considering the pass element, error amplifier, output capacitor, equivalent series resistance and the feedback network[1]. The output capacitor has a crucial role to play in stability of LDO. For the system to be stable the output capacitance is chosen to be large in the range of micro farads. But a large output capacitance cannot be integrated in the chip which leads to manufacturing of the LDO with a off-chip external capacitor.

$$f_{p1} = 1/(2\Pi C_0 (Ro_{-pass}+R_{ESR})) \quad (3)$$

$$f_{p2} = 1/(2\Pi C_{par1} R_{oa1}) \quad (4)$$

$$f_{p3} = 1/(2\Pi C_{par2} R_{par2}) \quad (5)$$

$$f_{z1} = 1/(2\Pi C_0 R_{ESR}) \quad (6)$$

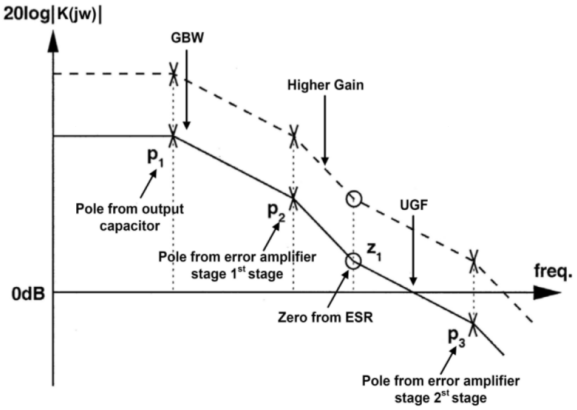

Fig.4: Pole-zero plot for a basic LDO architecture [1].

The absence of the large external capacitor is provided by an internal high frequency path. The differentiator provides fast transient sensing path and internal AC compensation. The feedback capacitance C_f senses the change in the output voltage and converts it to a corresponding current. This current is injected into the gate capacitance of the pass transistor using a current amplifier. The differentiator contributes a pole at the frequency $1/(RC_f)$ and a zero at the zero frequency[2].

IV. Simulation Results

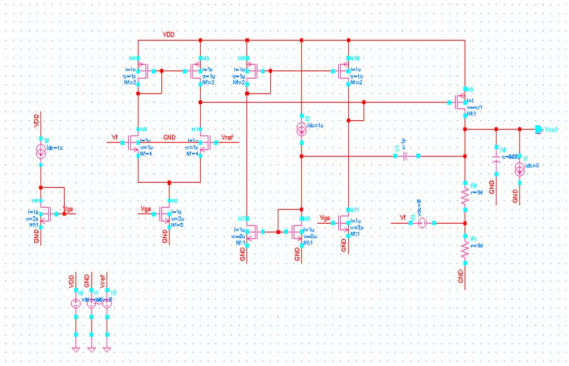

Fig.5: Schematic of the LDO in Cadence

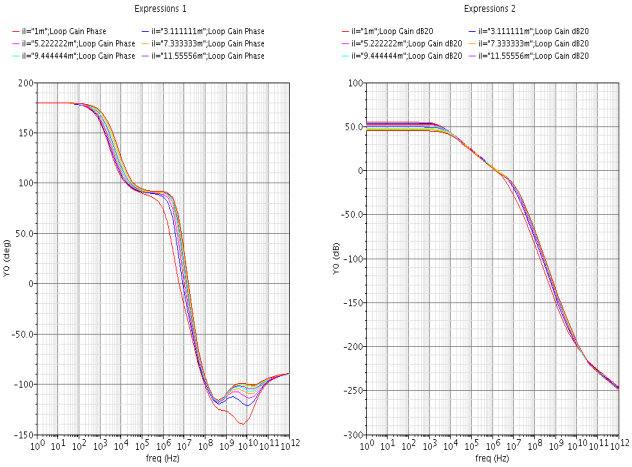

Fig.6: Gain and Phase plots for Load Variations

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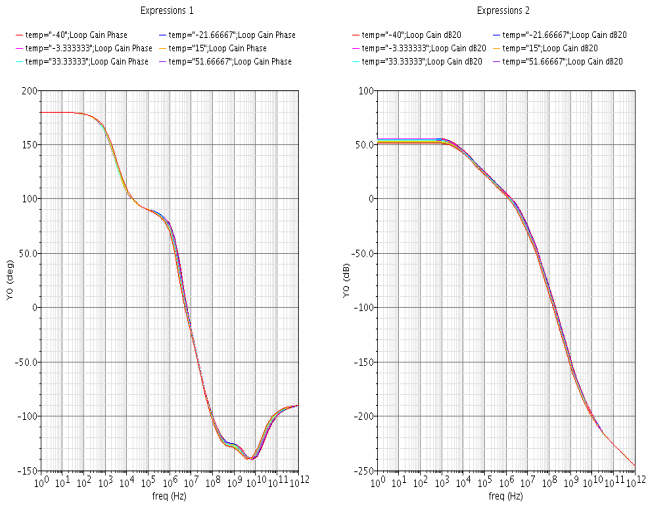

Fig.7: Gain and Phase plots for temperature variation at 1mA load current\

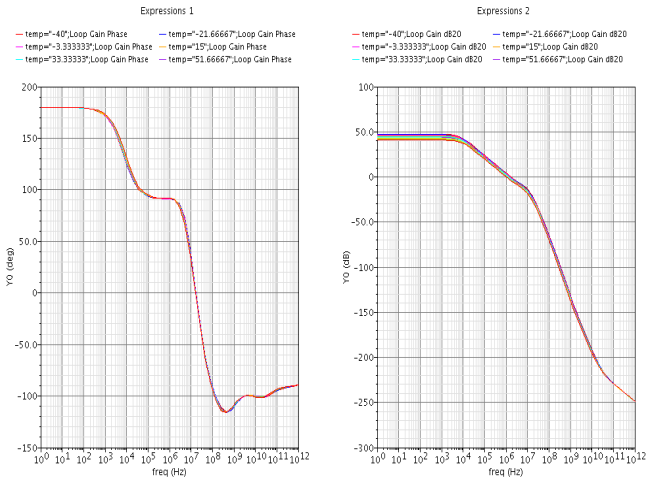

Fig.8: Gain and Phase plots for temperature variations at full load.

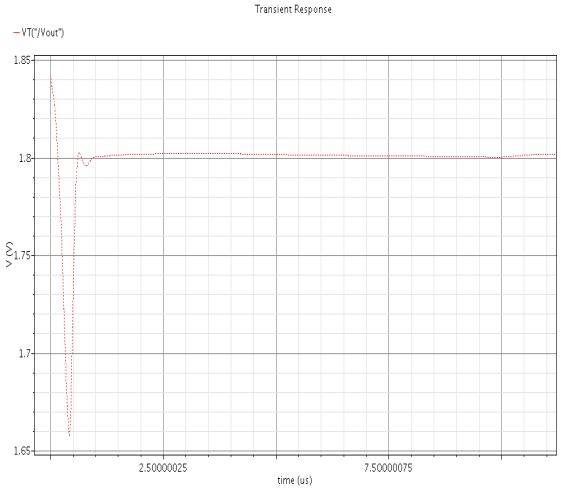

Fig.9: Settling time for transient change in load current.

V. Conclusion

This work describes the design strategy of LDO voltage regulators. Simulations are run for different process corners, supply variations, load variations and load current variations. The designed LDO has a DC gain of 56dB with a phase margin of 60° for the varying load of 1mA to 20mA, i.e., 5% to 100% variation. The settling time is found to be 1us. The results are verified for the temperature variations from -40 to 125 degree Celsius. The circuit consumes a total of 15uA current in no load condition. The fast transient compensation is demonstrated with a current mirroring technique using a capacitor of 800pF.

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