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Modeling and Design of Highly EMI Immune CMOS OpAmp Topologies

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***Abstract*—This paper gives a review of the modeling and design of CMOS Miller operational amplifier (OpAmp) and folded cascode (FC) operational amplifier that has high immunity to electromagnetic interference (EMI). The highly EMI immune CMOS Miller OpAmps and folded cascode OpAmps have distinctive features, such as low output offset voltage and moderate power when compared to the classical Miller OpAmp and the classical folded cascode OpAmp presented in the literature. The EMI immune CMOS OpAmps take advantage of the replica concept combined with the source-buffered technique in order to achieve high EMI immunity across a wide range of frequencies (1 MHz to 1 GHz). The highly EMI immune CMOS OpAmps are designed using the first-order quadratic mathematical model. The modeling equations for the output offset current are derived and validated for CMOS OpAmps, taking into account both the body effect and channel length modulation. The circuits has been fabricated/designed using 0.18 μm mixed-mode CMOS technology. The performance result shows that the maximum EMI-induced output offset voltage for these CMOS OpAmps are less than 7 mV over an extensive frequency range from 1 MHz to 1 GHz, which is approximately 97 % lower when compared to the traditional CMOS OpAmps.**

***Index Terms*—EMI, Miller OpAmp, Robust Miller OpAmp, Compact Miller OpAmp, Folded cascode OpAmp, Robust folded cascode OpAmp, compact folded cascode OpAmp**

I. Introduction

The Integrated Circuit (IC) technology growing very expeditiously in the recent years. As the technology changes rapidly, the challenges for electronic circuit design is increasing day by day. The semiconductor fabrication has introduced improved technology to handle high-density circuitry, higher clock rates, which helps in faster data transfer processing for cloud computing, artificial intelligence (AI), gaming, and virtual reality (VR). However, electromagnetic interference (EMI) can cause unpredictable behavior in ICs, leading to malfunctions, data corruption. Ensuring EMI immunity helps in maintaining the reliability of electronic systems. In addition, the electronic industry is growing very abruptly, and the adoption of EMI immunity is on the rise for electronic gadgets with evolving EMI standards [5]-[15]. The EMI is becoming an increasing concern in the recent years, due to high level of electronic circuit integration in a small space of Ic's, and system levels. The effect of EMI on electronic systems can arise from a wide variety of sources like mobile phones, laptop, computers, satellites and many electronic gadgets [1]-[12]. The EMI poses significant challenges in medical and sensor systems that capture low-amplitude signals, such as electroencephalogram (EEGs) and bio medical signals. In EEGs, the signals received from patients typically range from few μV to few mV, with 3 dB cutoff frequencies at 0.05 Hz and 100 Hz [18]-[20]. Designing EMI-resistant circuits and systems has become mandatory for most safety-critical device applications [15]-[17].

There are few solutions available in the literature to design EMI immune CMOS Miller OpAmps [3]-[16] and classical folded-cascode OpAmp (CFCO) topologies [29]-[31]. The available solutions are based on cancellation, cross coupling, replication and source buffering. However, they strive from more power expenditure and larger area, and are unable to achieve low output offset voltage (OOV) across a wide range of frequency. The main focus of this work is to address these issues by comparing all the available EMI immune CMOS Miller OpAmps and folded cascode OpAmps (FCO) in 0.18 μm mixed-mode CMOS technology. In the EMI immune CMO and FCO, the OOV is minimized by employing a low pass filter (LPF) at low to mid frequencies and the source-buffered topology at high frequencies. The two concepts together provides a low OOV for the both CMOS OpAmp topologies over a wide range of frequencies. The solution is unique compared to the existing EMI immune CMOS OpAmps. The modeling equations led to the solution, enabling wide-band operation while maintaining moderate power consumption and minimal area. The CMOS OpAmp topologies utilises the intuitions developed from the results derived from the modeling equations are discussed in the following sections. Additionally, this work provides a thorough review and comparability with existing EMI-immune topologies like CMO, robust Miller OpAmp, compact Miller OpAmp and CFCO,robust FCO and compact FCO.

The paper is organised as follows: in Section II, the CMO with the modelling equations are presented along with the solutions to reduce the OOV. Section III discuss about the FCO with the proposed EMI immune low power FCO and compact FCO. Section IV details the performance results and provides a comparison among the CMOS Miller OpAmps and FCO topologies. Finally, Section V concludes the paper.

II. CMOS Miller OpAmp Topologies with high EMI Immunity

A. Classical Miller OpAmp

The CMO is one of the very important analog circuit which has very high gain precision circuit. The CMO is used in various analog applications and it is very sensitive to EMI [9]. A DC OOV is produced at the output of the CMO, due

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to the asymmetric slew rate and the non-linearity of the first stage of the Miller OpAmp, when an EMI signal is applied at the input terminal of the OpAmp [12]. This DC output offset alters the correct DC biasing of the connected analog circuits.

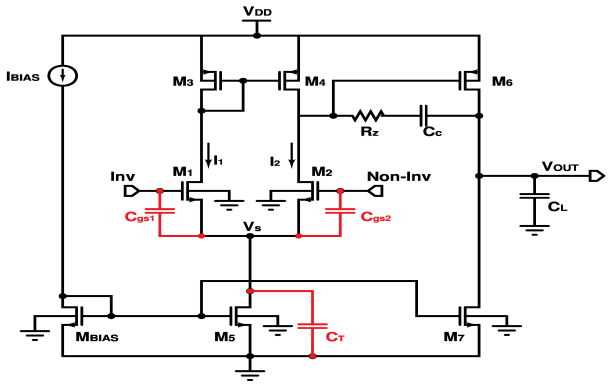

Fig. 1. Classical Miller OpAmp

The circuit diagram for the CMO is shown in Fig. 1. The OOV is produced due to the mismatch between the drain currents I_1 and I_2 and the parasitic coupling between the input capacitance's (C_{gs1}) of transistor M_1, M_2 and the tail capacitance (C_T) of M_5. The tail node capacitance of M_5 transistor behaves like a short circuit when the frequency is increasing and it introduces a mismatch between the drain currents of I_1 and I_2, when the CMO is connceted in voltage follower configuration. The standard OOC I_{os} is given by:

$$I_{os} = \overline{I_1} - \overline{I_2} \tag{1}$$

The MOS transistor drain current, I_i (I_1 and I_2), in saturation region [2], including the body effect and the channel length modulation (CLM) is given by [18]:

$$I_i = \beta\left[\left((G_i)^2 + (v_{xi}(t))^2 + (2K_i v_{xi}(t))\right) \times \left(1 + \lambda_i V_{DSi} + \lambda_i v_{dsi}(t)\right)\right] \tag{2}$$

where i = 1, 2, and
$G_i = V_{GSi} - V_{t0} - \gamma_i\left(\sqrt{2\phi_F + V_{SBi}}\right) + \gamma_i\left(\sqrt{2\phi_F}\right)$,

$v_{xi}(t) = v_{gsi}(t) - \frac{g_{mbi}}{g_{mi}} v_{sbi}(t)$.

where g_{mi} is the transconductance and g_{mbi} is the bulk transconductance, respectively.

The simplified and elaborated OOC equation is given in (3). The average value of the time-varying small-signal (v_{gs} and v_{bs}) is assumed to be zero in the simplified equation, with the assumption that $V_{GS1} = V_{GS2}, \gamma_1 = \gamma_2, V_{DS1} = V_{DS2}, V_{SB1} = V_{SB2}$,
$\lambda_1 = \lambda_2 \quad and \quad K_1 = K_2$.

The equation (3), will give the complete information of OOC and its parameters which will affect the OOC. The OOV is given by:

$$V_{os} = \frac{Ios}{g_{m1}} \tag{4}$$

The modeling equations are validated for the first stage of the CMO as the offset is coming mainly from the first stage. The spectre simulations are compared with the MATLAB and are shown in Fig. 4 [18]. The maximum OOV of the CMO is 187.19 mV at 1 GHz, when a 900 mVpp EMI signal is applied at the input of the CMO [18].

B. Highly EMI Immune OpAmp-1:Robust Miller OpAmp

The CMO provides a higher OOV over a wide range of frequencies. The aim of the circuit designer is to have a very less OOV for the entire frequency range with out altering the main specifications. One of the possible solution to have a very low OOV is by using a Low Pass Filter (LPF) at the input of the CMO. The LPF effectively rejects any out-of-band differential-mode and common-mode EMI disturbances that are superimposed on the input signal. The CMO with the LPF reduces the OOV (less than 10 mV), however, low Phase Margin (PM) of CMO makes it impractical to use. A Modified Replica Miller OPAmp (MRMO) is proposed to overcome the stability issues. The MRMO employs a LPF between an inner differential pair and an outer differential pair, with diode-connected load transistors M3 and M4a as dipicted in Fig.7 [18]. This configuration allows the MRMO to deliver a low OOV (10 mV) over a broad frequency range starting from 1 MHz to 200 MHz. The tail capacitance dominates at very high frequencies, hence the OOV voltage increases beyond 200 MHz.

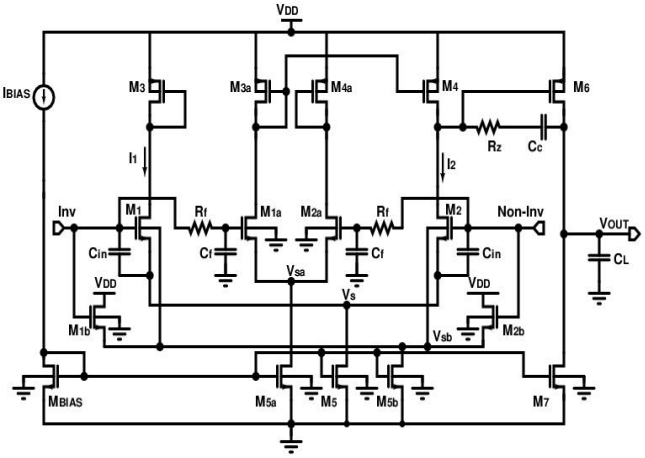

Fig. 2. Robust Miller OpAmp

It is necessary to have a low OOV over a wide band of frequencies up to 1 GHz. The OOV at high frequencies can be reduced to less than 10 mV using another popular concept, know as Source Buffered technique. The source buffered Miller OpAmp (SBMO) [18] is designed to deliver a low OOV at higher frequencies. This source buffered topology contains main differential papir and an auxiliary differential pair. The auxiliary differential pair (M_{1a},M_{2a} and M_{5a}), has its tail node connected to the body terminals of the main transistors M_1 and M_2. The auxiliary differential pair bootstraps the bulk source voltage of M_1 and M_2 and maintains the average drain current constant [12],[18], and [20]. The modeling equations

$$I_{OS-DIFFAMP} = \beta\left(1+\lambda_1 V_{DS1}\right)\left[\overline{v_{g1}^2(t)} - \overline{v_{g2}^2(t)}\right] - \left[2\beta\left(1+\lambda_1 V_{DS1}\right)\left(1+\frac{g_{mb1}}{g_{m1}}\right) + 2\beta K_1\lambda_1\right]\left[\overline{v_s(t)v_{id}(t)}\right] + 2\beta K_1\lambda_1\left[\overline{v_{g1}(t)v_{d1}(t)} - \overline{v_{g2}(t)v_{d2}(t)}\right] - \left(1+\frac{g_{mb1}}{g_{m1}}\right)2\beta K_1\lambda_1\left[\overline{v_s(t)v_{d1}(t)} - \overline{v_s(t)v_{d2}(t)}\right], \quad (3)$$

developed for the source buffered technique allow for the the placement of two additional gate capacitance's C_{in} at the gate source terminals of transistors M_1 and M_2. The extra gate source capacitance C_{in} calculated value is 300 fF. The SBMO provides a low OOV of less than 10 mV beyond 200 MHz, as the tail capacitance increases. The combination of MRMO with the SBMO gives a low OOV (10 mV) over a wide range of frequencies from 1 MHz to 1 GHz. The resulted amplifier is called as the Robust Miller OpAmp (RMO). The RMO circuit diagram is shown in Fig. 2.

The modeling equations are derived for the first stage of RMO in a similar way to the CMO and the simplified OOC is given in equation (5). It is perceivable from the equation, the OOC is cancelled, when compared to the first stage OOC expression of the CMO. The OOV equation is given in (4). The node voltage V_s, V_{sa}, V_{sb}, V_{d1a}, V_{d1}, V_{d2a} and V_{d2} expressions are given in [18]. The modeling equations for the first stage of the RMO is validated with the spectre simulations and MATLAB are shown in Fig. 15 [18]. The OOV for the RMO is plotted and simulated using the Spectre simulator is shown in Fig. 3. The RMO is connected in voltage follower configuration and the OOV is compared with the CMO, when a 900 mVpp EMI signal is applied at the input of the OpAmp. The OOV for the RMO is less 10 mV at all frequencies when compared to the CMO. Table I shows the frequency-response specifications of the RMO and are compared with the CMO. The RMO power dissipation (2.5 mW) is increased by 19 %, when compared to the CMO (2.1 mW) and the maximum OOV is 10 mV.

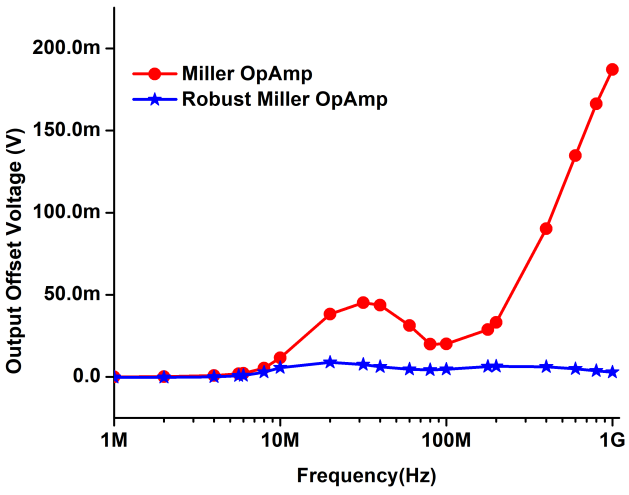

Fig. 3. Output offset voltage plot when a 900 mVpp EMI signal is applied at the input of the OpAmp

TABLE I
MAIN SPECIFICATION COMPARISON TABLE BETWEEN THE CMO AND RMO

Parameters	CMO	RMO
Gain (dB)	68	73
Phase margin (deg)	67	66
UGF (MHz)	50	43
Power (mW)	2.1	2.5

The OOV can be further reduced to a lower value (5 mV), if two Rs resistances are connected to M_1 and M_2 of the RMO . The RMO with Rs will linearise the circuit further and it provides an OOV of 5 mV over extensive range of frequencies up to 1 GHz [21].

C. Highly EMI Immune OpAmp-2:Compact Miller OpAmp

The RMO and RMO with source degeneration provides a low OOV over a vast range of frequencies. But, the power dissipation of the RMO is 19% excessive of the CMO. Is there any way, we can reduce the power dissipation to a lower value? A new circuit topology is proposed to lower the power consumption close to the CMO and less than the RMO. The key idea is generated from the modeling equations. From equation (5), it is observed that, the OOC is reduced due to the LPF up to medium frequency range (200 MHz) and cancelled because of the source-buffered nature at higher frequencies (after 200 MHz) [21]. The circuit diagram of RMO, contains three differential input pair structures. The extra differential pair is used, to cancel the output offset current at higher frequencies. If we can use the source-buffered nature with out the extra differential pair, the power consumption will be reduced to a lower value. This is realisable, as we have already two differential pairs.

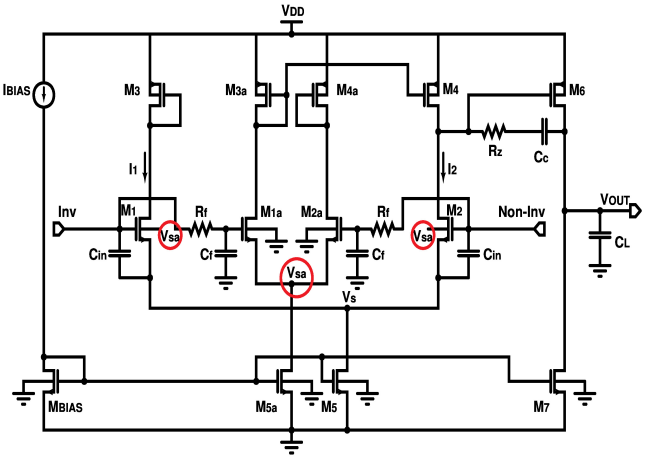

Fig. 4. Compact Miller OpAmp

The body of the outer differential pair transistors M_1 and M_2 are connected to the inner differential pair tail node (V_{sa}).

$$I_{OS-ROBUST} = \beta\left(1+\lambda_1 V_{DS1}\right)\left[\overline{v_{g1}^2(t)} - \overline{v_{g2}^2(t)}\right] - \left[2\beta\left(1+\lambda_1 V_{DS1}\right)\left(1+\frac{g_{mb1}}{g_{m1}}\right) + 2\beta K_1\lambda_1\right]\left[\overline{v_s(t)v_{id}(t)}\right]$$
$$+2\beta K_1\lambda_1\left[\overline{v_{g1}(t)v_{d1}(t)} - \overline{v_{g2}(t)v_{d2}(t)}\right] - \left(1+\frac{g_{mb1}}{g_{m1}}\right)2\beta K_1\lambda_1\left[\overline{v_s(t)v_{d1}(t)} - \overline{v_s(t)v_{d2}(t)}\right]$$
$$+2\beta\left(1+\lambda_1 V_{DS1}\right)\frac{g_{mb1}}{g_{m1}}\left[\overline{v_{sb}(t)v_{id}(t)}\right] + \left(\frac{g_{mb1}}{g_{m1}}\right)2\beta K_1\lambda_1\left[\overline{v_{sb}(t)v_{d1}(t)} - \overline{v_{sb}(t)v_{d2}(t)}\right], \quad (5)$$

The resulted new circuit is called as Compact Miller OpAmp and can only be implemented in a twin-tub process [12],[18], and [21] due to the bulk biasing. The circuit diagram for the compact Miller OpAmp is shown in Fig. 4.

The modeling equations developed for the RMO will remain same for the Compact Miller OpAmp. The OOC equation is given in equation (5). The only change for the Compact Miller OpAmp is the node V_{sb} is changed to V_{sa}. As we observe from equation (5) it is very clear that, the OOC is getting canceled. The highlighted blue color terms are getting canceled with the red color. Thanks to the LPF for giving a low OOV up to 200 MHz and the source-buffering technique offering the low OOV at very higher frequencies beyond 200 MHz. The power dissipation of the compact Miller OpAmp reduces to 8% when compared to the RMO.

The validation of the modeling euations are carried out for the first stage of Compact Miller OpAmp. The OOC equation will remain the same as equation (5) and its OOV is given in equation (4). The node voltage expressions for V_s, V_{d1a}, V_{d1}, V_{d2a} and V_{d2} are the same as RMO. The only change is, the node voltage V_{sb} of RMO will now become V_{sa} for the compact Miller OpAmp. The validation of the modeling equations with the spectre simulations and the comparision with MATLAB can be done without much difficulty in the way same as RMO.

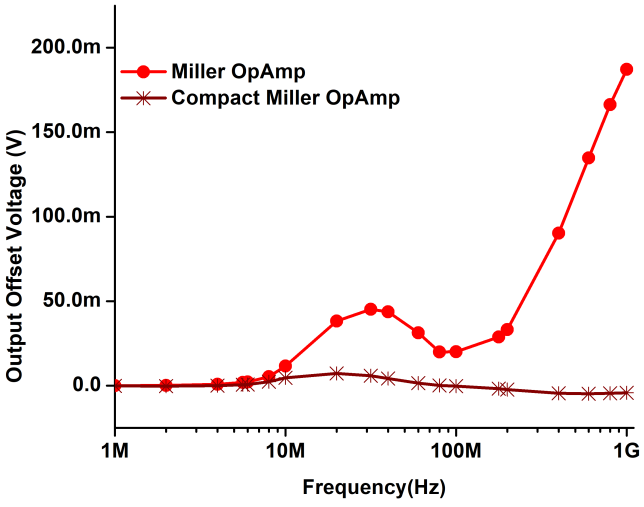

Fig. 5. Output offset voltage plot when a 900 mVpp EMI signal is applied at the input of the OpAmp

The Spectre simulations are carried out for the two stage compact Miller OpAmp, and the OOV plots are shown in Fig. 5. The OOV is compared with the CMO when a 900 mVpp EMI signal is applied at the input of the OpAmp. The power dissipation of the Compact Miller OpAmp is decreased by 8 % when compared to the RMO and its OOV stays very low at all the frequency range. The main specifications of the Compact Miller OpAmp are compared with the CMO and are given in Table II.

TABLE II
MAIN SPECIFICATION COMPARISON TABLE BETWEEN THE CMO AND COMPACT MILLER OPAMP

Parameters	CMO	Compact Miller OpAmp
Gain (dB)	68	73
Phase margin (deg)	67	67
UGF (MHz)	50	39
Power (mW)	2.1	2.3

The OOV can be further reduced to 5 mV, by connecting two Rs resistors to M_1 and M_2 of the RMO. This configuration linearises the circuit and delivers an OOV of 5 mV up to 1 GHz [21].

III. FOLDED CASCODE OPAMP TOPOLOGIES WITH HIGH EMI IMMUNITY

A. Classical Folded Cascode OpAmp

A classical CMOS OpAmp is a two stage CMOS amplifier consists of an input differential pair followed by a second stage amplifier. The CMO uses a miller compensation to maintain the stability and it is very sensitive to EMI. A folded cascode OpAmp (FCO) is another popular analog circuit used in high performance CMOS OpAmps used in Integrated Circuits. The FCO is a single stage design with a cascode configuration folded into the input stage. In certain applications where EMI immunity is a priority, the FCO is sometimes preferred over the two stage Miller OpAmp. The folding technique reduces the miller capacitance seen by the input transistor, results in improved high-frequency response and large bandwidth. The FCO is implicitly a stable structure as it is a single stage amplifier. The FCO is a symmetrical structure, which means that it can be designed to exhibit a more symmetrical slew-rate when compared to the Miller OpAmp architecture. The FCO has a reduced EMI offset at low to mid frequencies [29]-[31]. The circuit diagram of the FCO is shown in Fig.8. A DC OOV is generated at the output port of the FCO, when an EMI signal is applied at the input of the FCO. The resulted DC OOV is mainly due to the non-linear distortion introduced by the input differential pair of the FCO.

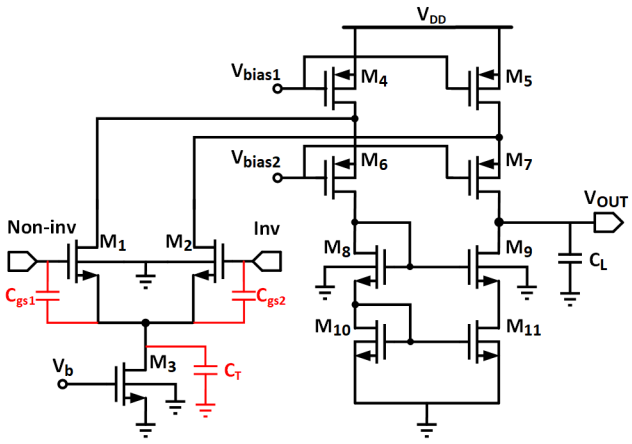

Fig. 6. Circuit diagram of FCO

The OOV in the FCO is mainly due to the mismatch between the two currents of I_1 and I_2. The mismatch is created because of the capacitive coupling between (C_{gs1} and C_{gs2}) of the input differential pair (M_1, and M_2) along with the tail node capacitance (C_T) of transistor M_3. The tail node capacitance of the transistor M_3 starts behaving as a short circuit at very high frequencies. The OOC I_{os} is given in equation (1) which is same as the CMO OOC. The drain current of the MOS transistor in saturation [2] is expressed by I_i (I_1 and I_2) is given in equation (2). The OOC expression is simplified in the same way as the CMO and is given by equation (3) and its OOV is given by equation (4).

The modelling equations are developed and validated for the first stage of FCO [32]. This FCO has been designed in 0.18 µm CMOS technology with a supply voltage of 3.3 V and the aspect ratio of the transistors are same as to what is reported in [31]. When a 1.7 Vpp EMI signal is applied at its input port is the FCO, delivers a maximum OOV up to 300 mV.

B. Highly EMI Immune Folded Cascode OpAmp-1: Robust Folded Cascode OpAmp

The amount of OOV provided by the FCO is very high (up to 300 mV) at high frequencies. One of the possible solution is to use a LPF at the input of FCO [32]. The LPF rejects any out-of-band EMI effectively. The RC LPF cut-off frequency is selected to be 800 KHz, as the FCO starts increasing the OOV in the mid range of frequencies. The LPF FCO gives a low OOV, but the phase margin will become very poor, which makes it impractical to use. A replica folded cascode OpAmp (RFCO) is proposed [32] to overcome the stability issues.

In RFCO a LPF is placed between an inner differential pair and an outer differential pair and the outer differential pair is driven from the inner differential pair to provide a low OOV (6 mV) up to 300 MHz. The RFCO shows a higher OOV after 300 MHz as the tail capacitance C_T will act as a short circuit at higher frequencies. As a circuit designer the aim is to have a less OOV over a wide range of frequencies. To reduce the OOV at high frequencies another popular concept known as Source Buffered technique. In source buffered concept, the body of the main differential pair transistors (M1 and M2) are biased by an auxiliary differential amplifier (M1a and M2a). The OOV is very low (6 mV) at high frequencies (after 300 MHz) for the source bufferred folded cascode OpAmp (SBFCO) [32].

The RFCO with SBFCO is known as robust folded cascode OpAmp(Robust FCO). The robust FCO offers an OOV 6 mV over a wide frequency range up to 1 GHz. The robust FCO circuit diagram is shown in Fig. 7.

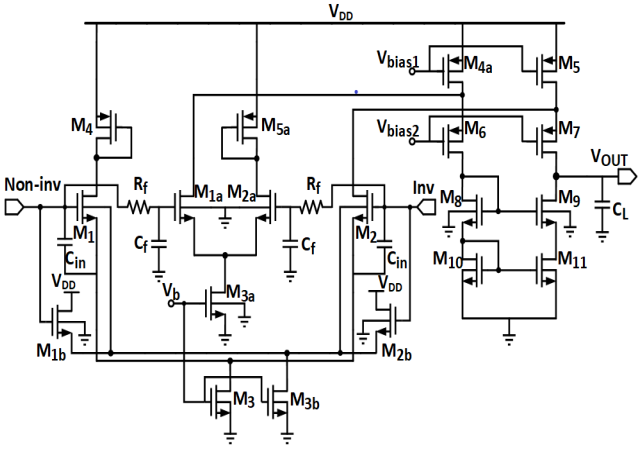

Fig. 7. Circuit diagram of a robust FCO

The validation of the modeling equations are carried out for the input stage of the robust FCO and the OOC is given in equation (5). The OOC for the robust FCO is cancelled in comparison with the OOC expression of the FCO, and the OOV is given by equation (4).

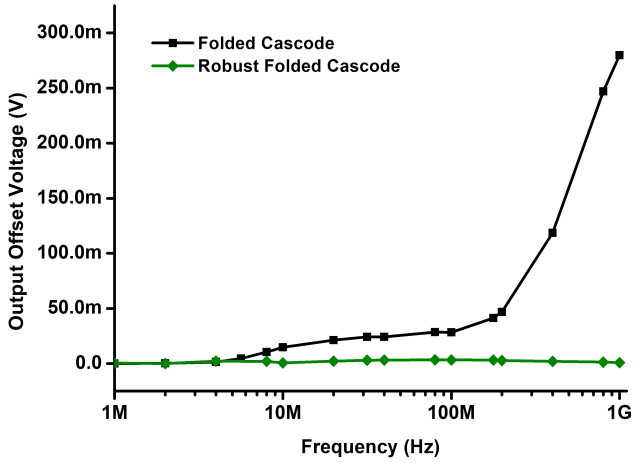

Fig. 8. Output offset voltage plot when a 1.7 Vpp EMI signal is applied at the input of the OpAmp

The Cadence spectre simulations are carried out for the Robust FCO and is shown in Fig. 8. The OpAmps are connected in a voltage follower configuration with a 1.7 Vpp EMI signal is applied at their input port. The OOV of the Robust FCO is limited to 6 mV and outperforms at all the frequency range when compared to the FCO. The low OOV is achieved at a cost of additional power consumption of 1.3

mW when compared to the FCO power consumption. The main specifications of the Robust FCO are given in Table VI and are compared with the FCO.

TABLE III
MAIN SPECIFICATION COMPARISON TABLE BETWEEN THE FCO AND ROBUST FCO

Parameter	FCO	Robust FCO
Gain (dB)	60	61
Phase margin (deg)	85	88
UGF (MHz)	23.7	11.6
Power (mW)	1.3	2.6

C. Highly EMI Immune Folded Cascode OpAmp-2: Compact Folded Cascode OpAmp

While achieving low OOV, the robust FCO consumes twice the power dissipation when compared by the FCO. Can we reduce the power dissipation in comparable to the FCO and lower than the robust FCO is the next question. This is possible by observing the modeling expressions derived, especially from equation (5). The OOC is reduced, due to the LPF at low frequency range and cancellation at high frequencies due to the source buffered concept.

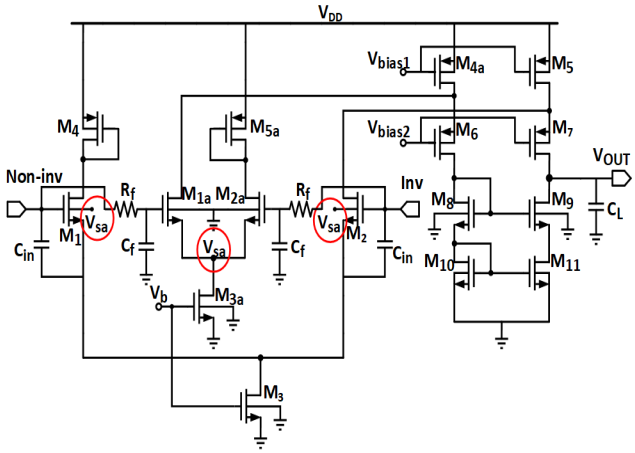

Fig. 9. Circuit diagram of a compact FCO

If we can provide the source buffered topology with out the auxiliary differential pair M_{1b}, M_{2b} and M_{3b} transistors the power dissipation will be reduced. This is possible if the outer differential pair input transistor M_1, M_2 bodies connected to the inner differential pair. The new circuit topology is named as compact folded cascode OpAmp (Compact FCO). The power dissipation for the compact FCO is reduced by 23% when compared to FCO. As the body is connected to the inner differential pair source terminal, the compact FCO can only be implemented in a twin-tub process [34] due to the body biasing. The circuit diagram for the compact FCO is shown in Fig. 9.

The modeling equations and its validation is carried out for the input stage of the compact FCO and the OOC expression remains the same as equation (5). The OOV is given in equation (4). The only change for the compact FCO is the node V_{sb} is changed to V_{sa}. The compact FCO has 23% power saving when compared to the robust FCO. The validation of the input stage compact FCO modeling equations are given in [34].

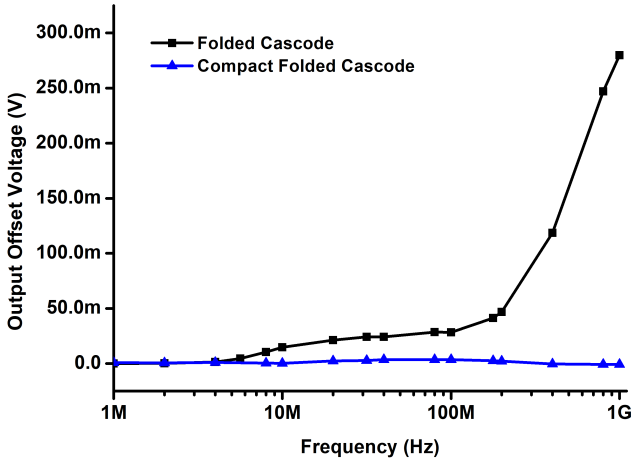

Fig. 10. Output offset voltage plot when a 1.7 Vpp EMI signal is applied at the input of the OpAmp

The Cadence specture simulations are performed for the compact FCO and is shown in Fig. 10. The OOV of the compact FCO is 6 mV over the entire frequency range up to 1 GHz, when compared with the FCO. The both the OpAmps are connected in voltage follower configuration when a 1.7 Vpp EMI signal is applied at their input port. The compact FCO outperforms in terms of OOV, power dissipation and area. The maximum OOV is 6 mV, the power dissipation is 23% and 10% area reduction when compared to the robust FCO. The main specifications of the Compact FCO are given in Table V and are compared with the FCO.

TABLE IV
MAIN SPECIFICATION COMPARISON TABLE BETWEEN THE FCO AND COMPACT FCO

Parameter	FCO	Compact FCO
Gain (dB)	60	61
Phase margin (deg)	85	88
UGF (MHz)	23.7	11.8
Power (mW)	1.3	2

IV. SIMULATION RESULTS AND COMPARISON AMONG THE CMOS MILLER OPAMP AND FOLDED CASCODE OPAMP TOPOLOGIES

The frequency response specifications and the OOV mesaurements are carried out for all the CMOS Miller OpAmps- the CMO, the RMO, the compact Miller OpAmp, and the compact Miller OpAmp with R_s were designed using a standard 0.18 µm CMOS process with 1.8 V supply voltage. The design aims to achieve a DC gain of 68 dB, a PM of 65°, a Unity Gain Frequency (UGF) of 50 MHz, and an input common-mode range (ICMR) of 0.6 V to 1.6 V. A load of 10 pF (C_L) was considered. The cutoff frequency of the LPF components R_f - C_f was set at 800 kHz. All the circuits use identical transistor dimensions to enable a fair comparison among the topologies [21]. The values of R_Z and C_C were tuned to ensure stability [12], [18] and [21].

All the five CMOS OpAmp topologies are connected in voltage follower configuration and are subjected to a 1 Vpp EMI signal at the non-inverting terminal and the OOV is

TABLE V
COMPARISON AND SUMMARY OF THE HIGHLY EMI IMMUNE CMOS OPAMP TOPOLOGIES

Parameter	CMO	RMO [18]	RMO with Rs [21]	Compact Miller OpAmp [21]	Compact Miller OpAmp with Rs [21]
Power (mW)	2.1	2.5	2.5	2.3	2.3
Maximum Offset Voltage (mV) when EMI = 1Vpp @ 20 MHz	45.7	9.5	6.6	7.7	4.6
Area (in μm)	125 X 99	166 X 186	166 X 186	160 X 183	160 X 183
Mean when EMI = 900 mVpp @ 1 GHz temp= 70 and VDD= 1 V	183.2 m	-	-	-	5.7 m

TABLE VI
COMPARISON AND SUMMARY OF THE HIGHLY EMI IMMUNE FOLDED CASCODE OPAMP TOPOLOGIES

Parameter	FCO	Robust FCO [34]	Compact FCO [34]
Gain (dB)	60	61	61
Phase margin (deg)	85	88	88
UGF (MHz)	23.7	11.6	11.8
3-dB BW (kHz)	21	19	19
CL (pF)	10	10	10
Power (mW)	1.3	2.6	2
Area (μm^2)	2294	35875	32287
EMI Immunity	NO	YES	YES
Maximum Offset Voltage (mV) when EMI = 1.7 Vpp @ 1 GHz	265.8	6.7	6.6

plotted as shown in Fig. 11. It is very clear from the OOV plot, the OOV stay less than 9 mV for all the EMI immune CMOS OpAmps.

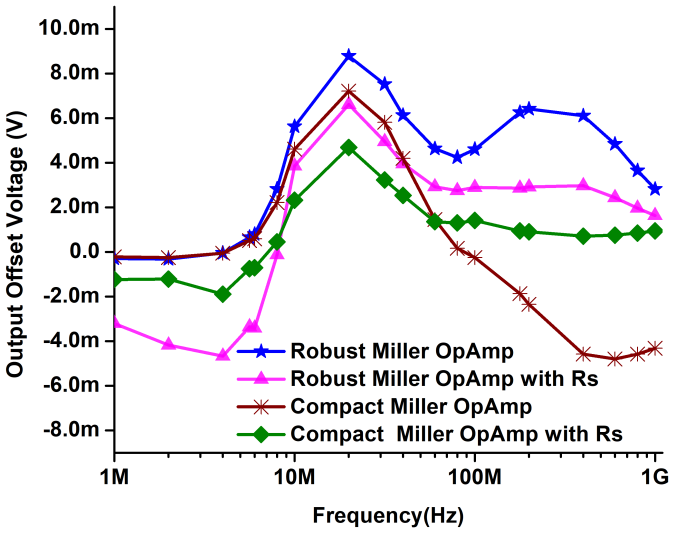

Fig. 11. Output offset voltage plot when a 1 Vpp EMI signal is applied at the input of the OpAmp

The folded cascode OpAmp and the highly EMI immune folded cascode OpAmps-the robust FCO, and the compact FCO are configured in voltage follower to measure the OOV and in an open loop configuration to find the frequency response specifications. All the FCO designed using a standard 0.18 µm CMOS process with 3.3 V supply voltage. The FCO's are aimed to achieve a DC gain of 60 dB, a PM of 80°, a UGF of 25 MHz, and an ICMR of 0.9 V to 2.6 V. A load of 10 pF (C_L) was used and the cutoff frequency of the R_f - C_f LPF was set at 800 kHz.

All the three FCO circuit topologies are designed with identical feature sizes to ensure a fair comparison and are excited with a 1.7 Vpp EMI signal at the non-inverting terminal and the OOV is plotted as shown in Fig. 12. It is noticeable from the plot that, the robust FCO and the compact FCO gives a very low OOV (5 mV) when compared to the solutions available.

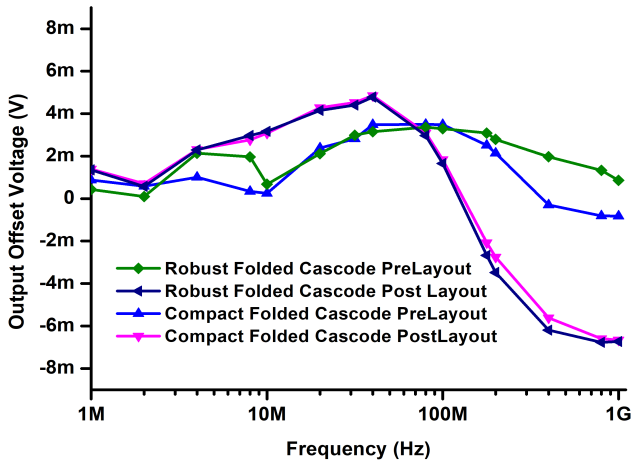

Fig. 12. Output offset voltage plot when a 1.7 Vpp EMI signal is applied at the input of the OpAmp

The main frequency response specifications summary of all the CMOS OpAmp topologies and the folded cascode OpAmp topologies are given in Table VI and Table VII. The both tables shows that the compact Miller OpAmp and the compact folded cascode OpAmp outperform the available CMOS OpAmps and folded cascode OpAmps.

V. CONCLUSION

This paper presents a review of CMOS Miller OpAmps and folded cascode OpAmps that exhibit high immunity to EMI while maintaining low power consumption, small area, and low output offset voltage across a wide frequency range. The highly EMI-immune CMOS Miller OpAmps and the folded cascode OpAmps demonstrate lower power dissipation compared to other CMOS OpAmp topologies. Additionally, modeling equations for OOC are derived and validated for these EMI-immune CMOS Miller OpAmps and folded cascode OpAmps, taking into account the body effect and channele length modulation.

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