# Capless LDO Regulator Achieving −76 dB PSR and 96.3 fs FOM

Seong Jin Yun, *Student Member, IEEE*, Jeong Seok Kim, *Student Member, IEEE*, and Yong Sin Kim, *Member, IEEE*

***Abstract*—The performance of switching devices such as display driver ICs is degraded by large power supply noise at switching frequencies from a few hundreds of kilohertz to a few megahertz. In order to minimize the power supply noise, a low-dropout (LDO) regulator with higher power supply rejection (PSR) is essential. In this brief, a capless LDO regulator with a negative capacitance circuit and voltage damper is proposed for enhancing PSR and figure of merit (FOM), respectively, in switching devices. The proposed LDO regulator is fabricated in a 0.18 $\mu$m CMOS. Measurement results show that the proposed LDO regulator achieves −76 dB PSR at 1 MHz and 96.3 fs FOM with a total on-chip capacitance of as small as 12.7 pF.**

***Index Terms*—Low-dropout (LDO) regulator, negative capacitance, power supply rejection (PSR).**

## I. Introduction

THE INCREASING demands for larger display and higher resolution have meant that display driver ICs (DDIs) have been developed with more driving channels. This has led to larger switching current and larger supply noise at the switching frequency range from a few hundreds of kilohertz to a few megahertz [1]. As a result, the perturbed bias voltage of each pixel due to the supply noise degrades the display quality. In order to overcome this problem, a low-dropout (LDO) regulator with higher power supply rejection (PSR) for the aforementioned frequency range is generally required. Several LDO regulators with high PSR have been proposed over the last few years [2]–[6]. However, these conventional LDO regulators require a large external output capacitor, which prevents their use in fully integrated system-on-chip designs; capless LDO regulators are thus preferred in these applications [7]–[13].

Several techniques can be used to achieve high PSR performance in designing capless LDO regulators. The supply noise shielding technique in [7] uses an nMOS cascode transistor with its gate biased separately as a source follower, in order to prevent the entire regulator from fluctuating caused by the power supply noise. However, this technique is not suitable for most applications due to the high dropout voltage and the poor transient response. To overcome these drawbacks, the feed-forward supply-noise cancellation technique was proposed in [8], but it exhibits poor PSR performance due to the sensitivity in the variations of the input voltage and the load current. Another method with the power supply ripple injection filter was proposed in [1], although its PSR performance is limited because the ripple rejection accuracy purely depends on the passive elements of the filter. In contrast to both of these methods (with the maximum load capacitance of less than 100 pF), a capless LDO regulator with the load capacitance larger than 100 pF was presented in [9]. However, the PSR of the aforementioned capless LDO regulators is limited to −41 dB PSR at 1 MHz [1], [7]–[9]. To achieve −70 dB PSR at 1 MHz, the feed-forward current injection technique was introduced in [10] at the expense of large on-chip capacitance of 28 pF and a poor figure of merit (FOM) of 290 fs.

This brief presents a capless LDO regulator that achieves high PSR performance and superior FOM while using the smallest on chip capacitance compared to other capless LDO regulators. This brief is organized as follows. The proposed PSR enhancing scheme is presented in Section II. Design considerations for the fundamental circuit blocks are discussed in Section III. Simulation and experimental results of the proposed LDO regulator are presented in Sections IV and V, respectively, followed by the conclusion in Section VI.

## II. Proposed LDO Regulator

### A. Basic Structure

The proposed negative capacitance circuit (NCC) allows for higher PSR performance with a simpler and smaller circuit. Fig. 1 shows the fundamental blocks of the proposed LDO regulator composed of an error amplifier (EA), a pass transistor $M_P$, a frequency compensator (FC), the voltage damper (VD), and the NCC. $C_L$ and $R_L$ refer to the load capacitor and load resistor, respectively, which are externally connected for the test. The proposed LDO regulator adopts the conventional FC for a phase margin higher than 60° [10]. The NCC is modeled as a variable capacitor with a negative value. The main path of the supply noise in the conventional LDO regulator is the supply voltage coupled through the gate-source and the gate-ground parasitic capacitances of $M_P$. The coupled gate-source

Manuscript received September 6, 2016; revised November 7, 2016; accepted November 13, 2016. Date of publication November 15, 2016; date of current version September 25, 2017. This work was supported in part by the Basic Science Research Program through the National Research Foundation of Korea within the Ministry of Science, ICT and Future Planning under Grant NRF-2014R1A1A1003771 and in part by Samsung Electronics. This brief was recommended by Associate Editor H.-J. Chiu.

The authors are with the School of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail: flamental@korea.ac.kr; hanshin06@korea.ac.kr; shonkim@korea.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2016.2628965

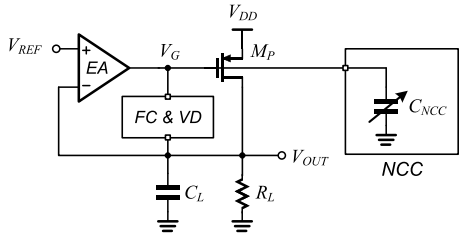


Fig. 1. Fundamental blocks of the proposed LDO regulator.

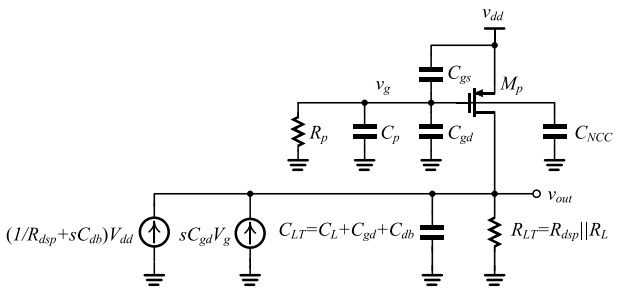


Fig. 2. Small-signal equivalent circuit of the proposed LDO regulator.

voltage from the supply is converted into a current through $M_P$, resulting in PSR performance degradation by affecting the output voltage of the LDO regulator. The NCC cancels the supply noise coupling effect by adding the negative capacitance, $C_{\rm NCC}$, to the gate node of $M_P$, which enhances the PSR performance significantly at a certain frequency range.

### B. Small-Signal Analysis of the Proposed LDO Regulator

Fig. 2 shows the small-signal equivalent circuit of the proposed LDO regulator. $R_p$ and $C_p$ are the parasitic resistance and capacitance, respectively, which include EA, FC, and VD. $C_{\rm gs}$ and $C_{\rm gd}$ represent the parasitic capacitances of the gate-source and the gate-drain of $M_P$, respectively. The two voltage controlled current sources, $(1/R_{\rm dsp}+sC_{\rm db})v_{\rm dd}$ and $sC_{\rm gd}v_g$, are the feed-forward paths due to the drain-bulk parasitic capacitance of $M_P$, $C_{\rm db}$, and $C_{\rm gd}$, respectively. The total load resistance $R_{\rm LT}$ meets $R_{\rm LT} = R_{\rm dsp}||R_L$, where $R_{\rm dsp}$ is the drain-source parasitic resistance of $M_P$. Since the effect of these current sources in the PSR performance is trivial, they can be neglected in the small signal analysis [10]. In the conventional LDO regulator without $C_{\rm NCC}$, the small signal gate voltage of $M_P$, $v_g$, can be approximated as

$$v_g = \frac{sC_{\rm gs}}{\frac{1}{R_p} + s\big(C_{\rm gs}+C_p+C_{\rm gd}\big)}v_{\rm dd} \cong \frac{C_{\rm gs}}{C_{\rm gs}+C_p+C_{\rm gd}}v_{\rm dd}. \tag{1}$$

Note that $R_p$ is large enough for $1/R_p$ to be ignored [10]. Therefore, $v_g$ can be approximated as a linear function of the small signal supply voltage $v_{\rm dd}$. In the proposed LDO regulator, the correlation between $v_g$ and $v_{\rm dd}$ in (1) can be eliminated at the expense of an additional capacitance $C_{\rm NCC}$ at the gate of $M_P$, which can be rewritten as

$$v_g \cong \frac{C_{\rm gs}}{C_{\rm gs}+C_p+C_{\rm gd}+C_{\rm NCC}}v_{\rm dd}. \tag{2}$$

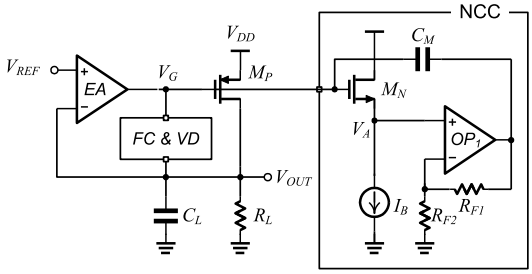


Fig. 3. Implementation of NCC with fundamental blocks.

If $C_{\rm NCC}$ cancels out the parasitic capacitances $C_p$ and $C_{\rm gd}$ as

$$C_{\rm NCC} = -\big(C_p + C_{\rm gd}\big) \tag{3}$$

then $v_g$ can be simply approximated as

$$v_g \cong \frac{C_{\rm gs}}{C_{\rm gs}+C_p+C_{\rm gd}-(C_p+C_{\rm gd})}v_{\rm dd} = v_{\rm dd}. \tag{4}$$

The small signal gate-source voltage of $M_P$ is approximated to zero as $v_{\rm gs} = v_g - v_s = v_{\rm dd} - v_{\rm dd} = 0$, which means the small signal output voltage $v_{\rm out}$ is zero and thus enhances PSR by eliminating the supply voltage induced noise through $M_P$.

## III. Circuit Implementation

### A. Negative Capacitance Circuit

The circuit diagram of NCC shown in Fig. 3 is the implementation of the negative capacitance discussed in (3). NCC includes the noninverting amplifier with $OP_1$, $R_{F1}$, $R_{F2}$, and the miller capacitor $C_M$. The equivalent capacitance $C_{\rm NCC}$ can be modulated by the Miller effect as

$$C_{\rm NCC} = C_M(1-A_{CL}) = C_M\left\{1-\left(1+\frac{R_{F1}}{R_{F2}}\right)\right\} = -\frac{R_{F1}}{R_{F2}}C_M \tag{5}$$

where $A_{CL}$ is the closed loop gain of the non-inverting amplifier. To control the negative capacitance $C_{\rm NCC}$, a feedback resistor $R_{F1}$ or $R_{F2}$ can be digitally controlled. Consequently, this scheme has two advantages as follows.

1) The value of negative capacitance can be optimized according to the operating conditions,
2) On-chip capacitance $C_M$, of which the maximum value is equal to $C_p + C_{\rm gd}$, can be minimized by depending on the ratio of the feedback resistors $R_{F1}$ and $R_{F2}$.

While the source follower $M_N$ is not necessary for implementing the NCC, it reduces the voltage level of $V_A$ for the required headroom range of $O_{P1}$.

### B. Voltage Damper

Since a capless LDO regulator cannot take advantage of a large decoupling capacitor for absorbing the voltage spike at the output when the load current is abruptly changed, fast load-transient performance is one of the most important features of a capless LDO regulator. The conventional capless LDO regulators generally adopt additional transient enhancing schemes at the expense of larger power dissipation [14]–[18].

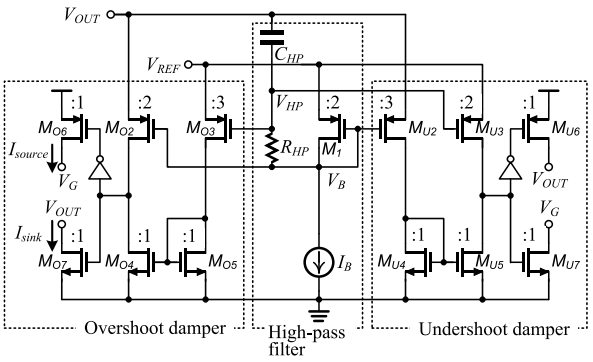


Fig. 4. Detailed circuit diagram of the proposed VD.

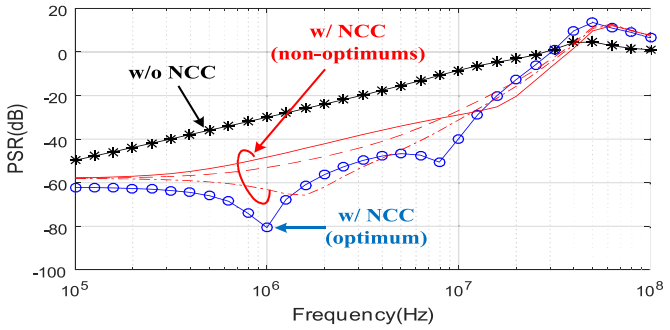


Fig. 5. Simulated PSR performance of the proposed LDO regulator with and without NCC at 50 mA load condition.

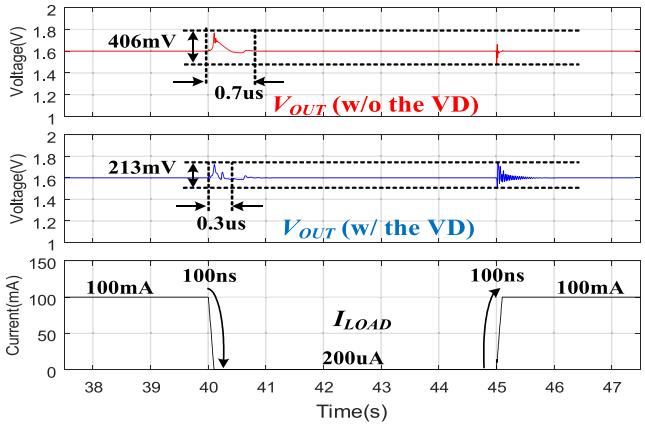


Fig. 6. Simulated load transient response of the proposed LDO regulator with and without the VD.

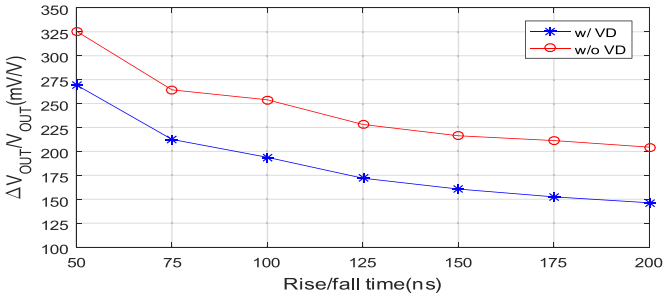


Fig. 7. Simulated $\Delta V_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ of the proposed LDO regulator with and without VD under various rise/fall time.

In the proposed LDO regulator, a VD is proposed as a simple transient enhancing scheme with its stand-by current of less than 1% of the overall quiescent current.

The circuit diagram of the proposed VD shown in Fig. 4 is composed of a high-pass filter, an overshoot damper, and an undershoot damper. In the high-pass filter, any abrupt change in $V_{\mathrm{OUT}}$ is transferred to $V_{\mathrm{HP}}$, while the dc bias is supplied by $V_B$. The overshoot damper consists of an asymmetrical input stage (the common-gate amplifier of $M_{O2}$ and the common-source amplifier of $M_{O3}$), active loads ($M_{O4}$ and $M_{O5}$), and p/nMOS switches ($M_{O6}$ and $M_{O7}$). When the overshoot voltage is applied to the asymmetrical input stage, the gate-source voltage of $M_{O2}$ increases and vice versa for $M_{O3}$. This mitigates the overshoot by increasing both the current $I_{\mathrm{source}}$ to the $V_G$ node and $I_{\mathrm{sink}}$ from the $V_{\mathrm{OUT}}$ node.

The undershoot damper also consists of an asymmetrical input stage ($M_{U2}$ and $M_{U3}$), active loads ($M_{U4}$ and $M_{U5}$) and p/nMOS switches ($M_{U6}$ and $M_{U7}$). Similarly, the undershoot damper can mitigate undershoots at $V_{\mathrm{OUT}}$ by increasing both the source current to the $V_{\mathrm{OUT}}$ node and the sink current from the $V_G$ node. The quiescent current of VD including the bias current $I_B$ is 0.7 $\mu$A.

## IV. Simulation Results

Fig. 5 shows the simulated PSR performance of the proposed LDO regulator with and without NCC at a load current of 50 mA. The optimum PSR performance at a certain frequency range can be found by controlling the ratio of $R_{F1}/R_{F2}$ shown in Fig. 3. The maximum PSR enhancement of the proposed LDO regulator over the LDO without NCC is obtained as 50 dB at 1 MHz.

The simulated load transient responses of the proposed LDO regulator with and without VD are shown in Fig. 6. For both cases, the step load current from 200 $\mu$A to 100 mA is applied to $V_{\mathrm{OUT}}$ with its rise/fall time of 100 ns. The peak-to-peak output voltage of the proposed LDO regulator with VD is 310 mV, resulting in 23.6% reduction compared with that without VD. The simulated $\Delta V_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ of the proposed LDO regulator with and without VD under various rise/fall times is shown in Fig. 7, which shows a decrease in $\Delta V_{\mathrm{OUT}}/V_{\mathrm{OUT}}$ as the rise/fall time increases.

## V. Experimental Results

The proposed LDO regulator is fabricated in a 0.18 $\mu$m CMOS. Fig. 8 shows a microphotograph of the proposed LDO regulator. The active area of the proposed LDO regulator is 0.033 mm$^2$, excluding options for digitally controlling $R_{F2}$ and regulator. The active area of the proposed LDO regulator is 0.033 mm$^2$, excluding options for digitally controlling $R_{F2}$ and the serial-to-parallel interface. The regulated output voltage of the LDO regulator is 1.6 V for the input voltage ranging from 1.8 to 2.2 V. The total on-chip capacitance is as small as 12.7 pF. The output capacitance of 100 pF is externally added to model the power line capacitance of $V_{\mathrm{OUT}}$ node. The quiescent current varies from 71 to 101 $\mu$A under the possible load current range from 0.2 to 100 mA. The measurement setups for PSR and the load transient are shown in Fig. 9. To inject

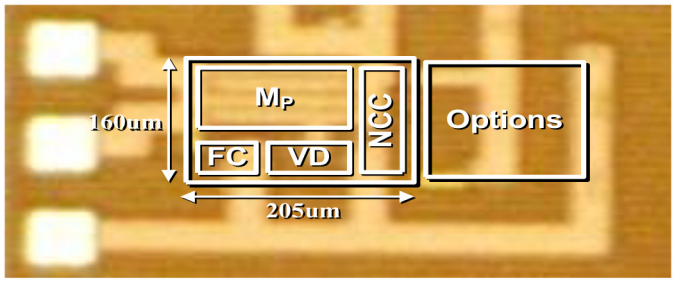


Fig. 8. Microphotograph of the proposed LDO regulator.

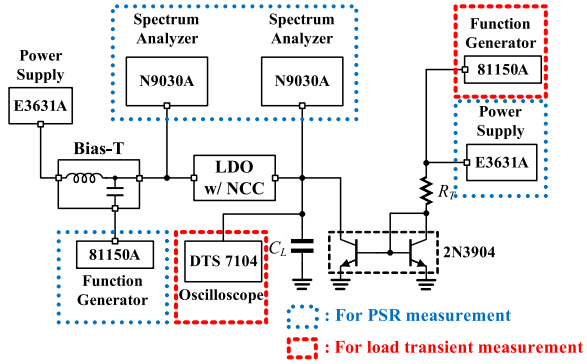


Fig. 9. Measurement setup.

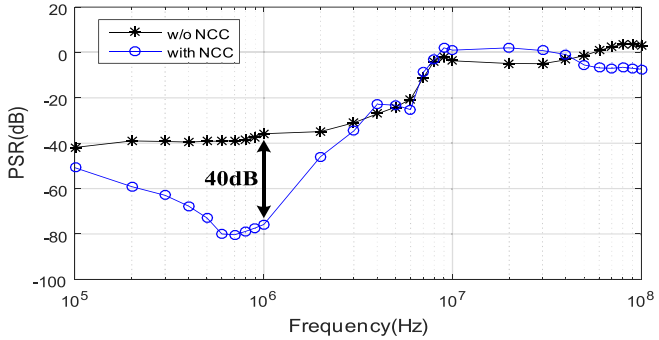


Fig. 10. Measured PSR performance of the proposed LDO regulator with and without NCC at 50 mA load condition.

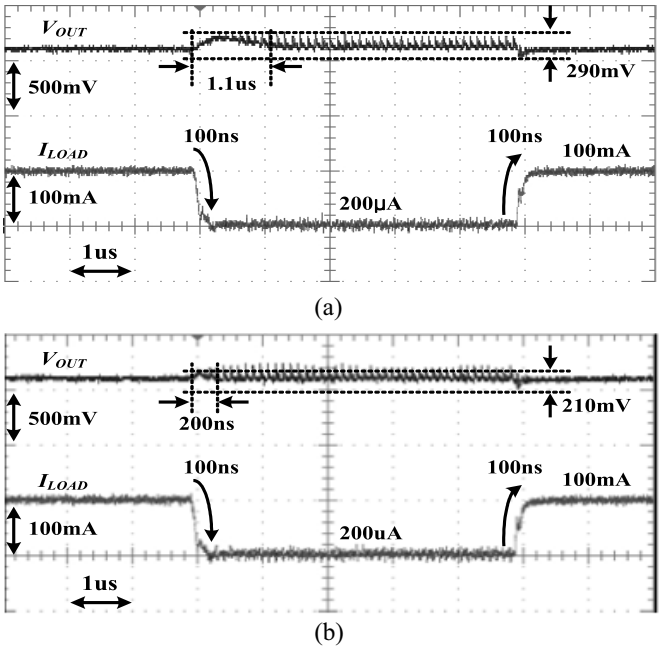


Fig. 11. Measured load transient response of the proposed LDO regulator (a) without the VD and (b) with the VD.

TABLE I
PERFORMANCE COMPARISON

| Parameter | [1] | [8] | [9] | [10] | [12] | This work |
|---|---|---|---|---|---|---|
| Year | 2012 | 2011 | 2015 | 2014 | 2015 | 2016 |
| Technology (μm) | 0.13 | 0.18 | 0.18 | 0.18 | 0.065 | 0.18 |
| $I_{LOAD,max}$ (mA) | 50 | 25 | 10 | 50 | 10 | **100** |
| $V_{OUT}$ (V) | 1 | 1.5 | 1.2 | 1.6 | 1 | 1.6 |
| $V_{DROP}$ (mV) | 200 | 300 | 600 | 200 | 150 | 200 |
| $I_Q$ (μA) | 37.32 | 300 | 265 | 80 | 50~90 | 71~101 |
| $C_{LOAD}$ (pF) | 20 | 25 | 600 | 100 | 130 | 100 |
| $C_{ON\text{-}CHIP}$ (pF) | 41 | 100 | 40 | 28 | N/A | **12.7** |
| PSR@1MHz (dB) | -40 | -40 | -41 | -70 | -21 | **-76** |
| $\Delta I_{LOAD}$ (mA) | 49.95 | 25 | 9.99 | 50 | 10 | **99.8** |
| $\Delta V_{OUT}/V_{OUT}$ (mV/V) | 94 | N/A | 36.7 | 125 | 82 | 131 |
| Edge times Δt (μs) | 0.2 | N/A | 0.05 | 0.1 | 0.0002 | 0.1 |
| Area ($mm^2$) | 0.018 | 0.041 | 0.079 | 0.14 | 0.023 | 0.033 |
| Current efficiency (%) | 99.92 | 98.8 | 97.35 | 99.84 | 99.5 | **99.93** |
| FOM* (fs) | 28.1 | N/A | 42400 | 290 | 26600 | 96.3 |

*FOM= $C_{LOAD}\Delta V_{OUT}I_Q/(\alpha\Delta I_{LOAD}{}^2)$, where $\alpha$ is a process scaling factor.

supply noise, a dc bias voltage and a sine wave are combined by using a bias tee. An input sine wave was swept from 0.1 to 100 MHz to evaluate the PSR of the proposed LDO regulator. The pulse output of the function generator is applied to the bipolar junction transistor current mirror for load transient measurement.

Fig. 10 depicts the measured PSR performance of the proposed LDO regulator with and without the NCC at a load current of 50 mA. The proposed LDO regulator with the NCC achieves 40 dB superior PSR over that without NCC in the 0.6–1 MHz range. Especially, at 1 MHz, −76 dB PSR is obtained by the proposed LDO. The PSR enhancement is rapidly decreased at frequencies over 2 MHz due to the bandwidth limitation of $OP_1$. If it is possible to increase the bandwidth of $OP_1$ using an advanced process, the PSR performance at the high frequency range can be further enhanced. Fig. 11 compares the measured load transient response of the proposed LDO regulator without VD and with VD. Similar to the simulation setups, the step load current is applied to $V_{OUT}$ from 0.2 to 100 mA with its rise/fall time of 100 ns. The proposed LDO regulator without VD shows the undershoot and the overshoot output voltages of 200 and 90 mV, respectively, and a settling time of 1.1 $\mu$s. The undershoot and the overshoot output voltages of the proposed LDO regulator with VD are reduced to 110 and 100 mV, respectively, with its settling time of 200 ns.

The proposed LDO regulator is compared with other capless LDO regulators in [1], [8]–[10], and [12] as shown in Table I, where the PSR performance and current efficiency

of the proposed LDO regulator is shown to be superior to other LDO regulators with the least amount of on-chip capacitance. The performance of the FOM of the proposed LDO regulator follows. Even though the LDO regulator in [1] exhibits the best FOM, its $\Delta V_{\mathrm{OUT}}$ is measured at the rise/fall time of 200 ns unlike those of 100 ns in [7] and [10], and this brief.

## VI. Conclusion

A capless LDO regulator for enhancing PSR is proposed. The proposed LDO regulator achieves −76 dB PSR and 96.3 fs FOM with a total on-chip capacitance of as small as 12.7 pF. The proposed LDO regulator can be widely used for any fully integrated switching device where high PSR and better FOM are required while occupying a small area.

## References


[1] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 356–360, Jun. 2012.

[2] K. Wong and D. Evans, "A 150mA low noise, high PSRR low-dropout linear regulator in 0.13μm technology for RF SoC applications," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Montreux, Switzerland, Sep. 2006, pp. 532–535.

[3] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sánchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.

[4] A. P. Patel and G. A. Rincon-Mora, "High power-supply-rejection (PSR) current-mode low-dropout (LDO) regulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 11, pp. 868–873, Nov. 2010.

[5] Y.-S. Yuk *et al.*, "A CMOS LDO regulator with high PSR using gain boost-up and differential feed forward noise cancellation in 65nm process," in *Proc. IEEE Eur. Solid-State Circuit Conf. (ESSCIRC)*, Bordeaux, France, Sep. 2012, pp. 462–465.

[6] Y.-S. Yuk *et al.*, "PSR enhancement through super gain boosting and differential feed-forward noise cancellation in a 65-nm CMOS LDO regulator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 10, pp. 2181–2191, Oct. 2014.

[7] V. Gupta and G. A. Rincon-Mora, "A 5mA 0.6μm CMOS Miller-compensated LDO regulator with -27dB worst-case power-supply rejection using 60pF of on-chip capacitance," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, Feb. 2007, pp. 520–521.

[8] B. Yang, B. Drost, S. Rao, and P. K. Hanumolu, "A high-PSR LDO using a feedforward supply-noise cancellation technique," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2011, pp. 1–4.

[9] J. Zarate-Roldan, M. Wang, J. Torres, and E. Sánchez-Sinencio, "A capacitor-less LDO with high-frequency PSR suitable for a wide range of on-chip capacitive loads," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 9, pp. 2970–2982, Sep. 2016.

[10] C.-J. Park, M. Onabajo, and J. Silva-Martinez, "External capacitor-less low drop-out regulator with 25 dB superior power supply rejection in the 0.4–4 MHz range," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 486–501, Feb. 2014.

[11] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.

[12] Y. Lu, Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue, "A fully-integrated low-dropout regulator with full-spectrum power supply rejection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 707–716, Mar. 2015.

[13] C.-J. Park, J. Silva-Martinez, and M. Onabajo, "Design techniques for external capacitor-less LDOs with high PSR over wide frequency range," in *Proc. IEEE 57th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, College Station, TX, USA, Aug. 2014, pp. 342–345.

[14] P. Hazucha *et al.*, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.

[15] Y.-H. Lam and W.-H. Ki, "A 0.9V 0.35 μm adaptively biased CMOS LDO regulator with fast transient response," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2008, pp. 442–626.

[16] P. Y. Or and K. N. Leung, "An output-capacitorless low-dropout regulator with direct voltage-spike detection," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458–466, Feb. 2010.

[17] C. Zhan and W.-H. Ki, "An output-capacitor-free adaptively biased low-dropout regulator with subthreshold undershoot-reduction for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 1119–1131, May 2012.

[18] M. R. V. Bernal, S. Celma, N. Medrano, and B. Calvo, "An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 10, pp. 643–647, Oct. 2012.

[19] X. Qu, Z.-K. Zhou, B. Zhang, and Z.-J. Li, "An ultralow-power fast-transient capacitor-free low-dropout regulator with assistant push–pull output stage," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 2, pp. 96–100, Feb. 2013.