2024 IEEE Biomedical Circuits and Systems Conference (BioCAS) | 979-8-3503-5495-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/BioCAS61083.2024.10798368

A Fully Integreated Current-Mode LDO Using PSRC and APSR Technique With -71.8 dB PSRR at 6.78 MHz for Implantable Medical Device

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***Abstract*—This paper presents a fully integrated capacitor-less high PSRR LDO based on current-mode topology. A power supply ripple cancellation technique (PSRC) is proposed to improve the PSRR at high frequency. The PSRC is based on the flipped voltage follower (FVF) and the super source follower structure (SSF) is added to improve the stability of proposed LDO. The small signal of the PSRC technique is set up and the PSRR at low frequency is not affected in proposed LDO. In addition, an adjustable PSRR technique is achieved. The PSRR at the range from 100 kHz to 10 MHz can be greatly improved at a specific frequency by adjusting the value of the compensation resistance according to the working frequency of specific applications. The proposed LDO is designed in a 0.18 µm CMOS process, which achieves the PSRR of -79 dB at DC and -71.8 dB at 6.78 MHz. Moreover, the PSRR is enhanced by 30 dB at 126 MHz.**

***Index Terms*—capacitor-less, current-mode, flipped voltage follower (FVF), low-dropout regulator (LDO), power supply rejection ratio (PSRR)**

I. Introduction

The resonant wireless power transfer (WPT) is more suitable for implantable medical devices (IMDs) compared with the inductive WPT [1]. Fig. 1 shows a scheme for wireless power transformation in IMDs. Although the long distance of two coils of resonant WPT is an advantage, the working frequency of 6.78 MHz is much higher than the inductive WPT of 200 kHz. The low-dropout regulator (LDO) connected after rectifier can filter the power supply noise of 200 kHz easily [2]–[5]. However, how to improve the power supply rejection ratio (PSRR) of LDO at high frequency has received widespread attention and research for resonant WPT in IMDs.

Recently, voltage-mode LDOs [6], [7] are widely used and researched. In the voltage-mode (VM) LDO, the output of the error amplifier (EA) directly controls the gate voltage of the power transistor. The gate-to-source voltage V_{GSP} changes from the threshold voltage V_T to the supply voltage V_{IN}. Therefore, the power transistor can not always work in the saturation region in the voltage-mode LDO, and the DC-gain and the PSRR of power transistor are variable within the whole output current range. This is an inherent drawback of the voltage-mode LDO.

In [8], the current-mode (CM) architecture of LDO is proposed, as shown in Fig. 2 (a). The current mirror is composed of the transistors M_{P1} and M_P. The transistor M_N

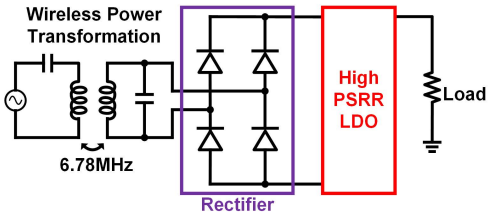

Fig. 1. Scheme for wireless power transformation in implantable medical devices.

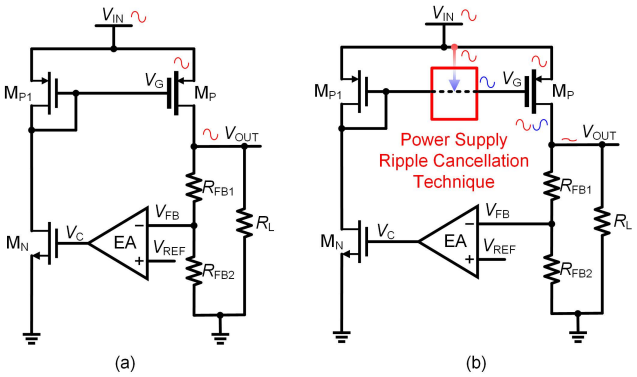

Fig. 2. The current-mode LDO. (a) Proposed CM-based LDO with the PSRC technique. (b)

works as a voltage-to-current converter to transfer the control voltage V_C to the drain current of M_{P1}. The drain current of M_{P1} is converted to the load current I_{Load} by the current mirror. The DC-gain and the PSRR are high within the whole output current range since M_P always works in the saturation region. However, the power supply ripple couples to the gate voltage of M_P through M_{P1}, and the PSRR is low at high frequency.

To solve the above issues, this paper proposes a high PSRR capacitor-less LDO based on the current-mode LDO topology. A power supply ripple cancellation technique (PSRC) is proposed to improve the PSRR at high frequency of the LDO, as shown in Fig. 2 (b). The compensating ripple is generated by the PSRC and injected into the gate voltage of the power transistor M_P. The power supply ripple is rejected by the

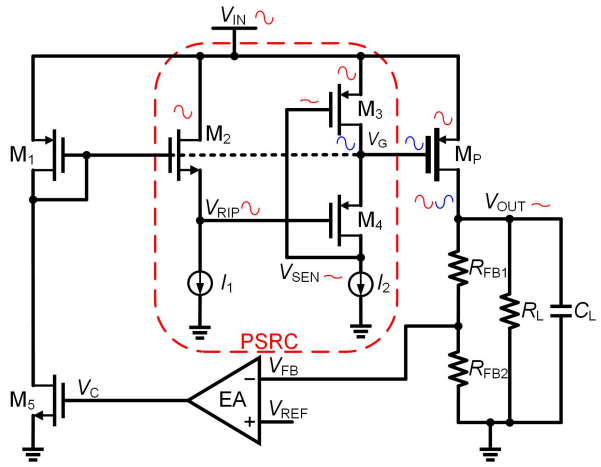

Fig. 3. Schematic of proposed LDO with the FVF-based PSRC technique.

compensating ripple, and the PSRR is extended to the high frequency. The proposed PSRC is composed of the flipped voltage follower (FVF) and the supper source follower (SSF). By analyzing the small signal of the PSRC, the PSRR at high frequency is improved by the PSRC, and the PSRR at low frequency is not affected. Furthermore, an adjustable PSRR technique (APSR) is proposed to greatly improve the PSRR at a specific frequency.

The rest of this paper is organized as follows. Section II introduces the overall schematic of the proposed high PSRR LDO, and analyzes the PSRR by using the small-signal model. The simulation results are presented in Section III. Finally, we conclude this paper in Section IV.

II. Design of the Proposed LDO

A. Proposed Power Supply Ripple Cancellation Technique

Fig. 3 shows the detailed circuit of proposed LDO with the FVF-based PSRC technique. A PMOS transistor (M_P) is used as the power transistor. The feedback voltage V_{FB} is obtained from the output voltage V_{OUT} via the feedback resistors R_{FB1} and R_{FB2}. The basic current-mode LDO is composed of the error amplifier (EA), and the transistors M_1, M_5, and M_P. The proposed PSRC which is composed of transistors $M_2 - M_4$ is a two cascaded stage. The first stage is a simple source follower, and the second stage is the flipped voltage follower (FVF). Compared to a conventional source follower, the FVF has a faster transient response, which can improve the circuit's response speed [9], [10]. Furthermore, the FVF is important to improve the stability of the circuit because it is a negative feedback structure.

The proposed buffer significantly enhances the PSRR at high frequency. The PSRR at high frequency is analyzed as follows. The power supply ripple is injected into the drain of M_2 and the source of M_3. The power supply ripple is amplified by M_2, and the signal V_{RIP} which is the output of M_2 is in the same phase as the power supply ripple. The signal V_G is composed of two signals: one is amplified from the power supply ripple by M_3, and the other is amplified

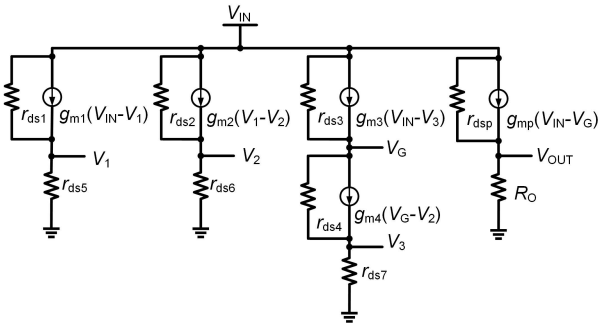

Fig. 4. The small-signal model of FVF-based PSRC technique in proposed LDO.

from the V_{RIP} by M_4. Both of them are in the same phase as the power supply ripple, so the V_G is in the same phase as the power supply ripple. A low-noise signal V_{SEN} is generated from the ground through the current source I_2, and the analysis of the V_G is not affected by the low-noise signal V_{SEN}. In addition, the FVF provides negative feedback, which helps guarantee the stability of the V_{SEN}.

According to the analysis, the V_G is in the same phase as the power supply ripple, and the magnitude of the V_G is related to the gains of transistors $M_2 - M_4$. Therefore, by adjusting the gains of these transistors, the power supply ripple can be rejected by the V_G. A low-noise output voltage V_{OUT} is achieved, and the PSRR at high frequency is improved.

B. Small-Signal Analysis of the PSRC Technique

The PSRR at high frequency can be improved by proposed PSRC technique based on the FVF, but whether the PSRR at low frequency will be affected by the buffer is uncertain. In this section, the small-signal model is used to analyze whether the PSRR at low frequency will be affected by the PSRC. The small-signal model of the proposed LDO is shown in Fig. 4. The EA and the main loop can be disconnected and the analysis and study of the small-signal model can be simplified.

In Fig. 4, the r_{ds1} is the output impedance and the g_{m1} is the transconductance of the M_1. The r_{ds2} is the output impedance and the g_{m2} is the transconductance of the M_2. The r_{ds3} is the output impedance and the g_{m3} is the transconductance of the M_3. The r_{ds4} is the output impedance and the g_{m4} is the transconductance of the M_4. The r_{ds5} is the output impedance of the M_5. The r_{dsp} is the output impedance and the g_{mp} is the transconductance of the M_P. The R_O is the load resistance. The r_{ds6} is the equivalent impedance of the current source I_1. The r_{ds7} is the equivalent impedance of the current source I_2. The KCL equations at nodes V_1, V_2, V_3, V_G, and V_{OUT} are shown in the equations (1)-(5) as follows:

$$\frac{V_{IN} - V_1}{r_{ds1}} + g_{m1}(V_{IN} - V_1) = \frac{V_1}{r_{ds5}} \tag{1}$$

$$\frac{V_{IN} - V_2}{r_{ds2}} + g_{m2}(V_1 - V_2) = \frac{V_2}{r_{ds6}} \tag{2}$$

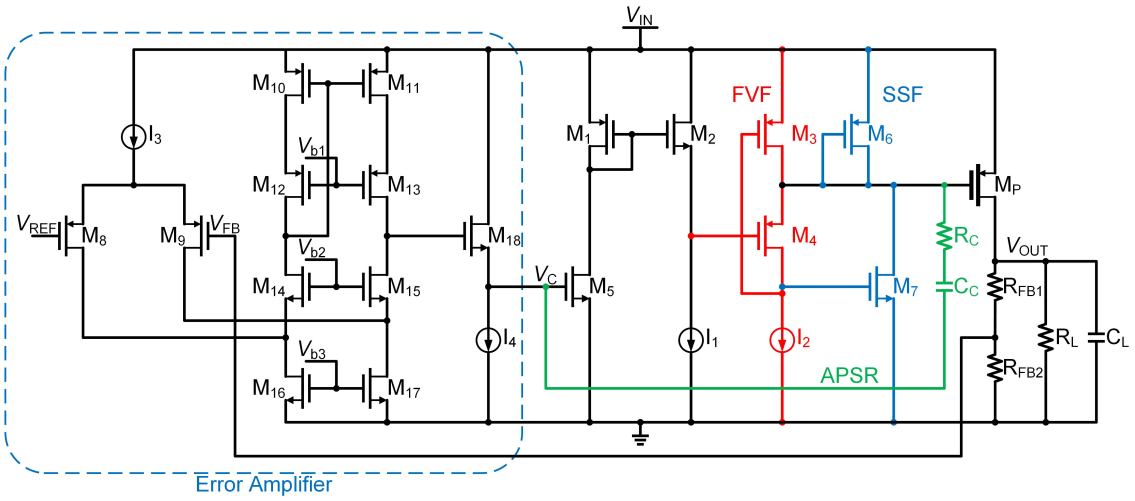

Fig. 5. The overall schematic of the proposed LDO with the FVF+SSF.

$$\frac{V_G - V_3}{r_{ds4}} + g_{m4}(V_G - V_2) = \frac{V_3}{r_{ds7}} \tag{3}$$

$$\frac{V_{IN} - V_G}{r_{ds3}} + g_{m3}(V_{IN} - V_3) = \frac{V_G - V_3}{r_{ds4}} + g_{m4}(V_G - V_2) \tag{4}$$

$$\frac{V_{IN} - V_{OUT}}{r_{dsp}} + g_{mp}(V_{IN} - V_G) = \frac{V_{OUT}}{R_O} \tag{5}$$

$$r_{dsp} = \frac{V_{OUT} L}{R_O} \tag{6}$$

The expression of r_{dsp} is shown in equation (6), where L is the gate length of M_P. The relationship between V_1 and V_{IN} can be obtained from equation (1) as shown in equation (7). Since $(g_{m1} \cdot r_{ds1} + 1) \cdot r_{ds5}$ is much larger than r_{ds5}, V_1/V_{IN} is approximately equal to 1. Similarly, equations (2)-(6) can obtain the relationship between each node and V_{IN} as shown in equations (8)-(11) respectively.

$$\frac{V_1}{V_{IN}} = \frac{(g_{m1} r_{ds1} + 1) r_{ds5}}{(g_{m1} r_{ds1} + 1) r_{ds5} + r_{ds1}} \approx 1 \tag{7}$$

$$\frac{V_2}{V_{IN}} = \frac{(g_{m2} r_{ds2} + 1) r_{ds6}}{(g_{m2} r_{ds2} + 1) r_{ds6} + r_{ds2}} \approx 1 \tag{8}$$

$$\frac{V_3}{V_{IN}} = 1 - \frac{1}{\frac{(g_{m3} g_{m4} r_{ds3} r_{ds4} + g_{m3} r_{ds3} + 1) r_{ds7}}{(g_{m4} r_{ds3} + 1) r_{ds4} + r_{ds3}} + 1} \approx 1 \tag{9}$$

$$\frac{V_G}{V_{IN}} = 1 + \frac{(g_{m3} r_{ds4} - 1)}{(g_{m4} r_{ds4} + 1)(g_{m3} r_{ds7} + 1) + \frac{r_{ds4} + r_{ds7}}{r_{ds3}}} \approx 1 \tag{10}$$

$$V_{OUT}^2 L + R_O^2 V_{OUT} = R_O^2 V_{IN} \tag{11}$$

As shown in equation (11), the V_{OUT}^2 is an infinitesimal quantity and can be neglected, so the V_{OUT} is equal to the V_{IN}. According to this result, the conclusion is that the PSRR at low frequency is not affected by the PSRC based on the FVF structure.

C. Overall Schematic of the Proposed LDO

The overall schematic of the proposed LDO is shown in Fig. 5. The EA in Fig. 3 is a two-stage EA which is composed of transistors $M_8 - M_{18}$. The first stage is a folded cascode amplifier composed of transistors $M_8 - M_{17}$, which can improve the loop gain and achieve excellent PSRR at low frequency. The second stage is a source follower composed of the transistor M_{18} and the current source I_4.

The super source follower (SSF) which is composed of transistors M_6 and M_7 is added to the FVF. The SSF also can reduce the output impedance of the FVF without affecting the DC operation of the circuit [11], [12]. The pole frequency in the gate of M_P is reduced by the low output impedance of the SSF, and the stability of the loop is improved.

D. Adjustable PSRR Technique

The resistor R_C and the capacitor C_C are connected between the gate of M_P and the gate of M_5. The PSRR at high frequency can be greatly improved at a specific frequency by adjusting the value of the R_C. With the decrease of the value of the R_C, the PSRR can be improved at a higher frequency. The value of the R_C can be flexibly adjusted according to the operating frequency of different applications so that the PSRR of the circuit can be improved at the operating frequency. In this paper, the PSRR can be adjusted in the wide frequency range of 100 kHz-10 MHz.

III. Simulation Results

The proposed fully integrated capacitor-less LDO is designed in a 0.18 μm CMOS process. The input voltage range is 2 V to 5 V, while the output voltage range is 1.2 V to 4.85 V. The minimum dropout voltage is 150 mV, and the maximum load current is 200 mA. The total on-chip capacitor is 100 pF.

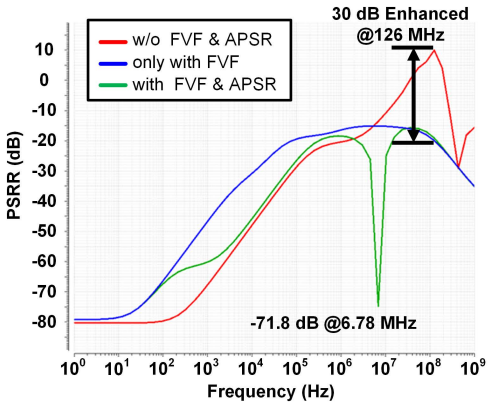

Fig. 6. Simulated PSRR of the conventional current-mode LDO and the proposed LDO.

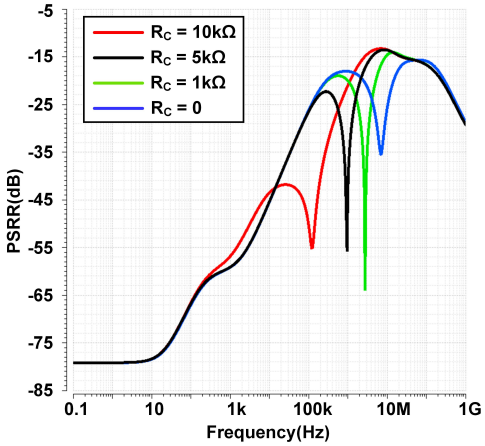

Fig. 7. Simulated PSRR of the proposed LDO at different values of R_C.

Fig. 6 compares the PSRR of the conventional current-mode LDO and the proposed LDO under the load current of 100 mA. Simulation results show that the proposed LDO and the conventional current-mode LDO both achieve good PSRR at low frequency. However, the conventional LDO does not effectively reject power supply ripple at high frequency, and the PSRR cannot be rejected around 100 MHz. In comparison, the proposed LDO achieves -71.8 dB of PSRR at 6.78 MHz. Furthermore, there is a 30 dB improvement of PSRR at 126 MHz. The simulation results prove that the proposed LDO achieves the significant rejection of power supply ripple at high frequency. Moreover, simulation results show that proposed PSRC based on the FVF structure has no effect on the PSRR at low frequency and can achieve an excellent PSRR of -79 dB.

Fig. 7 shows the simulation results of proposed LDO's PSRR for different R_C values. By adjusting the values of R_C, the greatest PSRR can be set within the frequency range from 100 kHz to 10 MHz.

Fig. 8 shows the simulation results of load regulation under different output voltage conditions. By adjusting the feedback resistors, the load regulation of the simulated circuit

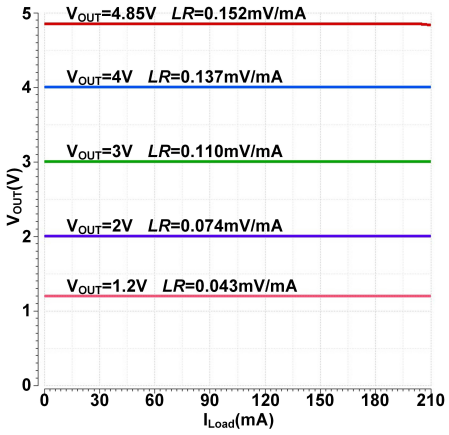

Fig. 8. Simulated the load regulation of the proposed LDO at different V_{OUT}.

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	TPEL [13]	TCASII [14]	ISCAS [15]	**This Work**
Technology(nm)	180	180	180	**180**
Capacitor-less	yes	yes	yes	**yes**
Input Voltage(V)	0.6	1.6-1.8	1.92-3.6	**2-5**
Output Voltage(V)	0.5	1.4-1.6	1.87	**1.2-4.85**
Dropout(mV)	100	200	50	**150**
Max. Load Current (mA)	0.75	50	100	**200**
Total Capacitor(pF)	N/A	0-50	4-100	**100**
Load Regulation (mV/mA)	4.77	0.194	0.00136	**0.043**
PSRR(dB)@10Hz	-22.5	-71	-65	**-79**
PSRR(dB)@100kHz	-22.5	-60	-5	**-55**
PSRR(dB)@6.78MHz	-12	-22	0	**-71.8**
PSRR(dB)@100MHz	-3	-10	N/A	**-18**

is obtained for output voltages of 1.2 V, 2 V, 3 V, 4 V, and 4.85 V. The minimum load regulation is 0.043 mV/mA.

Table I provides a comparison of capacitor-less LDOs in recent years. The proposed LDO exhibits significant advantages in PSRR, and the performance of the PSRR is excellent within the high frequency range.

IV. Conclusion

A fully integrated CM-based LDO is proposed to achieve high PSRR for implantable medical devices. A power supply ripple cancellation technique is proposed to improve the PSRR at high frequency. By analyzing the small signal of the PSRC, the PSRR at low frequency is not affected. An adjustable PSRR technique is proposed to greatly improve the PSRR at a specific frequency by adjusting the value of the compensation resistance. The simulation shows that the proposed LDO achieves -71.8 dB of PSRR at 6.78 MHz and 30 dB improvement of PSRR at 126 MHz.

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