A High-PSR LDO using a Feedforward Supply-Noise Cancellation Technique

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***Abstract*— A feed-forward noise cancellation (FFNC) technique to improve the power supply noise rejection (PSR) of a low dropout regulator (LDO) is presented. The proposed FFNC operates in conjunction with a conventional LDO and extends the noise rejection bandwidth by nearly an order of magnitude. Fabricated in 0.18μm CMOS, at 10mA load current, the prototype achieves a PSR of -50dB and -25dB at 1MHz and 10MHz supply noise frequencies, respectively. Compared to a conventional LDO, this represents an improvement of at least 30dB at 1MHz and 15dB at 10MHz. The prototype uses only 20pF load capacitance and occupies an active area of 0.04mm^2.**

I. Introduction

Supply voltages in large system-on-chips (SoCs) are generated by a switching regulators [1]. Switching power supplies are designed under tight constraints such as limited die area/board space, and low-cost passive components. Consequently, the output contains significant voltage ripple (10-50mV) which degrades the performance of precision analog and radio-frequency circuits such as high resolution data converters and low jitter phase-locked loops. Because the ripple is typically at a relatively low frequency (0.5-5MHz), suppressing it by a low-pass filter requires a prohibitively large capacitor. Additionally, coupling of switching noise from digital circuits through supply lines further exacerbates performance degradation of analog circuits. To overcome these difficulties, a low drop-out (LDO) regulator is commonly used to shield sensitive circuits from fluctuations in the supply voltage [2]–[4]. As a result, power supply rejection (PSR) of the LDO often determines the robustness of analog circuits to power supply noise.

The schematic of a conventional LDO along with its PSR curves, for two cases discussed later, is shown in Fig. 1. Using a high gain error amplifier, A_{FB}, the negative feedback modulates the impedance of the pass transistor, M_{P}, and regulates the output voltage, V_{OUT}, at the desired reference voltage, V_{REF}. The main objective of this circuit is to achieve high power supply rejection along with a low drop out voltage, small area, and low quiescent current. Unfortunately, in practice, as elucidated next, the tight coupling between these performance parameters makes the design of high-PSR LDO challenging.

The LDO, shown in Fig. 1, has two closely-spaced poles, ω_{a} and ω_{o}, at the output of the error amplifier and the LDO, respectively. While making either ω_{a} or ω_{o} dominant ensures stability, the two choices lead to very different PSR characteristics. The PSR of this feedback-based LDO, denoted

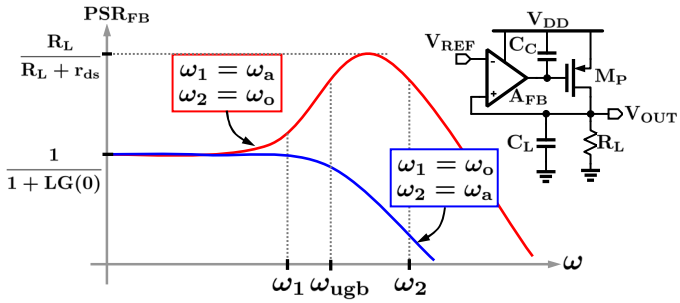

Fig. 1. Conventional LDO and its PSR characteristics.

by PSR_{FB} is given by,

$$\text{PSR}_{\text{FB}} = \frac{v_{out}(\text{s})}{v_{dd}(\text{s})} = \frac{\left(\frac{\text{R}_{\text{L}}}{\text{R}_{\text{L}}+\text{r}_{\text{ds}}}\right)}{\left(1+\frac{\text{s}}{\omega_{\text{o}}}\right)(1+\text{LG}(\text{s}))} \quad (1)$$

where LG(s) is the loop gain and R_{L} and r_{ds} denote the load resistance and the output impedance of M_{P}, respectively. Plotting Eq. 1, as shown in Fig. 1, for the two compensation scenarios reveals important design tradeoffs. For the case when ω_{a} is made dominant, loop gain rolls-off at -20dB/decade slope causing the PSR also to degrade at the same rate from ω_{a}. This degradation continues until the loop-gain unity-gain frequency, ω_{ugb}, after which PSR remains flat because the noise is only reduced by the resistive divider formed between R_{L} and r_{ds}. Beyond ω_{o}, PSR improves as load capacitor C_{L} starts to reduce the output impedance. In the second case, when ω_{o} is dominant, PSR remains constant until ω_{ugb} because the reduction in loop gain is compensated by the proportional reduction in the output impedance.

Based on the PSR curves depicted in Fig. 1, it is desirable to make ω_{o} as the dominant pole to eliminate peaking in the PSR and achieve excellent wide band supply noise rejection. However, large gate capacitance of the pass transistor, M_{P}, combined with the high output impedance of the error amplifier and low load resistance, R_{L}, mandate a very large output capacitor, C_{L}. For instance, C_{L} must be in the μF range to make ω_{o} the dominant pole and achieve good PSR. Due to the need for such a prohibitively large capacitor, fully-integrated LDOs are typically implemented by making ω_{a} dominant, at the expense of poor PSR. Using an NMOS pass transistor improves PSR, but results in a large drop out voltage [2].

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In view of these drawbacks, the focus of our work is to improve PSR without either using a big capacitor or a large drop out voltage. To this end, we present a feed-forward noise cancellation (FFNC) technique that seeks to improve high frequency PSR by cancelling the supply-noise-induced current before it appears at the load. Using the proposed FFNC, the prototype LDO improves the PSR of a conventional LDO by more than 35dB and 15dB at 1MHz and 10MHz supply noise frequencies, respectively. Unlike [4], the PSR improvement is achieved without using an external capacitor and calibration is utilized to make FFNC insensitive to process variations. Rest of the paper is organized as follows: Section II describes the proposed LDO architecture and the measured results are presented in Section III.

II. Proposed LDO Architecture

The conceptual block diagram of the proposed LDO is shown in Fig. 2. In addition to the conventional LDO, it

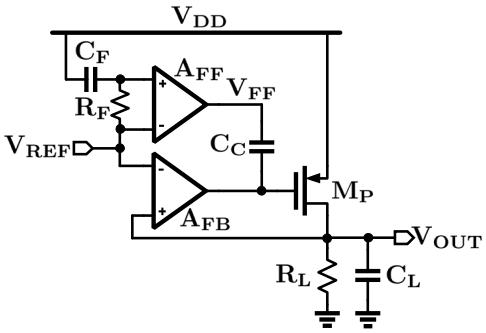

Fig. 2. Simplified schematic of the proposed LDO.

consists of a feed-forward noise cancellation path composed of a high-pass filter, formed by R_F and C_F, and amplifier, A_{FF}. By adjusting the cancellation gain (realized by varying the gain of A_{FF}) appropriately, the residual supply noise from the feedback path is cancelled, thus improving the PSR. The feed-forward and feedback paths are summed using the compensation capacitor, C_C. The two amplifiers, A_{FF} and A_{FB}, are implemented using high gain folded-cascode amplifier and wide bandwidth resistor loaded differential pair, respectively.

To understand how FFNC improves PSR, consider the small-signal model shown in Fig. 3. For simplicity, the impact of high-pass filters on PSR is ignored, thus components, R_F, C_F, and C_C are removed in the small-signal model. Using

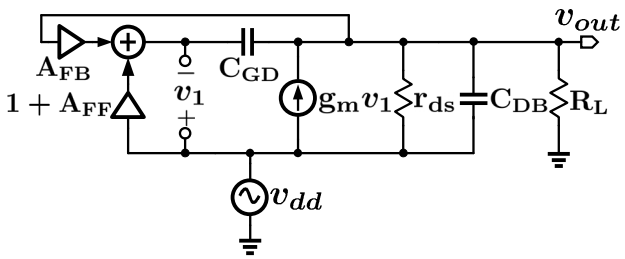

Fig. 3. Small-signal model of the proposed LDO architecture.

simple nodal analysis, and ignoring C_{GD} and C_{DB} for now, PSR of the proposed LDO can be calculated as,

$$\mathrm{PSR} = \mathrm{PSR_{FB}} \cdot (1 - g_m r_{ds} A_{FF}) \ .$$

The above equation illustrates that FFNC improves the PSR of a conventional LDO to the extent that feed-forward gain, A_{FF}, matches the reciprocal of the intrinsic gain of the pass transistor, $\frac{1}{g_m r_{ds}}$.

Including C_{GD} and C_{DB}, PSR becomes frequency dependent, as shown below,

$$\mathrm{PSR} \approx \mathrm{PSR_{FB}} \cdot \frac{(1 - g_m r_{ds} A_{FF}) \left(1 + \frac{s(C_{DB} + C_{GD}) r_{ds}}{(1 - g_m r_{ds} A_{FF})}\right)}{1 + s\,(C_L + C_{DB} + C_{GD})\,(R_L \parallel r_{ds})} \ .$$

The zero due to C_{GD} and C_{DB} degrades the PSR of FFNC at high frequencies. Even when $A_{FF} = 1/g_m r_{ds}$, the PSR degrades at -20dB/decade slope from DC. Because, R_L is typically very small, the pole occurs at a very high frequency and has negligible impact on the PSR.

The bandwidth of the feed-forward amplifier also has a detrimental impact on the PSR. With a feed-forward amplifier pole at ω_p, PSR can be calculated as,

$$\mathrm{PSR} \approx \mathrm{PSR_{FB}} \cdot \frac{(1 - g_m r_{ds} A_{FF}) \left(1 + \frac{s}{\omega_p (1 - g_m r_{ds} A_{FF})}\right)}{1 + s/\omega_p} \ .$$

The above equation reveals that ω_p also limits the effectiveness of FFNC. For instance, with the feed-forward amplifier pole at 400MHz, the maximum rejection provided by FFNC at 10MHz noise frequency is approximately 1/40, or -32dB. Therefore, maximizing the feed-forward bandwidth is key to extending the cancellation bandwidth. Intuitively, both the parasitic capacitors and the finite bandwidth cause a phase shift in the cancellation path and thus no matter how close the cancellation gain is to its ideal value, some amount of supply noise leaks to the output.

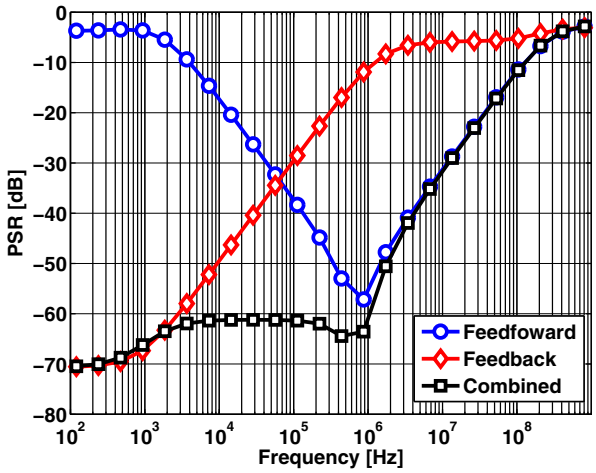

Fig. 4. Simulated PSR curves at 10mA load current and 300mV dropout.

The PSR curves obtained from transistor-level simulations of the LDO are shown in Fig. 4. The dropout voltage and the load current are equal to 300mV and 10mA, respectively. As expected, the PSR due to the feedback portion of the LDO starts to roll-up at ω_a ($\approx 20\pi$krad/s) and saturates at ω_{ugb} ($\approx 4\pi$Mrad/s). It stays fixed at approximately $\frac{R_L}{R_L + r_{ds}}$, as ω_o is at a very high frequency. On the other hand, the PSR due to FFNC starts to roll-off from the frequency of the zero due to the ac-coupling capacitor ($\approx 20\pi$krad/s) and starts to roll up due to the zeros caused by C_{GD} and the finite feed-forward amplifier pole. Thus, FFNC improves PSR beyond ω_a and extends the -50dB rejection frequency from 100KHz to about 2MHz.

The optimal feed-forward gain, as discussed earlier, is equal to the reciprocal of the intrinsic gain of the pass transistor. Because, both the transconductance, g_m, and the output impedance, r_{ds}, depend on process and bias conditions, a method to calibrate the feed-forward gain is needed. A correlation-based calibration scheme that seeks to operate in background and determines the optimal feed-forward gain is shown in Fig. 5. The noise components in the supply and the

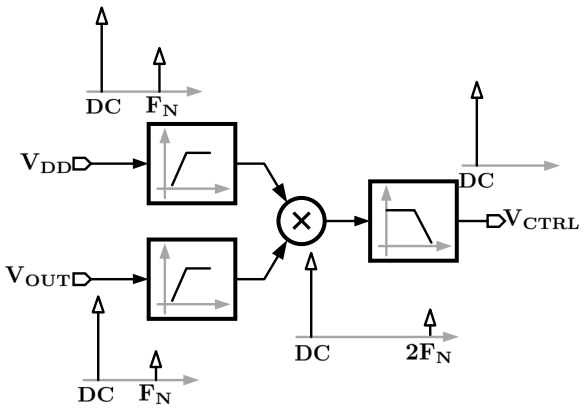

Fig. 5. Correlation-based gain calibration scheme.

output voltages, extracted using high-pass filters, are mixed to generate a DC output voltage that represents the amount of noise correlation. The high frequency component at $2F_N$ is filtered by a low-pass filter, thus generating the output voltage, V_{CTRL}, which controls the gain of the feed-forward amplifier. The mixer and the low-pass filter are implemented using a CMOS switch-based passive topology and a G_M-C_I integrator, respectively. The calibration bandwidth is designed to be much lower than the LDO loop bandwidth to avoid interaction between the two loops.

III. Experimental Results

The proposed LDO was fabricated in a 0.18μm CMOS process and the die photograph is shown in Fig. 6. It occupies an active area of 0.04mm^2 ($200\mu\text{m} \times 200\mu\text{m}$). The measured PSR curves at three different load currents, are plotted as a function of the control voltage in Fig. 7. The dropout voltage is 300mV and the noise amplitude and frequency

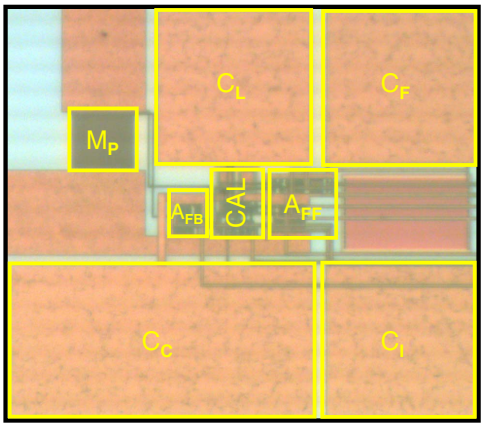

Fig. 6. Die micrograph.

are set to 30mV peak-to-peak and 2MHz, respectively. These

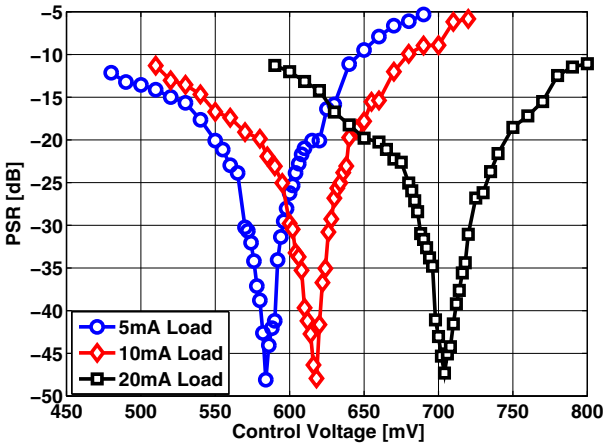

Fig. 7. Measured PSR versus the control voltage for different load currents.

plots reveal that the PSR can be controlled with a feed-forward path as proposed. Further, an optimal cancellation gain exists to achieve the highest PSR improvement. As load current increases, the gain of the pass transistor decreases, thus mandating a larger swing at the gate to replicate the same signal at the output. Consequently, the optimal control voltage increases with increasing load current, as seen in Fig. 7.

The measured PSR curves at three different load currents, are plotted as a function of the dropout voltage in Fig. 8. The load current is 10mA and the noise amplitude and frequency are set to 30mV peak-to-peak and 2MHz, respectively. At a lower dropout voltage, the output impedance of the pass transistor is smaller, thus requiring a larger cancellation voltage. As a result, the optimal control voltage increases at lower dropout voltages, as shown in Fig. 8.

Unfortunately, offset of the mixer in the calibration circuitry limited the cancellation accuracy. Because, the calibration loop converges to a control voltage that is offset from its optimal value, the supply noise could only be partially cancelled. However, transistor-level simulations performed after cancelling the

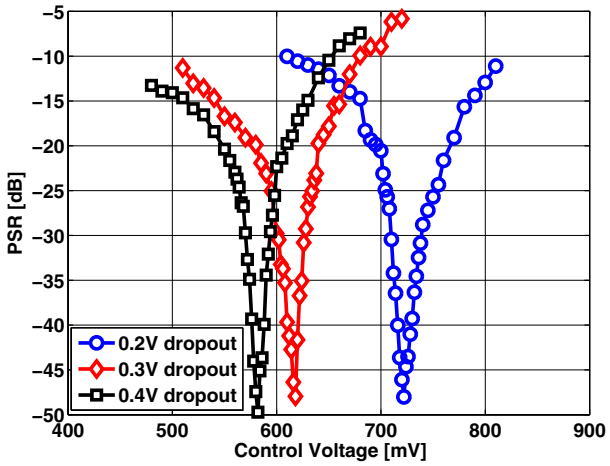

Fig. 8. Measured PSR versus the control voltage for different dropout voltages.

mixer offset indicate that the calibration loop always converges to the optimal cancellation gain. The measured PSR curves at different output load currents, obtained by manually setting the control voltage, are depicted in Fig. 9. The proposed

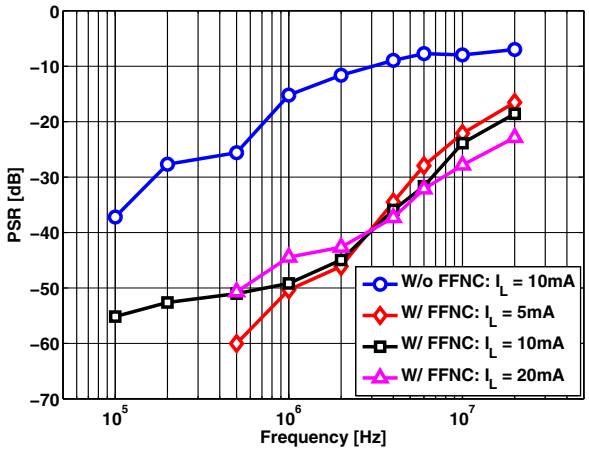

Fig. 9. Measured PSR with and without the proposed noise cancellation.

FFNC technique improves the PSR of a conventional LDO over a wide range of load currents. The improvement is more than 35dB and 15dB at 1MHz and 10MHz supply noise frequencies, respectively.

The current consumption in feed-forward and the feedback amplifiers are 200μA and 100μA, respectively. At 1.8V supply and a dropout voltage of 300mV, the LDO has a power efficiency of about 81%, compared to 83% when the feed-forward path is turned off. Thus, the proposed FFNC provides an attractive means to improve the PSR of an LDO with minimal degradation in power efficiency.

Performance summary of the prototype along with comparison to state-of-the-art high-PSR LDO is shown in Table. I. Compared to [2], the prototype achieves similar PSR at 5 times higher load current and 50% lower dropout voltage. Even though the FFNC LDO uses 65pF additional capacitance, [2] requires charge-pumps that consume significant area. Both [3], [4] use several orders of magnitude larger capacitance and hence are not suitable for fully-integrated applications.

IV. Summary

A feed-forward noise cancellation technique to improve the PSR of an LDO is presented. The proposed FFNC operates in conjunction with a conventional LDO and extends the noise rejection bandwidth by nearly an order of magnitude. Because FFNC does not rely on noise filtering, it obviates the need for large capacitors that are required in conventional high-PSR LDOs. Fabricated in a 0.18μm CMOS the prototype achieves a PSR of -50dB and -25dB at 1MHz and 10MHz supply noise frequencies, respectively, at 10mA load current. Compared to a conventional LDO, this represents an improvement of at least 30dB at 1MHz and 15dB at 10MHz. The prototype uses only 25pF load capacitance and occupies an active area of 0.04mm^2. Measurement results illustrating the sensitivity of PSR to load current and dropout voltage are presented. A background correlation-based gain calibration technique to determine the cancellation gain that guarantees high-PSR under all operating conditions is discussed.

TABLE I

Performance Summary and Comparison to State-of-the-Art

	[2]	[3]	[4]	This Work
Technology	0.6μm	0.35μm	0.13μm	0.18μm
Area [mm^2]	N/A	0.053	0.049	0.041
V_{DD} [V]	1.8	1.05	1.15	1.8
V_{OUT} [V]	1.2	0.09	1	1.5
Dropout [V]	0.6	0.15	0.15	0.3
Load [mA]	5	50	25	25
$I_{Quiescent}[\mu A]$	70	160	50	300
PSR@1MHz/10MHz	-40dB/ -27dB	-50dB/ N/A	-67dB/ -50dB	-40dB/ -22dB
Total cap	60pF	1μF	4μF	125pF

V. Acknowledgements

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