A 5.6 μA Wide Bandwidth, High Power Supply Rejection Linear Low-Dropout Regulator With 68 dB of PSR Up To 2 MHz

Kishan Joshi, *Student Member, IEEE*, Sanjeev Manandhar, *Member, IEEE*, and Bertan Bakkaloglu, *Fellow, IEEE*

***Abstract*— High power supply rejection (PSR) with a wide rejection frequency band is becoming a critical requirement in linear low-dropout regulators (LDOs) used in complex systems-on-chip (SOCs). Typical LDOs achieve higher PSR within their loop-bandwidth; however, their supply rejection performance degrades with reduced loop-gain outside their loop-bandwidth. Typical LDOs with external filtering capacitors may also have spectral peaking in their PSR response, causing excess system-level supply noise. This work presents an LDO design approach, which achieves a PSR of higher than 68 dB up to 2 MHz frequency and over a wide range of loads up to 250 mA. The wide PSR bandwidth is achieved using a current-mode feedforward ripple canceller (CFFRC) amplifier which provides up to 25 dB of PSR improvement. The feedforward path gain is inherently matched to the forward gain of the LDO, not requiring calibration. The LDO has a fast load transient response with a recovery time of 6.1 μs and has a quiescent current of 5.6 μA. For a full load transition, the LDO achieves settling with overshoot and undershoot voltages below 27.6 and 36.36 mV, respectively. The LDO is designed and fabricated in a 180 nm bipolar/CMOS/DMOS (BCD) technology. The CFFRC amplifier helps to achieve low quiescent power due to its inherent current mode nature, eliminating the need for supply ripple summing amplifiers and adaptive biasing.**

***Index Terms*— Current-mode feedforward ripple canceller (CCFRC), high power supply rejection (PSR), low quiescent current, low-dropout regulator (LDO), wideband PSR.**

I. Introduction

SYSTEMS-ON-CHIP (SOC) designs can integrate both high switching noise digital cores, as well as high dynamic range analog, mixed signal and RF blocks. Switching regulators, which provide efficient regulated power supply for SOCs require large passive components to suppress ripple at their output. High-performance RF and analog modules in SOCs such as ADCs, phase-locked loops (PLLs) [1], class D amplifiers [2] and RF circuits [3] are highly susceptible to supply ripple and require low ripple power supplies. In typical applications, a low-dropout regulator (LDO) is used in series with a switching regulator to filter out switching noise [4], thereby eliminating the need for large inductor-based filters [5].

Typical LDOs have their best power supply rejection (PSR) at lower frequencies and light load currents owing to higher low-frequency (DC) loop gain of the LDO regulation loop. But at higher frequencies and heavy load currents, the PSR starts degrading due to the limited loop bandwidth of an LDO [6]. In view of the increasing operating speeds, it is critical to achieve high PSR over a wide frequency bandwidth. Since LDOs are also used in Internet-of-Things (IoT) sensor systems, they need to have a low no-load quiescent power consumption in order to extend battery life.

Prior works on increasing the PSR bandwidth include feedback and feedforward techniques or adding series elements to shield the output from supply noise. While adding series cascode MOSFET is shown to improve the PSR [7], [8], it does so at the cost of increased dropout voltage, and degrading the maximum achievable efficiency of the LDO. In [9], a high-frequency sampling loop to increase the impedance from supply to output is proposed. While this does improve the PSR, it comes at the cost of additional complexity in design and increased losses due to quiescent power.

Feedforward ripple cancellation (FFRC) techniques have several advantages over the techniques presented above. Being an auxiliary feedforward path, FFRC does not impact the dropout performance of the LDO. A fixed gain, voltage mode FFRC is presented in [10]. The improvement in PSR is gained only for a limited load current of 25 mA and comes at the expense of quiescent power. For larger load currents, the increased pass transistor size would require a wider bandwidth for summing amplifier and lead to an increase in quiescent power and area. Quantizer based adjusted gain FFRC technique is presented in [11]. While this approach uses adjusted feedforward gain, the circuit complexity involved in having the second stage amplifier, filter and associated overhead on power and area makes this undesirable. In [12], a voltage mode FFRC is presented with adjustable gain to account for loop gain variations. The drawback of this technique is that, it requires a pre-regulated supply to power all blocks except the FFRC and the power MOSFET. Adaptive supply ripple-cancellation (ASRC) technique is presented in [13] to help improve the PSR over a wide bandwidth, but the improvement in PSR is less than 15 dB up to 2 MHz and the maximum load current is limited to 25 mA. In addition, the circuitry to tune

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Kishan Joshi and Bertan Bakkaloglu are with the School of Electrical and Computer Engineering, Arizona State University, Tempe, AZ 85287 USA (e-mail: kishan.joshi@asu.edu).

Sanjeev Manandhar is with Texas Instruments Inc., Dallas, TX 75243 USA.

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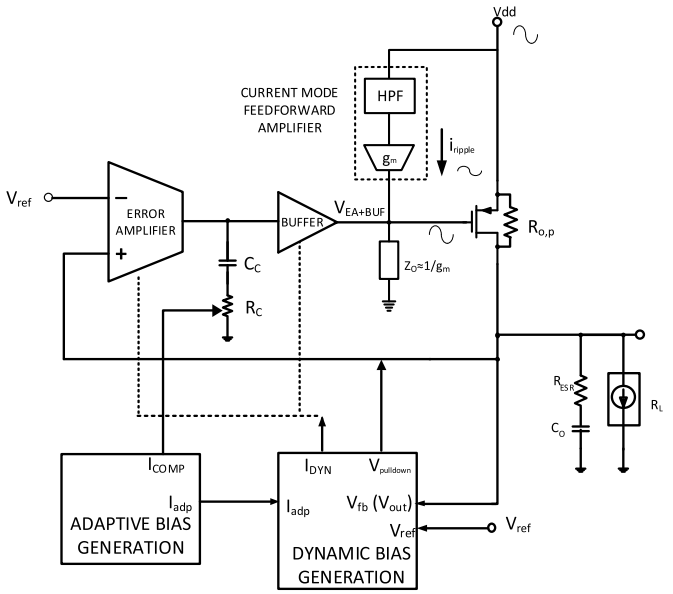

Fig. 1. Top-level LDO block diagram showing current-mode feedforward amplifier and adaptive/dynamic bias generators.

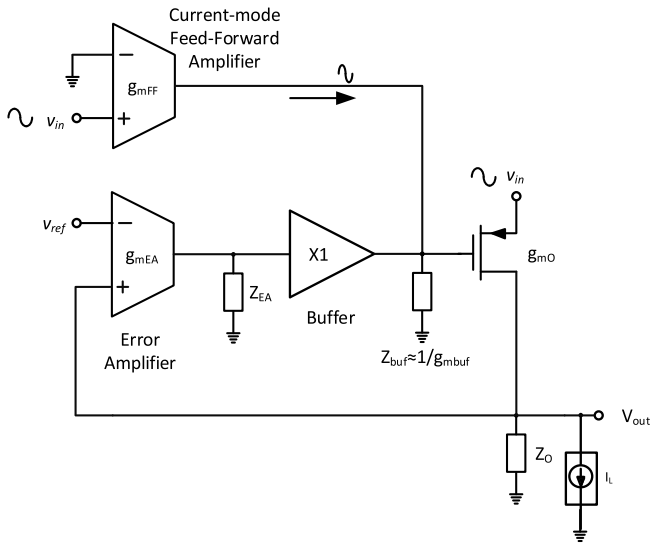

Fig. 2. CFFRC-based PSR improvement technique.

the gain increases the quiescent current to ∼300 μA and is not conducive for low power solutions.

This work utilizes a current-mode feedforward ripple canceller (CFFRC) amplifier to improve the PSR of a PMOS LDO by up to 25 dB over a wide bandwidth (greater than 68 dB upto 2 MHz) and over a wide range of loads (from 100 μA to 250 mA). While NMOS LDOs have faster transient performance due to inherent feedback of common drain configuration and support lower dropout voltages, they need additional charge pump in order to generate the required gate drive voltages [6], [14]–[16]. In the proposed approach, a PMOS LDO which does not require any special gate drive circuitry or charge pumps is used, thereby lowering the quiescent current as shown in Fig. 1. The LDO consists of a PMOS power FET, a folded cascode error amplifier (EA), the power FET driver buffer, current-mode feedforward (CFFRC) amplifier, adaptive and dynamic bias generation blocks and the compensation network.

The LDO works with an off-chip output capacitor setting the dominant pole with a PMOS power FET. Additionally, the inherent common source configuration of the PMOS LDO helps to improve the loop gain and low-frequency PSR of the LDO.

LDOs can have either NMOS or PMOS regulation FETs. In order to reject the ripple on the input voltage of an NMOS LDO, the gate of the power stage would have to be very low noise in comparison to the drain of the NMOS power FET. For a PMOS LDO, the gate of the PMOS power stage would have to track the ripple on the source of the transistor in order to provide efficient ripple cancellation at the LDO output [6]. Making supply ripple common mode at the regulation FET is the fundamental idea for most FFRC techniques [18]–[20]. In this work, the FFRC is achieved with the CFFRC amplifier and helps to improve the PSR over a wide bandwidth (from 100 Hz to 2 MHz).

With the proposed feedforward technique, the LDO achieves 68 dB PSR up to 2 MHz. The CFFRC improves the PSR over a wide range of loads from 100 μA to 250 mA by 25 dB. The LDO also uses adaptive biasing on the load current and has dynamic biasing to improve the transient response. Transient performance with low undershoot and overshoot voltages of 36.36 and 28.7 mV, respectively, is achieved. The recovery times for undershoot and overshoot are 9.9 and 6.1 μs, respectively. The low overshoot recovery time is achieved with the help of a pull-down circuit. The wideband PSR of the LDO is achieved without the need for complex circuitry and adaptive or dynamic biasing [17], ensuring the no-load quiescent current of 5.26 μA, without impacting the transient performance. The LDO is fabricated using 500 nm transistors in a 180 nm bipolar/CMOS/DMOS (BCD) process to support up to 5 V input supply.

The rest of this article is organized as follows. Section II presents the PSR analysis of a typical LDO and the proposed approach of the CFFRC-amplifier-based PSR improvement. Section III discusses the implementation of the LDO and transient improvement techniques. Experimental results are presented in Section IV, followed by the conclusion in Section V.

II. PSR Analysis for LDO and the Proposed Current-Mode FFRC Technique

In order to reduce the noise from supply coupled to output, it is imperative to reduce the ratio of impedance from output to ground with respect to the impedance from supply to the output. This can be achieved by using feedback or feedforward techniques. The main disadvantage of feedback techniques is the requirement for a large loop bandwidth to regulate the impedance at higher frequencies. This would lead to larger quiescent power consumption, thereby reducing the current efficiency of the LDO. Hence, feedforward based PSR improvement techniques are better for low power wide-bandwidth PSR LDOs.

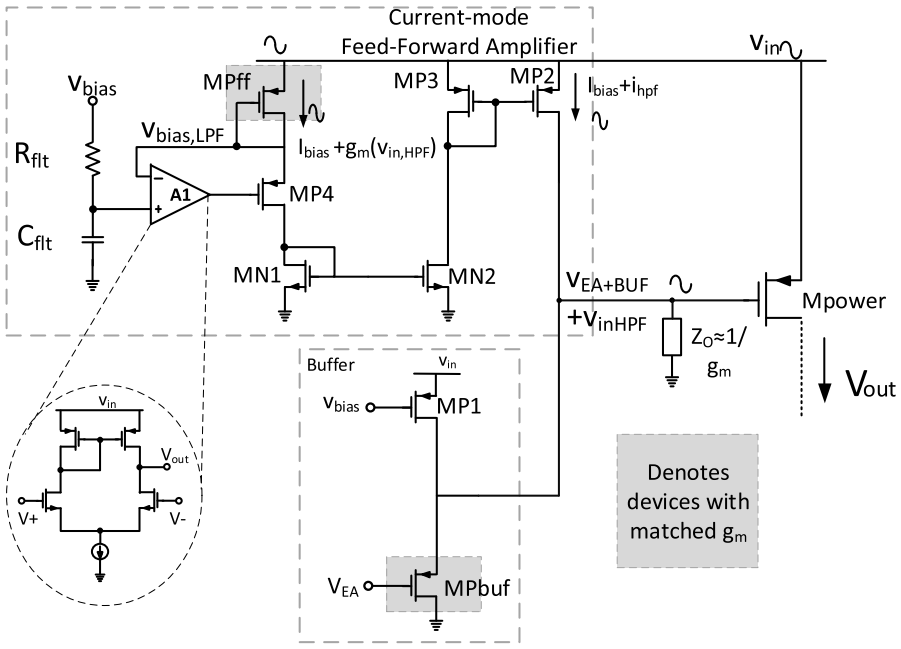

Fig. 3. CFFRC amplifier with source follower buffer.

One major drawback with the voltage-mode feedforward technique is that, the feedforward supply ripple voltage has to be summed with the loop control signal from the EA in voltage domain with high accuracy. Voltage domain summation requires an additional summing amplifier. This type of summation has two implications—first, the summing amplifier consumes additional power which degrades the current efficiency of the LDO. Second, the degree of supply-rejection is directly dependent on the bandwidth of the summing amplifier and the circuits in the series path. Therefore, the summing amplifier has to be wide-bandwidth.

CFFRC amplifier addresses the concerns with this approach. Current mode addition is inherent, not requiring any additional circuit, connecting the two current branches achieves the addition of the current-mode signals representing supply noise [21]. Current mode techniques provide wide bandwidth operation, improving PSR over a wide range of frequencies. The LDO is operated in unity gain feedback loop to get the maximum loop gain, thereby improving the dc PSR of the LDO.

The small-signal model of the LDO with the CFFRC amplifier is shown in Fig. 2. As shown in Fig. 2, LDO output v_{out} comprises two terms—the first one due to the regulation loop and the second due to the feedforward path as follows:

$$v_{\text{out}} = \left(\frac{A_{\text{CL}}}{1+A_{\text{CL}}}\right) v_{\text{ref}} + \left(\frac{A_P\left(1 - g_{m_{\text{ff}}}\left(\frac{1}{g_{m_{\text{buf}}}} || \frac{1}{sC_g}\right)\right)}{1+A_{\text{CL}}}\right) v_{\text{in}} \tag{1}$$

$$A_{\text{CL}} = g_{m_{\text{EA}}} Z_{\text{EA}} g_{m_O} Z_o \tag{2}$$

$$A_P = g_{m_O} Z_O \tag{3}$$

where A_{CL} is the closed-loop gain of the LDO, A_P is the gain of the power stage, v_{in} is the LDO input, v_{ref} is the reference voltage (scaled bandgap reference), Z_{EA} is the output impedance of the EA, g_{m_O} is the transconductance of the power MOSFET, C_g is the effective capacitance at the gate of the power MOSFET. Z_o is the output impedance of the LDO, $g_{m_{\text{EA}}}$ is the transconductance of the EA, $g_{m_{\text{FF}}}$ is the transconductance of the CFFRC amplifier and $1/g_{m_{\text{buf}}}$ is the output impedance of the buffer (ignoring C_{gs}&C_{gd} of the pass transistor since the buffer is designed as low impedance until few MHz which is the frequency range of interest). The objective is to make the second term in (1) zero, thereby helping to improve the PSR of the LDO. This can be achieved if we can design the term $g_{m_{\text{ff}}}/g_{m_{\text{buf}}}$ to be close to unity.

Fig. 3 shows the proposed CFFRC-amplifier-based PSR improvement technique. It is based on the core idea of high pass filtering the supply ripple to get only the AC content and then converting it to an equivalent current using V-to-I.

The filter R_{flt} (=100 MΩ) and C_{flt} (= 10 pF) are designed to set the filter cutoff frequency to 150 Hz so that the gate of MP_{ff} is at AC ground compared to its source. Non-silicide high resistance serpentine poly resistors are used to implement the resistor R_{flt} and C_{flt} is implemented using MIM capacitors. The amplifier A1 is used to set the DC bias current through MP_{FF}. The amplifier needs to be a wide bandwidth and low gain amplifier. Since the gain of the amplifier does not have to be large to set the DC bias, this amplifier can be designed with a relatively low Iq budget using the simple five-transistor operational transconductance amplifier (OTA) structure. The bias current through MP_{FF} and MP_{BUF} is set such that the g_ms of the two match. This is accomplished by ensuring that the same bias V_{bias}which sets the bias for the current source in buffer is used as the input to the amplifier A1 after filtering. This also ensures that after the filter, any remaining ripples on V_{bias} are eliminated. The DC offset of the amplifier does not have a significant impact on the DC bias. The small-signal

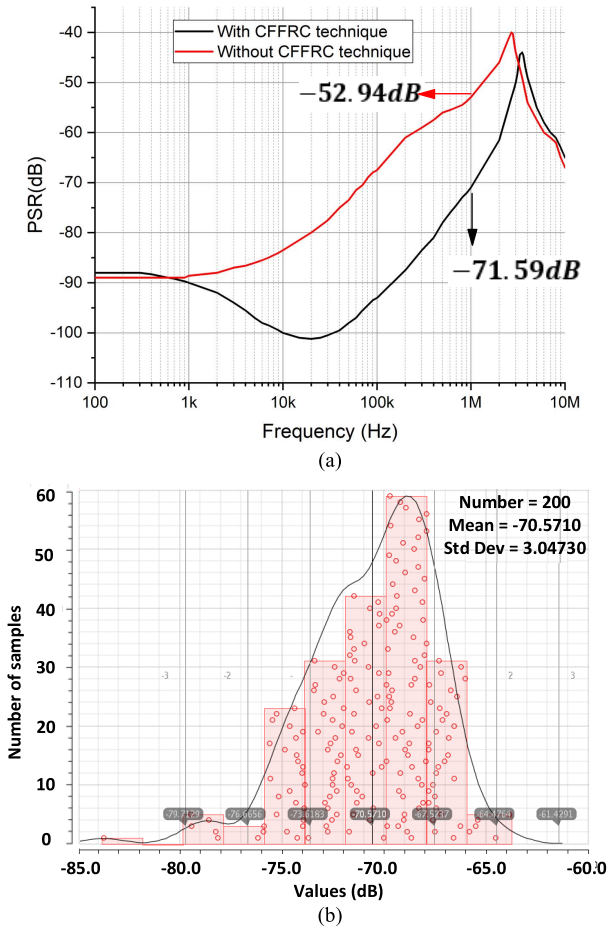

Fig. 4. (a) PSR improvement with CFFRC technique. (b) Monte Carlo simulation showing PSR at 1 MHz with 100 mA load. $V_{\text{in}} = 5$ V, $V_{\text{out}} = 4.5$ V and $C_L = 2.2$ μF.

current flowing through MP_{ff} is given by

$$i_{\text{hpf}} = g_{m_{\text{ff}}} \times V_{gs} = g_{m_{\text{ff}}} \times (V_{\text{in}} - V_{\text{in,lpf}}) \tag{4}$$

$$i_{\text{hpf}} = g_{m_{\text{ff}}} \times V_{\text{in}_{\text{hpf}}} = g_{m_{\text{ff}}} \times V_{\text{in}_{\text{ripple}}} \tag{5}$$

The current generated is summed at the output of the buffer (input of the power stage of the LDO) as shown in Fig. 3.

The impedance seen at the gate of the power stage is given by

$$Z_o = Z_{o_{\text{buffer}}} || C_{\text{gs}_{M\text{power}}} || C_{\text{gd}_{M\text{power}}} \tag{6}$$

$$Z_{o_{\text{buffer}}} \approx \frac{1}{g_{m_{\text{buf}}}} \tag{7}$$

Since the buffer is designed for low output impedance over a wide range of frequencies, the Z_O is dominated by $Z_{O_{\text{buffer}}}$ and the effect of $C_{\text{gs}_{M\text{power}}} \& C_{\text{gd}_{M\text{power}}}$ are not seen till a few MHz of frequency range. In the cases where the pass FET Mpower is large (in case of larger load currents in the order of 500 mA or more), other architectures like super source follower for buffer may be used which will ensure that the Z_O is dominated by $Z_{O_{\text{buffer}}}$.

The equivalent voltage ripple at gate of the power stage due to the additional current from the CFFRC amplifier is given by

$$V_{\text{ripple}} = i_{\text{hpf}} \times Z_o \approx i_{\text{hpf}} \times Z_{o_{\text{buffer}}} \tag{8}$$

From (5), (7), and (8), we obtain

$$V_{\text{ripple}} \approx \frac{g_{m_{\text{ff}}}}{g_{m_{\text{buf}}}} \times V_{\text{in}_{\text{ripple}}} \tag{9}$$

If we can ensure that $(g_{m_{\text{ff}}}/g_{m_{\text{buf}}}) = 1$, then the equivalent voltage ripple on the gate of the PMOS power stage would be

$$V_{\text{ripple}} \approx V_{\text{in}_{\text{ripple}}} \tag{10}$$

Having this ripple as common-mode input to both the gate and source of the PMOS power stage would ensure that minimal supply ripple gets coupled onto the drain which is the output of the LDO, thereby helping to improve the PSR of the LDO.

A PMOS source follower buffer helps to reduce the impedance at the input of the power stage as shown in Fig. 3. The buffer is biased using a combination of static and weak adaptive bias by using the bias current from adaptive bias block. The same bias is also used to bias the CFFRC feedforward MOSFET MP_{ff}.

The advantage of the CFFRC approach is that the main criterion for ensuring common-mode ripple on both the gate and source of the PMOS power stage is

$$\frac{g_{m_{\text{ff}}}}{g_{m_{\text{buf}}}} = 1 \tag{11}$$

Since this requires matching of the g_m of the two MOSFETS (CFFRC MOSFET MP_{ff} and the buffer MOSFET MP_{buf}), it ensures good matching and tracking across process corners. Both the devices are sized and biased similarly. This ensures that the improvement in PSR is steady across process, voltage, and temperature (PVT). At a steady state, with no ripples on the supply, the feedforward path does not have gain and hence, does not affect the main regulation loop.

Fig. 4(a) shows the PSR of the LDO with and without the CFFRC. Across the range of frequencies of interest, the CFFRC technique provides PSR improvement of the order of 18–25 dB. Fig. 4(b) shows the variation in PSR across PVT with Monte-Carlo simulations. As we can observe, the PSR variation is minimal due to the robust matching of g_m.

III. LDO Implementation and Transient Improvement Techniques

A. Folded Cascode EA and Buffer

A folded cascode OTA based EA is designed as shown in Fig. 5 to achieve high loop gain and high DC PSR. The folded cascode OTA takes in no-load bias current of 1.5 μA and gives 70 dB of gain with a bandwidth of 8.2 MHz.

The EA is biased with a combination of static bias current (for no-load operation) and adaptive and dynamic biasing (for transient and higher load currents).

Fig. 6 shows the loop response of the LDO with across process and temperature for an input voltage $V_{\text{in}} = 5$ V and $V_{\text{out}} = 4$ V. As seen from Fig. 6, the minimum phase margin across PVT is 33°.

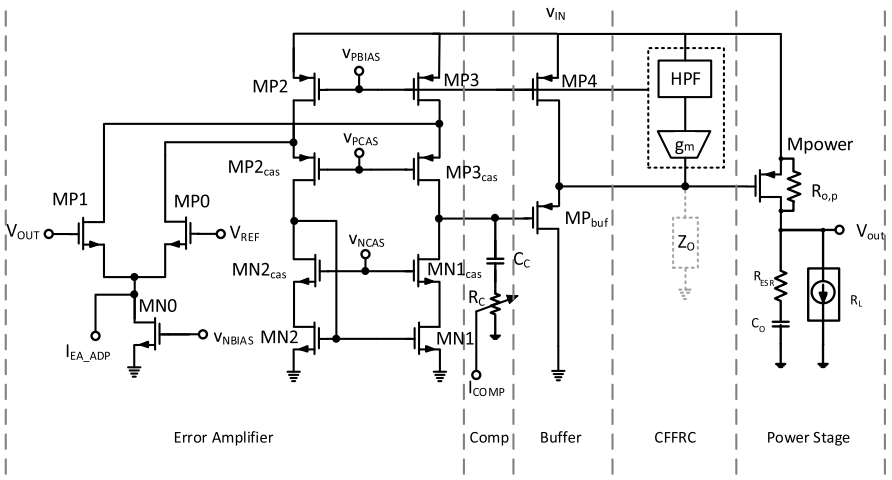

Fig. 5. Schematic of the proposed LDO.

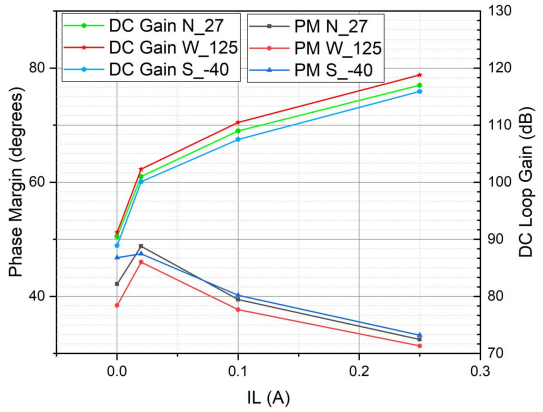

Fig. 6. Simulated dc loop gain and phase margin variation across corners.

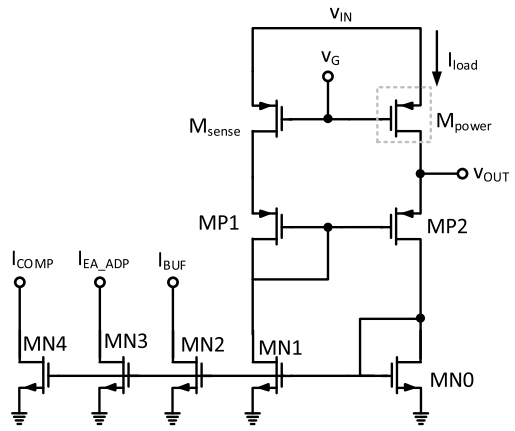

Fig. 7. Schematic of adaptive biasing block.

B. Adaptive and Dynamic Bias Generation

Fig. 7 shows the implementation of the adaptive biasing scheme. It uses a ratio of 1:M senseFET-based architecture to determine the load current flowing through the PMOS power stage [11], [17]. The sense ratio is kept at 1:12000. Any mismatch in the matching between the senseFET and the power FET only results in small variations in the scaled-down current.

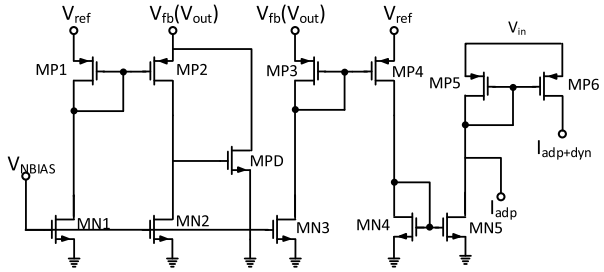

Fig. 8. Schematic of dynamic biasing block with current from adaptive biasing block.

The adaptive biasing block changes the bandwidth of different blocks adaptively based on the load current, thereby ensuring good transient response. The buffer and CFFRC amplifier have weak adaptive biasing in order to track changes of $R_{\mathrm{ds}_{M\mathrm{power}}}$ of the power MOSFET with load current and modulate the feedforward gain.

In addition to adaptive biasing, a dynamic biasing block is designed in order to provide bursts of current which helps to reduce the undershoot/overshoot voltage during load/line transients and helps to reduce the recovery time by temporarily increasing the bandwidth of the LDO loop [17]. Fig. 8 shows the dynamic biasing block designed in this LDO.

It makes use of a common-gate architecture (MP1–MP2 and MP3–MP4) and tracks V_{out} of the LDO as compared to V_{ref}. At steady state, $V_{\mathrm{out}} \approx V_{\mathrm{ref}}$. Following a load/line transient and V_{out} overshoots/undershoots, this common gate amplifier provides bursts of current which are used to modulate the bias of EA and buffer. The bias current flowing is of the order of 50 nA and hence, V_{ref} does not need an amplifier.

Since an LDO acts as a current source, typical LDO load current response from high to low current transients shows a linear discharge of the output voltage from the overshoot voltage which is dictated by the load. In order to address this, a pulldown MOSFET (MPD) which pulls down the output

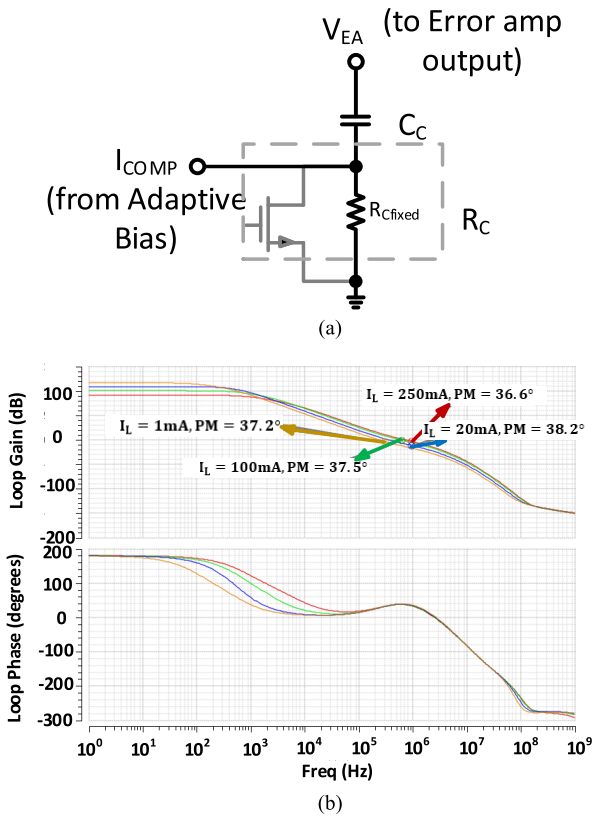

Fig. 9. (a) Pole–zero tracking frequency compensation scheme with parallel fixed resistance. (b) LDO loop response for different load currents.

whenever there is an overshoot is added to reduce the recovery time and overshoot voltage.

C. Compensation

In addition to the dominant output pole, there are two additional poles in the loop—first at the output of the EA and second at the output of the buffer. The buffer output pole is pushed beyond the unity-gain bandwidth of the LDO loop since the buffer output impedance is small. The buffer having weak adaptive biasing also helps with this since the output pole of the buffer tracks the load current of the LDO and moves accordingly. Effectively, this makes the LDO loop a two-pole system. Hence, in order for the loop to be stable compensation is required.

A pole-zero tracking compensation scheme is used to introduce a zero in the loop which compensates for the second pole of the EA as shown in Fig. 9(a) [22]. The pole generated from this R–C network is at high enough frequencies to impact the loop stability.

The resistor and capacitor used are $R_{C_{\text{fixed}}} = 563$ kΩ and $C_C = 3.5$ pF where $R_{C_{\text{fixed}}}$ is the fixed resistance used along with pole–zero tracking scheme. The transistor shown in gray in Fig. 9(a) is MN4 from Fig. 9 and it helps in modulating the effective resistance in parallel with $R_{C_{\text{fixed}}}$ to generate a zero. This is reflected in the connection I_{COMP} to the adaptive biasing block.

An advantage that comes with the adaptive biasing scheme is the presence of the load current information which can be directly used to modulate the zero location based on the load current. This ensures that the LDO is unconditionally stable across a wide range of load currents.

The addition of the feedforward loop does not affect the stability of the loop since the feedforward loop only feeds the ripple onto the gate of the power stage. Fig. 9(b) shows the variation of phase margin load currents, proving the stability of the LDO. Even though the phase drops in intermediate frequencies, the minimum it reaches to across corners and Monte Carlo simulations is ∼15° due to the zero tracking the load variations.

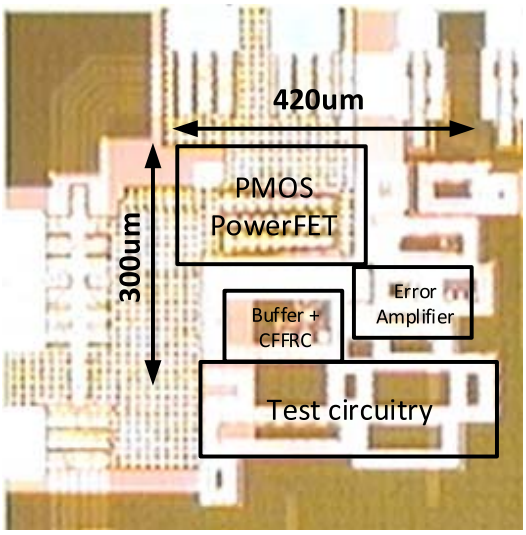

Fig. 10. Die micrograph of the designed LDO.

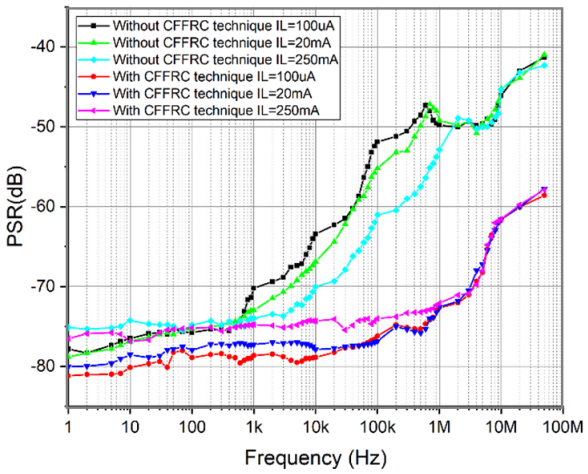

Fig. 11. Measured PSR of the LDO with and without the CFFRC technique for different load currents. $V_{\text{in}} = 5$ V, $V_{\text{out}} = 4.5$ V, and $C_L = 2.2$ μF.

IV. Experimental Results

The LDO is designed and fabricated on the 180 nm BCD process, with 500 nm devices to support 5 V input. Fig. 10 shows the die micrograph for the designed LDO. The active area for the chip is 0.12 mm^2. The CFFRC amplifier occupies only a 0.04 mm^2 die area. The nominal input and output voltage for the LDO are 5 and 4 V, respectively, and the maximum load is 250 mA. The typical output capacitance

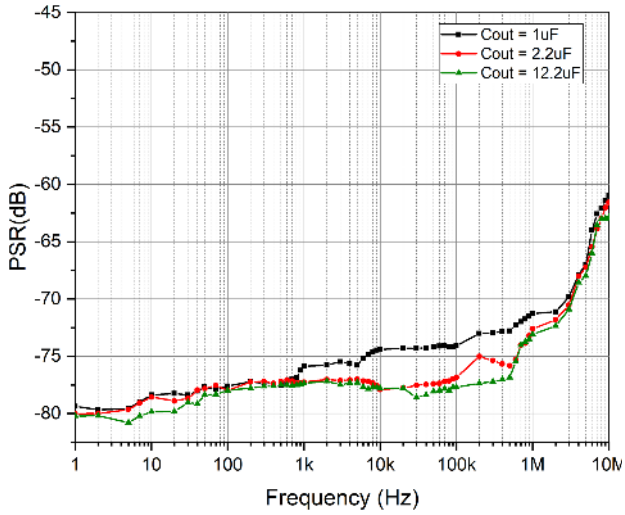

Fig. 12. Measured PSR improvement with varying output capacitors. Minimum PSR up to 2 MHz is 68 dB. $V_{\text{in}} = 5$ V, $V_{\text{out}} = 4.5$ V and $I_L = 20$ mA.

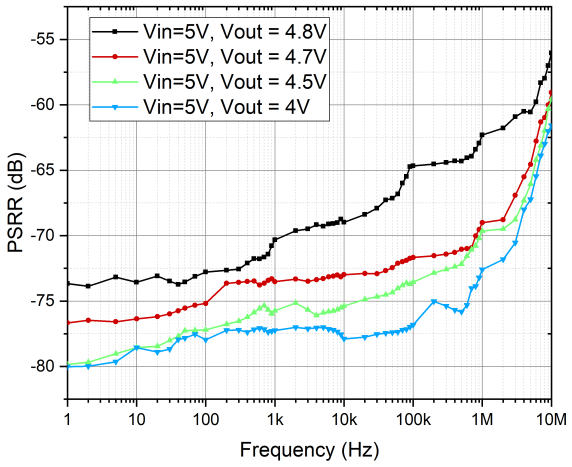

Fig. 13. Measured PSR across different dropout voltage VDO. $V_{\text{in}} = 5$ V, $C_L = 2.2$ μF and $I_L = 20$ mA.

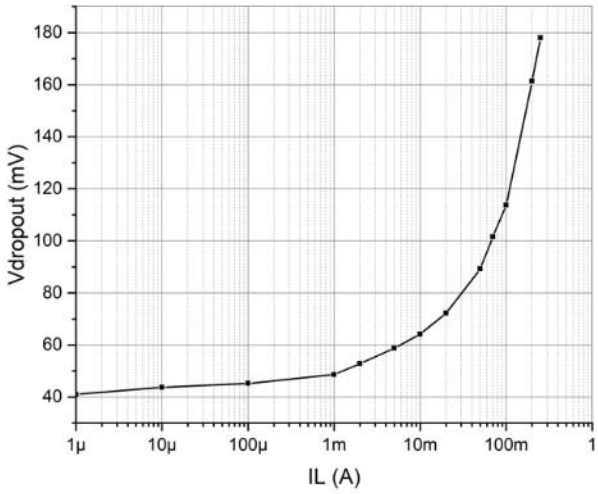

Fig. 14. Variation in dropout voltage with load current for $V_{\text{in}} = 5$ V.

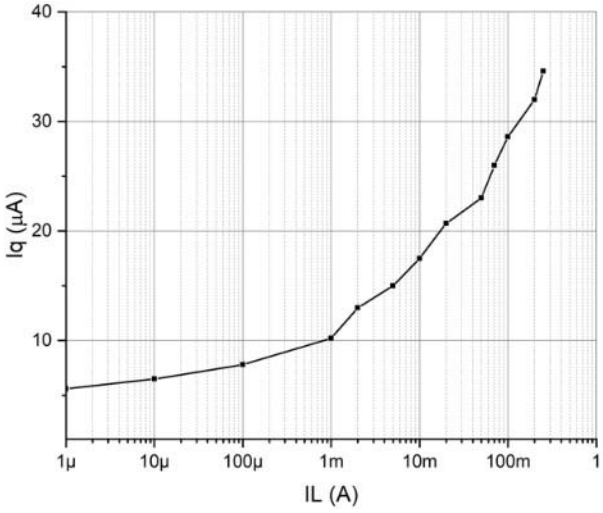

Fig. 15. Measured quiescent current (I_Q) variation across load current.

value used is 2.2 μF and the LDO is not dependent on the ESR for stability. The LDO has a no-load quiescent current consumption of 5.6 μA. The LDO works in unity gain configuration to take advantage of the maximum loop gain. A scaled reference is used to generate the required output voltage. Kelvin connection is adopted to ensure that drops due to parasitic inductance and resistance have minimum effect on the performance of the LDO [24].

The PSR measurement was performed by injecting noise onto the input supply using Picotest Line Injector J2120A. Fig. 11 shows the PSR of the LDO with and without the CFFRC PSR improvement technique for different range of load currents from 100 μA to 250 mA for $V_{\text{in}} = 5$ V and $V_{\text{out}} = 4.5$ V. The CFFRC high pass *RC* filter cutoff frequency is set to 100 Hz and the PSR improvement can be seen from 100 Hz to 5 MHz. The maximum impact of the CFFRC PSR improvement technique is seen in the range of 100 kHz to 1 MHz where the inherent PSR of LDO (without CFFRC technique) degrades due to rolling off of loop gain. The PSR improvement is of the order of 18–25 dB in this range of frequencies. The PSR is measured with a nominal output capacitor of 2.2 μF. As observed, under all loading conditions, the measured PSR is greater than 68 dB up to 2 MHz. Due to the CFFRC technique, the PSR bump that is normally observed in the LDO is not observed. The high-frequency degradation of the PSR is owing to the ESL of the capacitor which increases the impedance from output to ground as compared to the impedance from V_{in} to output around 2 MHz.

The variation of the PSR with the output capacitor is shown in Fig. 12. As expected, with the increase in the output capacitor, the high-frequency PSR improves. The LDO has minimum 68 dB of PSR at 2 MHz even with a small output capacitor of 1 μF.

Fig. 13 shows the efficacy of the CFFRC PSR improvement technique for different dropout voltages V_{DO}, which is defined as the difference between the input and regulated output

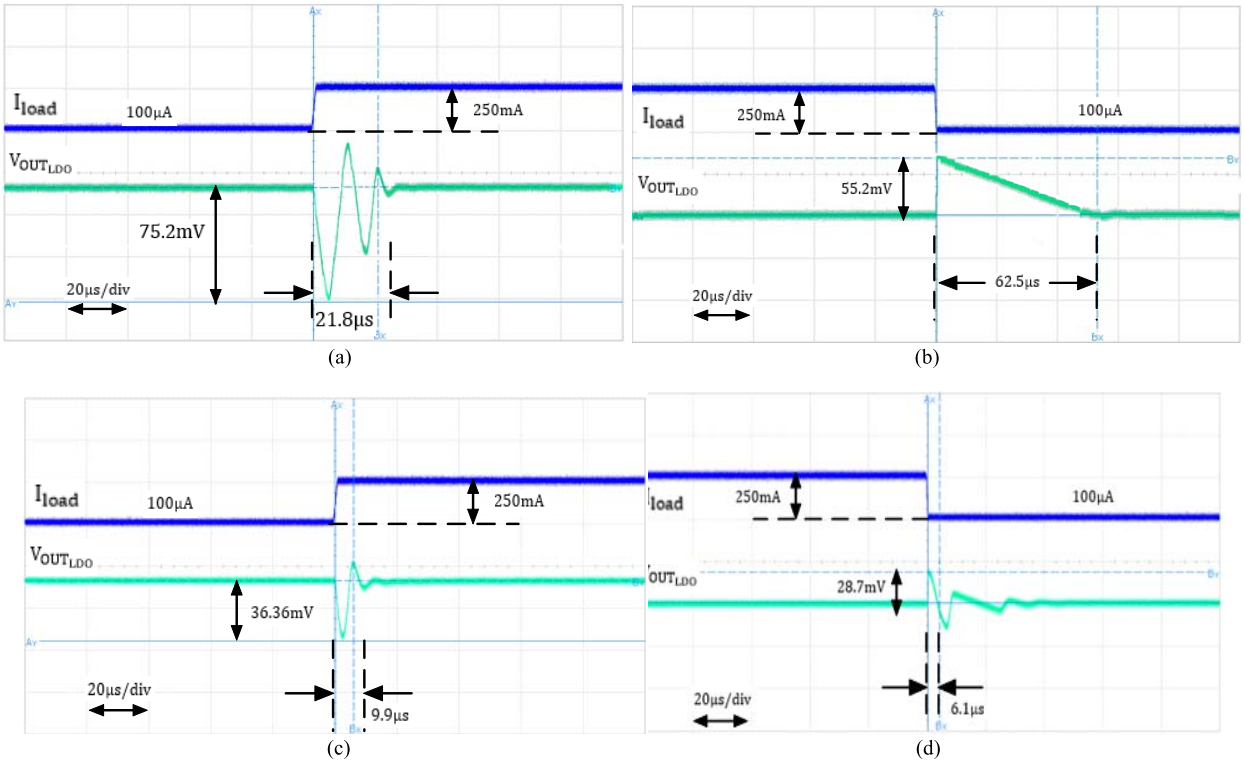

Fig. 16. (a) Load transient plot from 100 μA to 250 mA without adaptive biasing. (b) Load transient plot 250 mA to 100 μA without adaptive bias and pulldown. (c) Load transient plot from 100 μA to 250 mA. (d) Load transient plot 250 mA to 100 μA. All load transient plots are at 1 A/μs slew rate.

voltage (V_{in}–V_{out}). Even with 200 mV of V_{DO}, the PSR improvement is considerable since the CFFRC technique is not impeded by V_{DO}. The worst case PSR, which is observed for $V_{\text{DO}} = 200$ mV, $V_{\text{in}} = 2.5$ V and $I_L = 250$ mA (maximum load current), is 61.5 dB.

Fig. 14 shows the variation with the dropout voltage V_{DO} for various load currents. The dropout voltage is 178.8 mV for the maximum load of 250 mA. The line regulation of the proposed LDO is 10.2 mV/V when the loading current is 250 mA. The line regulation is also assisted by the CFFRC amplifier which helps the loop to respond faster to line transients owing to the feedforward nature.

Fig. 15 shows the variation in quiescent current (Iq) across the range of load currents. The no-load quiescent current is 5.6 μA and the full load quiescent current is $\sim$35 μA for a load current of 250 mA. The load transient response is shown in Fig. 16 for a load transient from 100 μA to 250 mA and vice versa with a load step of 1 A/μs. Settling time is defined as the time taken for the output to reach the targeted accuracy ($\sim$1%). Fig. 16(a) and (b) show the transient response without the pulldown network and adaptive biasing active, while Fig. 16(c) and (d) show the transient response with the adaptive biasing and pulldown turned on. For the low to high load transient, the undershoot voltage and recovery time are 36.36 mV and 9.9 μs, respectively, while for the high to low load transient, the overshoot voltage and recovery time are 28.7 mV and 6.1 μs, respectively. The small overshoot/undershoot voltage is due to the dynamic biasing circuit improving the transient behavior. The overshoot recovery time is less owing to the pulldown circuit which brings the output voltage back to the reference.

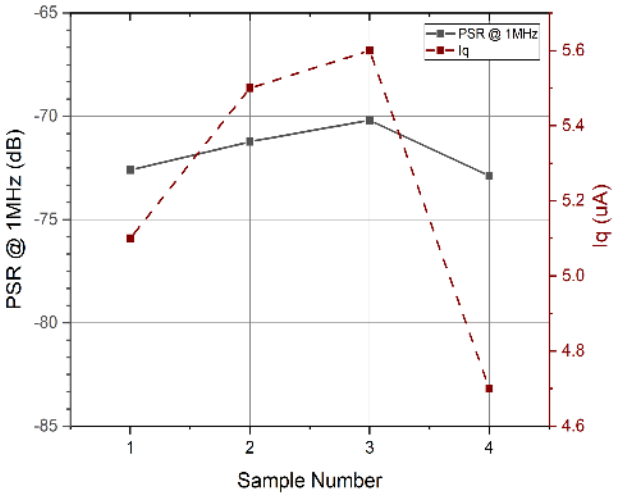

Fig. 17. Measured PSR and no-load quiescent current (I_Q) for four samples. For PSR measurement, $V_{\text{in}} = 5$ V, $V_{\text{out}} = 4.5$ V, $C_L = 2.2$ μF and $I_L = 250$ mA.

The efficacy of the CFFRC PSR improvement technique across different samples is shown in Fig. 17. Plot of the measured PSR at 1 MHz and the quiescent current across four samples is presented. The designed LDO has an integrated noise of 24.6 μV_{RMS} for the integration bandwidth 10 Hz–100 kHz. Most of the contribution to this comes from the noisy voltage

TABLE I
COMPARISON OF THE PROPOSED LDO WITH REPORTED LDOS

Parameter	**This Work**	[9]	[10]	[12]	[13]	[19]
Technology	**180nm BCD (500nm devices)**	1.5µm bipolar	130nm	65nm	65nm	65nm
Power Transistor	**PMOS**		PMOS	NMOS	PMOS	PMOS
I_Q (Quiescent current)	**5.6µA (no load) / 35.6µA (full load)**	18.5µA	50µA	40µA	8µA (no load) / 297.5µA (full load)	150µA
I_{LOAD}	**250mA**	5mA	25mA	100mA	25mA	25mA
C_{LOAD}	**2.2µF**	68nF	4µF	4.7µF	Capless	4.7µF
Output voltage	**1.5V-5.25V**	1.4	1V	1V	1V	1.0V
Overshoot /Undershoot	**28.7mV/36.36mV**	170mV/50mV	15mV/10mV	2mV/4mV	46mV	12mV/12mV
Dropout	**178mV**	200mV	150mV	80mV	200mV	150mV
Transient Load Regulation	**0.112 mV/mA**	0.92 mV/mA	0.048 mV/mA	0.010 mV/mA	0.042 mV/mA	0.04 mV/mA
PSR	**I_{LOAD}=250mA 80dB @ 10kHz, 70dB @ 1MHz, 66dB @ 5MHz**	I_{LOAD}=5mA 57dB @ 100kHz, 49dB @ 5MHz	I_{LOAD}=25mA > 62dB @1kHz-100kHz, 67dB @ 1MHz	I_{LOAD}=100mA 89dB @ 100kHz, 70dB @ 1MHz, worst case 66dB @ 800kHz	I_{LOAD}=25mA > 52dB @ 1MHz	I_{LOAD}=25mA > 61dB upto 1MHz, 47dB @ 10MHz
Area	**0.12mm²**	1.2mm²	0.049mm²	0.048mm²	0.08mm²	0.14mm²
FOM (upto 1MHz) [9] ($PSR_{min}I_{LOAD}/V_{DO}C_L$)	**1.996E9**	103.6E6	93.2E6	840E6	-	39.787E6

reference which is external in this case. By using a spectrally clean voltage reference, the integrated noise floor will come down further [23].

Table I shows the comparison of this work with prior LDOs. Proposed LDO achieves higher PSR without overhead on the quiescent power consumption. The LDO also requires a lesser output capacitor than most of the prior work approaches. The FOM defined provides a clear idea on the comparison of this LDO with the previous works. As observed, this LDO has FOM at least twice better than prior work. The capless LDOs do not have FOM defined. Another aspect to highlight for the proposed work is, even though it is designed and fabricated in 180 nm technology, owing to supporting higher voltage ranges, 500 nm (5 V) devices are used. According to the authors' knowledge, this is the only part that provides such high PSR while supporting higher voltages.

V. CONCLUSION

In this work, a wide bandwidth high PSR LDO fabricated in a 180 nm BCD technology is presented. The LDO features the CFFRC PSR improvement technique. With the CFFRC technique, 18–25 dB of PSR improvement is observed in the 100 Hz–5 MHz bandwidth for a wide range of load currents up to 250 mA, without the need for gain calibration. The LDO also features low no-load quiescent current of 5.6 μA and fast transient recovery of $<$10 μs. The LDO is stable with up to 1 μF load capacitor with worst case phase margin of 35°. The undershoot and overshoot voltages of 36.36 and 28.7 mV, respectively. The CFFRC technique along with the adaptive biasing helps to improve the PSR of the LDO over a wide bandwidth and for a large range of load currents.

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Kishan Joshi (Student Member, IEEE) received the M.S. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2016, where he is currently pursuing the Ph.D. degree.

He was an Analog Design Intern with Kilby Labs, Texas Instruments, Santa Clara, CA, USA, in 2016, with NXP Semiconductors, Chandler, AZ, in 2017, and with the Linear Power Group, Texas Instruments, Tucson, AZ, in 2018, where he worked on power converters, analog-to-digital converters, and ultra-low Iq low-dropout regulators (LDOs), respectively. From 2012 to 2014, he was a Digital Circuit Designer with Sankalp Semiconductors Pvt. Ltd., Hubli, India, where he worked on standard cell library design for mixed-signal libraries. Since 2019, he has been with Linear Power Group, Texas Instruments, where he is involved in the design of linear low-dropout regulators. His current research interests include low-power analog design, supply ripple rejection, and power management IC design.

Sanjeev Manandhar (Member, IEEE) received the B.S. and the M.S. degrees in electrical engineering from the University of Maine, Orono, ME, USA, in 2004 and 2006, respectively.

He joined Texas Instruments Inc., Tucson, AZ, USA, in 2006, and worked on high-performance low-dropout voltage regulators, supply voltage supervisors, and low-power designs, until 2018. He is currently a Member Group of Technical Staff and a Systems Engineer for the General Purpose Amplifier Productline with Texas Instruments Inc., Dallas, TX, USA. He defines and supports products for automotive, commodity, and space applications.

Bertan Bakkaloglu (Fellow, IEEE) received the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 1995.

He joined the Mixes Signal Wireless Design Group, Texas Instruments Inc., Dallas, TX, USA, working on analog, RF, and mixed-signal front ends for wireless and wireline communication ICs. He worked on system-on-chip designs with integrated battery management and analog baseband functionality as a design leader. In 2004, he joined the Electrical Engineering Department, Arizona State University, Tempe, AZ, USA, as an Associate Professor, where he is currently a Professor. His research interests include RF and Power Amplifiers (PA) supply regulators, high-efficiency dc–dc power converters, linear regulators, low-noise power management circuits, biomedical and instrumentation circuits and systems, high-speed data converters, and built-in-self-test circuits for analog ICs.

Dr. Bakkaloglu is a member of the National Academy of Inventors. He has been a Technical Program Chair and the General Chair of the IEEE RFIC Conference and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is the Founding Member of the IEEE Solid State Circuits Society Phoenix Chapter and the Microwave Theory and Techniques Society RFIC (TC-23) Subcommittee Chair.