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Double-OTA External Capless Low-power LDO Regulator with Enhanced PSR and Transient Response

Mohammad Ahmadi
IC Design Research Lab,
Electrical Engineering Department,
Shahrood University of Technology,
Shahrood, Iran
mohammad.ahmadi@shahroodut.ac.ir

Emad Ebrahimi
IC Design Research Lab,
Electrical Engineering Department,
Shahrood University of Technology,
Shahrood, Iran
eebrahimi@shahroodut.ac.ir

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***Abstract*—Low drop-out (LDO) regulators play a vital role in power management devices, serving as a critical component. This research paper introduces an innovative LDO regulator that offers enhanced load transient response and power supply rejection (PSR). In the proposed LDO, by using two OTAs as error amplifiers in a complementary scheme and transferring effectively the over/undershoot of the output voltage to their Tail transistors, the bias current of each OTA is modulated dynamically to improve the slew rate and load transient response. Besides, creating a zero by a low pass filter in the voltage supply terminal of the first error amplifier is caused to reduce the effect of the pole which is located in the gate of the pass transistor, which results in the improvement of the output PSR. These zeroes made the proposed LDO stable without any external capacitor with a phase margin of 60 degrees. The proposed design with an input voltage of 1.8 to 2.4 volts has a PSR of -69 dB at a 1 kHz frequency. In addition, the LDO quiescent current is as low as 600 nA, while delivers maximum current of 50 mA to the load.**

Keywords—External capacitor-less LDO, fast transient, low drop-out (LDO) regulator, power supply rejection (PSR).

I. INTRODUCTION

The adoption of portable and wearable biomedical devices powered by batteries has revolutionized medical care, and LDO regulators have emerged as an essential component within this ecosystem. By providing stable voltage regulation, minimizing voltage drop, and optimizing power utilization, LDO regulators have played a pivotal role in making medical care more accessible, convenient, and efficient. Moreover, these circuits need to exhibit a quick response to load transients, ensuring minimal output voltage fluctuations during the transition between sleep and active states or vice versa [1]. Furthermore, these equipment incorporate circuits that are susceptible to noise, including analog-to-digital converters (ADCs), where the consecutive switching of digital circuits and noise can generate voltage ripples in the power supply. Given the sensitivity of the analog circuits, it is crucial for the LDO employed in such equipment to possess a high Power Supply Rejection (PSR) capability.

Typically, the power supply rejection (PSR) of a low dropout regulator (LDO) is characterized across three frequency ranges: 1- The DC PSR covers frequencies in the range of a few Hz. 2- The mid-frequency PSR pertains to frequencies around 10 kHz. 3- The high-frequency PSR applies to frequencies exceeding 10 kHz. This paper centers on enhancing PSR at mid-frequency and high-frequency, which is commonly used in biomedical equipment [2]. According to Fig. 1, various paths exist through which power supply ripples are transmitted to the LDO's output, and each of these paths exerts a distinct influence on the output Power Supply Rejection (PSR). The output PSR in a conventional LDO is influenced by the ripples that propagate through four main paths, i.e. the ripples through the (1) reference voltage, (2) error amplifier, (3) drain-source conductance of the pass transistor and (4) the parasitic capacitance which is located in the pass transistor gate which is caused by the high dimensions of the pass transistor [3]. The most critical path that leads to the significant degradation of PSR in a conventional LDO is the parasitic capacitance situated in the gate of the pass transistor. This parasitic capacitance arises due to the large dimensions of the pass transistor [3]. Therefore it is considered as the primary contributor to the destruction of PSR in the system.

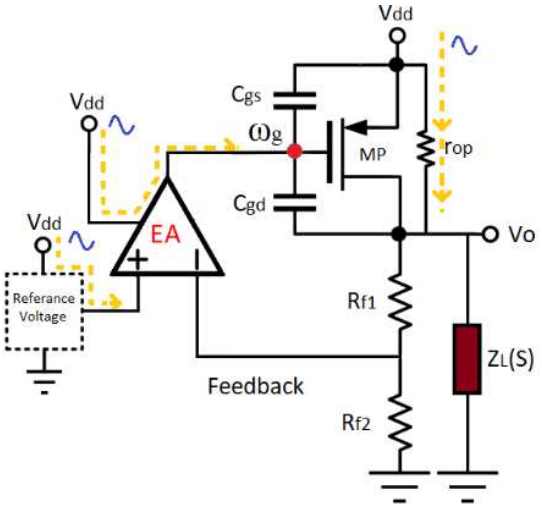

Fig. 1 . Schematic of a conventional LDO.

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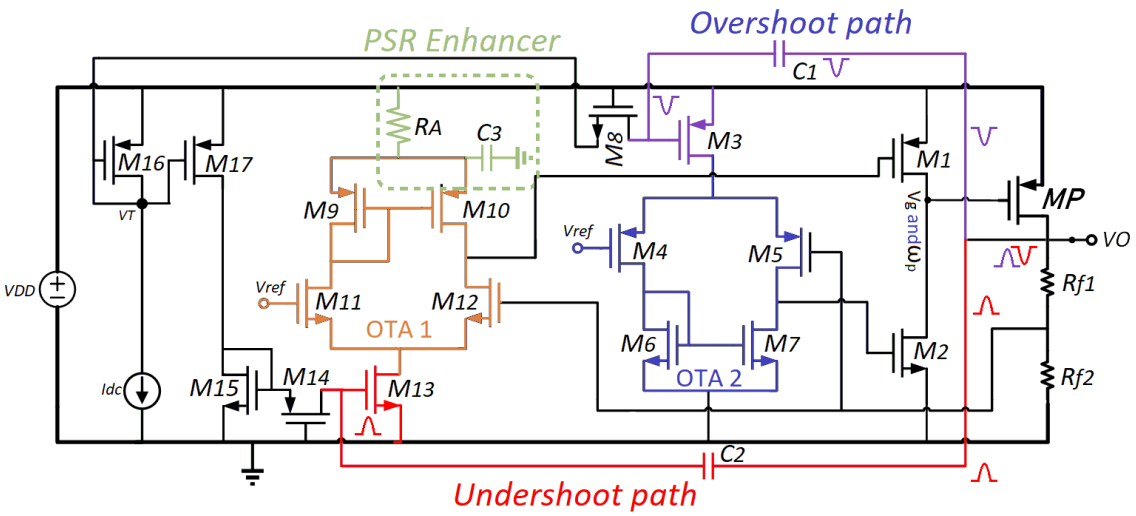

Fig. 2. Proposed LDO with double OTA.

One of the most important parameters that can play a major role in improving of PSR is the LDO's loop gain. Clearly, when the frequency of the pole at the gate of the pass transistor is increased, it leads to a reduction in the loop gain, which results in severe PSR degradation. Also, this pole reduces the feedback loop's speed, which results in a rise in the level of Over/Undershoot voltage when a load current step is present. Several methods have been suggested to minimize the effects of the pole situated at the gate of the pass transistor. One method involves parallelizing the negative capacitor with the pass transistor's gate [4]. However, these techniques often require additional complex auxiliary circuits, resulting in higher power consumption. Another approach suggested in [5] and [6], is the utilization of an NMOS transistor, instead of PMOS, as a pass transistor. However, this approach is not suitable due to the use of a charge pump circuit that results in higher power consumption and output PSR degradation at clock frequency of the charge pump.

Recently, several techniques have been presented to improve load transient response and PSR of the LDO regulators. Most of these techniques draw a lot of current from the supply to move the non-dominant poles to high frequencies, which increases the power consumption of the circuit. On the other hand, some other methods such as [7], [8] use large external capacitors to filter the PSR and improve the load transient response at the output node of LDO. However, the use of off-chip capacitor increase the PCB's area and the material's price.

The rest of the paper is structured as follows. The proposed LDO and its analysis is presented in Section II. summary of the proposed LDO's performance and comparisons with previous works is given in Section III. Finally, Section IV concludes this paper.

II. Proposed LDO and its Analysis

Fig. 2 shows the proposed LDO regulator. The proposed LDO regulator comprised of a PMOS pass transistor (Mp), two OTAs as error amplifiers, a feedback network (R_{f1} and R_{f2}), and a Bandgap reference voltage. The feedback resistors sample the output voltage which is compared with Vref by the OTAs. The OTAs generate the appropriate error signal and apply it to the pass transistor in a negative feedback loop to regulate the output voltage. Apparently the output regulated voltage is determined by the resistive feedback factor (β) and the reference voltage (Vref). The main novelty of the proposed circuit is using two OTAs in a complementary scheme and an R-C network to improve transient response as well as PSR.

According to Fig. 2, two simple OTAs are used as error amplifiers. The output of the first OTA with NMOS input transistors is connected to the gate of transistor M_1, and the output of the second OTA with PMOS input transistors is connected to M_2. Also, in both OTAs, the inverting input is connected to the feedback network and the non-inverting input is connected to the reference voltage. Capacitor C_3 and resistor R_A together form a low-pass filter. As known, to increase the speed of the circuit, the bias current should be maximized and the parasitic capacitance should be minimized. Since the proposed LDO should be used in battery-powered applications that power saving is very important, maximizing bias current is not possible for increasing the life time of battery. Therefore, to save power, the OTAs are biased in subthreshold region and to increase the speed of the loop, the parasitic capacitances are minimized by minimizing the transistors' dimensions. In order to improve the loop speed more a dynamic biasing scheme is also proposed.

A. PSR Enhancement Circuit

One of the parameters that improves the Low-frequency PSR is the loop gain of the LDO. Since the error amplifiers employed in the suggested LDO operate with biasing in the subthreshold region to decrease power consumption and quiescent current, 100 dB loop gain is achieved in low frequencies. Considering that the pole which is located in the gate of the pass transistor causes PSR destruction at high frequencies, a zero is needed to decrease the effect of the pole which is located in the gate of the pass transistor. According to [9] in OTAs with NMOS input transistors, the supply ripples are almost transferred to the output. Therefore, according to Fig. 2, if a low-pass filter is placed on the supply voltage of OTA_1, it can create a zero from the input to the gate of the pass transistor and reduce the pole's effect which is located in the gate of the pass transistor. Note that since the OTA is biased at very low bias current, the voltage drop on

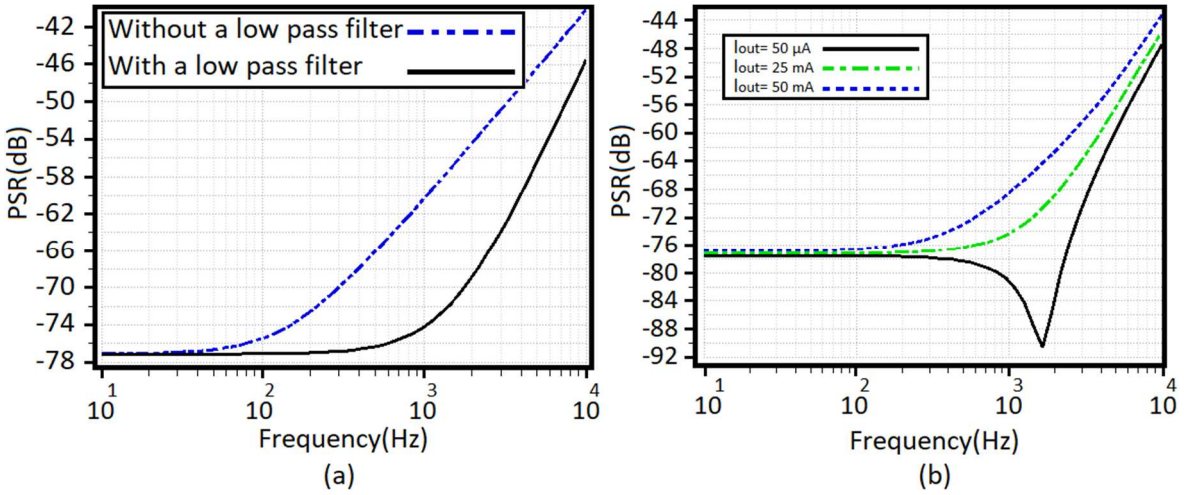

Fig. 3. PSR Simulation of the Proposed Regulator (a) without and with a low pass filter at 25 mA load current and also (b) at load currents of 50mA, 25mA and 50 µA

R_A resistor is negligible. The followings represents the transfer function and zero created by the low-pass filter.

$$\frac{V_g}{V_{dd}} = \frac{R_A C_3 S}{R_A C_3 S+1} g_{m1}(r_{ds1} \| r_{ds2}) \quad (1)$$

In Eq 1, C_3, R_A are the capacitor and the resistor of the low-pass filter respectively. Also g_{m1} and V_g are the transconductance of the transistor M_1 and gate voltage of pass transistor, and r_{ds1} and r_{ds2} are the drain-source resistance of the transistor M_1 and M_2, respectively.

According to (1) the created zero is at origin and the pole is at $-1/R_AC_3S$. Considering that C_3 is in the pf range and R_A resistance is in KΩ range, it can be said that the pole is situated in the high-frequency domain, and has no effect on circuit performance at medium and low frequencies. The high dimensions of the pass transistor increase the parasitic capacitances and creates a low frequency pole in the gate of this transistor, which can deteriorate the output PSR in the Mid frequencies. So the created zero reduces the effect of this pole to a suitable extent and improve Mid frequency PSR. Fig. 3(a) demonstrates the simulation results of output PSR with and without a low-pass filter, which apparently the PSR improvement in Mid frequencies is observed. Fig. 3(b) also depicts the output PSR of the LDO under various load currents of 50µA, 25mA and 50 mA, that accordingly shows the effectiveness of proposed technique at all load currents.

B. Over/Undershoot Voltage Improvement and Stability Analysis.

One of the issues that is important in LDOs is the load transient response. Generally, if the feedback loop's speed in the LDO is not high enough, the sudden changes in the load current will cause an over/undershoot voltage in the LDO output. One of the things that slows down the speed of the loop is the pole which is located in the pass transistor's gate. Because of the substantial dimensions of the pass transistor and Miller effect, this pole is not far enough from the origin and can affect the loop speed. The value of this pole is as follows:

$$\omega_p = -\frac{1}{(C_{gsp} + \underbrace{(1+A_p)C_{gdp}}_{C\ miller})(r_{ds1} \| r_{ds2})} \quad (2)$$

where C_{gsp} and C_{gdp} are the gate-source and gate-drain internal capacitance of the pass transistor (M_p) and the voltage gain of the pass transistor is Ap. According to the Fig. 2 the use of two OTAs in a complementary way increases the feedback loop speed in the presence of output current changes, which in turn reduces the amount of over/undershoot voltage in the circuit. Since over/undershoot voltage is considered as large signals [10], to examine the performance of the suggested LDO under the influence of over/undershoot voltage, large signal models should be used. According to Fig. 2, When the load current undergoes sudden variations, causing an increase in the output voltage (i.e. overshoot occurs), it causes an increase in the gate-source voltage of transistor M_{12} in OTA_1 and then is transferred to the gate of M_1 with a phase difference of 180 degree. Finally, this change reaches to the gate of the pass transistor (Mp) with another 180-degree phase difference. Since in the MOSFET transistor, a phase difference of 180 degrees exists between the gate and drain voltages, the transferred voltage changes to the gate of Mp is inverted in the output and in this way the overshoot is suppressed. Besides, in order to increase the loop's speed as much as possible, the output overshoot voltage is directly transferred to the gate of the tail transistor of OTA_1 through the capacitor C_2. Actually, this provides a dynamic biasing for OTA_1 that instantly increases the tail current in the presence of overshoot, increases the speed of the OTA_1 and a better suppression of overshoot in LDO output is achieved.

In the same way, when the output voltage decreases due to sudden changes in the load current (i.e. undershoot occurs), it causes an increase in the gate-source voltage of transistor M_5 in OTA_2 and then it is transmitted to the gate of transistor M_2 with a 180-degree phase difference. Finally, this change reaches to the the pass transistor's gate (Mp) with another 180-degree phase difference and suppress the undershoot at output node. In order to increase the loop's speed as much as possible, the output undershoot voltage is straightly transferred to the tail transistor's gate of OTA_2 through the capacitor C_1, and this undershoot voltage instantly increases the tail current which results in an increase in the speed of

the OTA_2 and a better suppression of undershoot in LDO output.

Briefly, in the proposed LDO each OTA is biased in subthreshold to decrease the quiescent current. In order to increase the loop speed for fast suppression of over/undershoot dynamic biasing is exploited. Using two OTAs in a complementary scheme guaranty the effective suppression of both overshoot and undershoot simultaneously. Fig. 4 shows the proposed LDO's load transient response, based on which the maximum amount of over/undershoot in the current range of 500µA to 50 mA is equal to 164 mV.

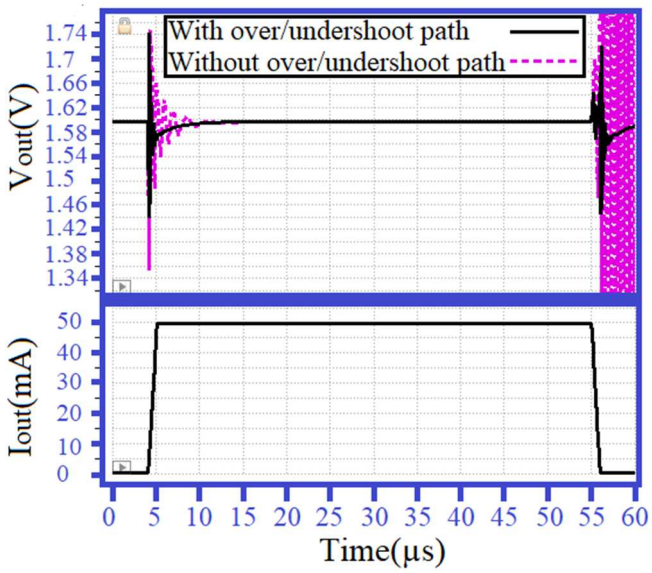

Fig. 4. Proposed LDO's load transient response without over/undershoot path and with over/undershoot path at 1 µs load current edge

Furthermore, using two nested capacitor from the output to the gate of Tail transistor in each OTA, a zero has been created that enables the proposed LDO to be stable without an off-chip capacitor. Fig. 5. illustrates the open-loop frequency response of the proposed design, from which it is determined that the phase margin of the proposed Low Dropout Regulator (LDO) is 47 degrees.

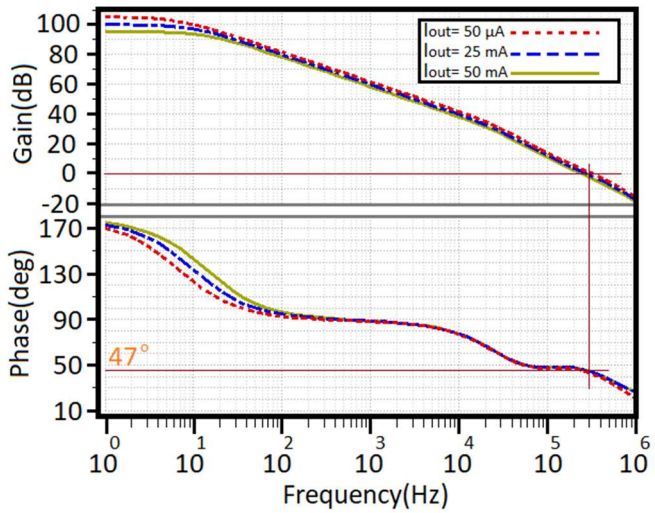

Fig. 5. LDO's open-loop frequency response

III. PVT Analysia and Performance Summary for the Proposed LDO and Prior Works

To examine the effect of process, voltage, and temperature (PVT) on the LDO performance, The PVT simulation results on the proposed LDO on TT, SS and FF corners in the temperature range of -20 to 85 degrees are presented in Table I, based on which the phase margin and PSR of the circuit in the worst case are equal to 42 degrees and -60 dB, respectively. Also, the amount of over/undershoot and line regulation and load regulation of the circuit in the worst case is only 162 mV, 488 µV/V and 1.58 µV/mA respectively. In addition Fig. 6 illustrates the outcomes of Monte Carlo simulations concerning power supply rejection (PSR) at a 1 kHz frequency and phase margin under a load current of 50 µA. A comparative analysis of the performance between the suggested low-dropout regulator (LDO) and previous research is presented in Table II. To ensure a fair evaluation, a widely recognized figure of merit (FOM) [11], expressed as (3), is employed for the comparison.

$$FOM = K\left(\frac{\Delta V_{out} I_Q}{\Delta I_L}\right) \qquad (3)$$

$$K = \frac{\Delta t \ used \text{ in } the \ measurment}{The \ smallest \ \Delta t \ among \ designs \ for \ comparison}$$

Table. I. Process, Voltage, and Temperature simulation results of the proposed LDO

Corners	Temp (°C)	Over/Undershoot Voltage (mV)	Load Regulation (µV/mA)	Load Current	Line Regulation (µV/V)	Phase margin (degree)	PSR(dB) @1kHz
TT	-20	118	0.8	50µA	15	42	-80
				50mA	21	46.3	-73
	+85	166	2.4	50µA	140	44	-74
				50mA	130	52	-64
FF	-20	148	1.48	50µA	90	48	-77
				50mA	79	49	-70
	+85	114	7	50µA	488	57	-60
				50mA	445	64	-66
SS	-20	119	0.72	50µA	11	42	-80
				50mA	9	46	-76
	+85	139	1.58	50µA	50	43	-72
				50mA	49	50	-60

Tabel II. Summary of the performance of the proposed LDO in comparison to previous works.

Parameters	This work	[12]	[13]	[14]	[15]
Year	2023	2022	2021	2023	2020
Technology (nm)	180	90	90	28	130
Off chip capacitor	No	No	No	Yes	No
$I_{Load(max)}$ (mA)	50	100	40	10	100
$I_{Load(min)}$ (µA)	50	40	30	0	100
V_{out} (V)	1.6	0.75	0.75	0.4V	0.4-1.1
$V_{Drop-out}$ (mV)	200	150	150	200	100
I_Q (µA)	0.6	1.74	1.83	31.4	21
$C_{On\ chip(pf)}$	4	1.1	0.49	-	11.28
C_{Load}	0-20pf	0-100pf	0-100pf	1µf	50pf
Line-reg (µV/V)	125.9	400	1000	9700	24800
Load-reg (µV/mA)	4.6	6	36	800	150
PSR (dB)	-69@1kHz -43@10kHz	-50@1kHz -30@10kHz	-43@1 kHz -43@10kHz	NA@1kHz -36@10kHz	-30@1kHz -30@10kHz
Δ I_{LOAD}(mA)	49.5	100	49.97	9.9	100
Δ V_{out} (mV/µs)	162/1	350/1.2	440/0.2	10 /0.1	89/0.3
FOM (µV)	19.6	73.1	32.2	31.7	56

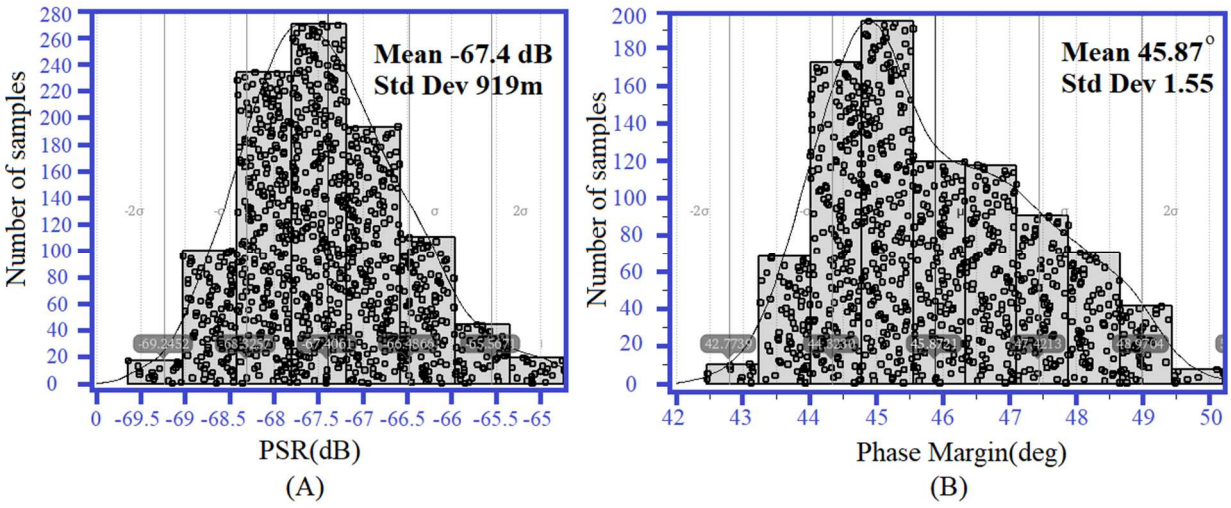

Fig. 6. Monte Carlo simulation outcomes of A, power supply rejection (PSR) at a frequency of 1 kHz, B, phase margin under a load current of 50 µA

IV. Conclusion

Low dropout regulators (LDOs) play a crucial role in analog circuits. These circuits require a reliable output PSR and transient response, as they are sensitive to supply ripples and sudden changes in the voltage of the output. Considering that the proposed LDO design is intended for battery-powered circuits, it incorporates a novel approach to dynamically increase the bias current of the error amplifiers. This design achieves a low quiescent current of as low as 600nA and a maximum output over/undershoot of 162mV in the presence of full load step current, making it suitable for low-power circuits. In addition, by creating a zero from the power supply to the gate of the pass transistor by using a low-pass filter, the proposed LDO has an impressive output PSR of -69 dB and -43 dB at frequencies of 1 kHz and 10 kHz, respectively. Furthermore, using two nested capacitor from the output to the gate of Tail transistor in each OTA, a zero has been created that enables the proposed LDO to reach a phase margin of 47 degrees without requiring any external capacitor. So, while the PSR and transient response of the proposed LDO are enhanced, the LDO is stabilized without any external capacitor.

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