Current-Mode LDO with Active Dropout Optimization

Gerhard Thiele and Erich Bayer
Texas Instruments Deutschland GmbH, 85356 Freising, Germany
Email: g-thiele@ti.com, e-bayer@ti.com

Abstract- **Power supplies for portable end equipment need to be optimized for highest efficiency and low output voltage ripple e.g. for TFT display applications. In general, the output voltage ripple of switched mode power supplies can be further reduced by means of an additional linear regulator (LDO) which is used as post-regulator/filter for the output voltage.**
Since the LDO is not coupled to the DC/DC converter there is either a too high dropout voltage which results in a reduced over-all efficiency or the dropout voltage is not high enough so the ripple rejection of the post regulator is not sufficient since the pass element of the LDO is operated in the linear region.
To overcome this problem, a Current Mode LDO in combination with a load current dependent dropout tracking circuit where the output current information comes from a replica of the pass transistor in the LDO is used. The dropout tracking circuit compares the voltages on the LDO terminals and sends a load current dependent control signal to the DC/DC converter. The goal of this configuration is a high power supply rejection ratio and therefore a low output voltage ripple at optimized efficiency. Depending on the type of the converter (hysteretic or linear regulated PWM) the dropout tracking circuit has to be realized as a hysteretic type with a comparator or linear type with an OP-AMP. A current mode LDO means that the PMOS passelement works like a voltage controlled current source.
This concept is possible for all converter topologies like Buck-, Boost-Converters, Charge-Pumps etc. The converter can be regulated in an energy saving PFM mode without sacrificing the ripple performance. Since the current mode LDO limits the load current, the system is inherently short circuit protected.

I. Introduction

Today's portable power applications are putting greater demands upon the power converter design especially to get a high efficiency and low output voltage ripple. The output voltage of a conventional DC/DC converter operating in a switched mode usually has a considerable ripple. This is especially the case for converters with hysteretic control. Since the general trend is towards lower supply voltage, the absolute value of the converter output voltage ripple needs to be reduced to keep the ratio of ripple to output voltage at a constant value.
The ripple rejection characteristic strongly depends on the frequency response characteristic of the closed loop feedback system in a converter. When the high output voltage ripple of a hysteretic inductive or capacitive voltage converter cannot be tolerated for a particular application, e.g. for a TFT-Display Power Supply [1], a linear regulator is inserted [2] between the output of the converter stage and the load to eliminate the ripple. Since the voltage regulator is not aware of the load requirements, the output voltage of the converter is adjusted to a level sufficient for the regulator to eliminate the ripple under all load conditions. As a consequence, the load current pass transistor in the voltage regulator usually operates in an unsaturated condition, resulting in a considerable loss of efficiency.
The present paper describes a combination of a switched-mode DC/DC converter and a linear regulator which drastically reduces the output voltage ripple of the converter by more than one decade at a minimum loss of efficiency. Additional the advantages of a current mode [3] controlled LDO system is shown with comparison to a voltage mode system focused on the converter stability. The power management system described in this paper was realized in the Texas Instruments TPS65120 power management device, a single-inductor quadruple output TFT LCD power supply [4].

II. Power Management System With Active Dropout Optimization

Fig. 1 shows a Power Management System for low output voltage ripple and optimized efficiency. The energy on the input, V_{IN} of a system is transferred via a switched mode converter (Buck-; Boost-Converter; Charge Pump; …) to a certain output converter voltage called V_{BOOT}.

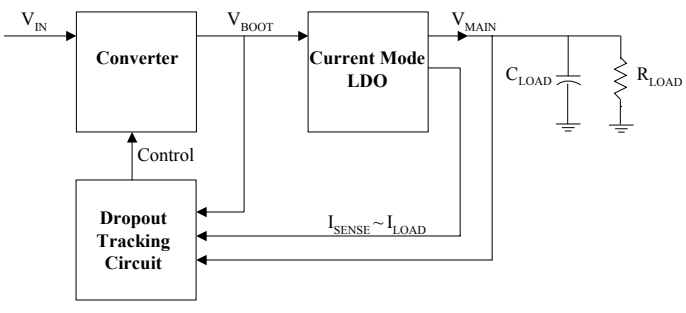

Fig. 1. Block Diagram of a Power Management System with DC/DC Switched Mode Voltage Converter, Current Mode LDO and Dropout Tracking Circuit for low ripple and optimized efficiency

0-7803-9033-4/05/$20.00 ©2005 IEEE.

A current mode LDO converts V_{BOOT} with a relative high voltage ripple to the output voltage V_{MAIN} with low ripple. The third (new) system component is called "dropout tracking circuit".
This block compares the voltages V_{BOOT} with V_{MAIN} and sends a control signal which is dependent on the load current I_{LOAD} at the output of the system to the switched-mode DC/DC converter (e.g. to modify the duty cycle).
The goal of this configuration is a low output voltage ripple at V_{MAIN} without high efficiency losses. To minimize the efficiency losses, the DC/DC converter output voltage V_{BOOT} is controlled via the dropout tracking circuit in a way that the voltage across the LDO pass element is minimized.

A. Function of Dropout Tracking Circuit in the Power Management System

Fig.2 shows the LDO which is designed in a current mode configuration and the Dropout Tracking Circuit more in detail. The internal compensated (C_C , R_C) gm-stage (error amplifier) of the current mode LDO compares the voltage V_{FB} on the feedback divider R2 and R3 with a reference voltage V_{REF}. The output of the gm1-stage controls the source follower M1. This follower works as a voltage to current converter in the output-stage. The current through R1 is mirrored via M2 with a current amplification factor k to the pass transistor M3. Dependent on the output load of the LDO the gate-source voltage of M3 is controlled. The sense transistor M4 sends a current I_{SENSE} which is proportional to the output current I_{LOAD} to the dropout tracking circuit.

Depending on the type of the converter (hysteretic or linear regulated PWM converter) the dropout tracking circuit has to be realized as a hysteretic type with a comparator or linear type with an OP-AMP. The output voltage "quality" of the system (voltage ripple; accuracy; power-supply-rejection…) is solely determined by the control loop characteristics of the current-mode LDO.
The dropout tracking circuit works as the error- amplifier in the DC/DC converter and has to be designed for this need (e.g. accuracy, compensation, gain). Additionally it ensures that the current-mode LDO has enough voltage drop across its pass element for good ripple rejection under all load conditions. To do this job, the hysteretic comparator in the example illustrated in Fig. 2 compares the voltages V_{MAIN} and V_X so that V_X is equal to:

$$VX = VBOOT - dV \qquad (1).$$

The offset voltage dV across R4 is proportional to the dropout of the LDO pass element M3. V_X is depending on the load current. For higher load current dV increases and the comparator sends a control signal to the converter to increase V_{BOOT}. This also means a controlled increase in dropout voltage (V_{DS}) of M3. So the output current (I_{LOAD}) dependent control signal of the dropout tracking circuit controls the DC/DC converter output voltage V_{BOOT} e.g. via changing the duty cycle or by switching the converter on and off (hysteretic control).
The current I_{BASIC} generates a load current independent offset voltage dV which defines the minimum dropout voltage of the LDO at zero output current.

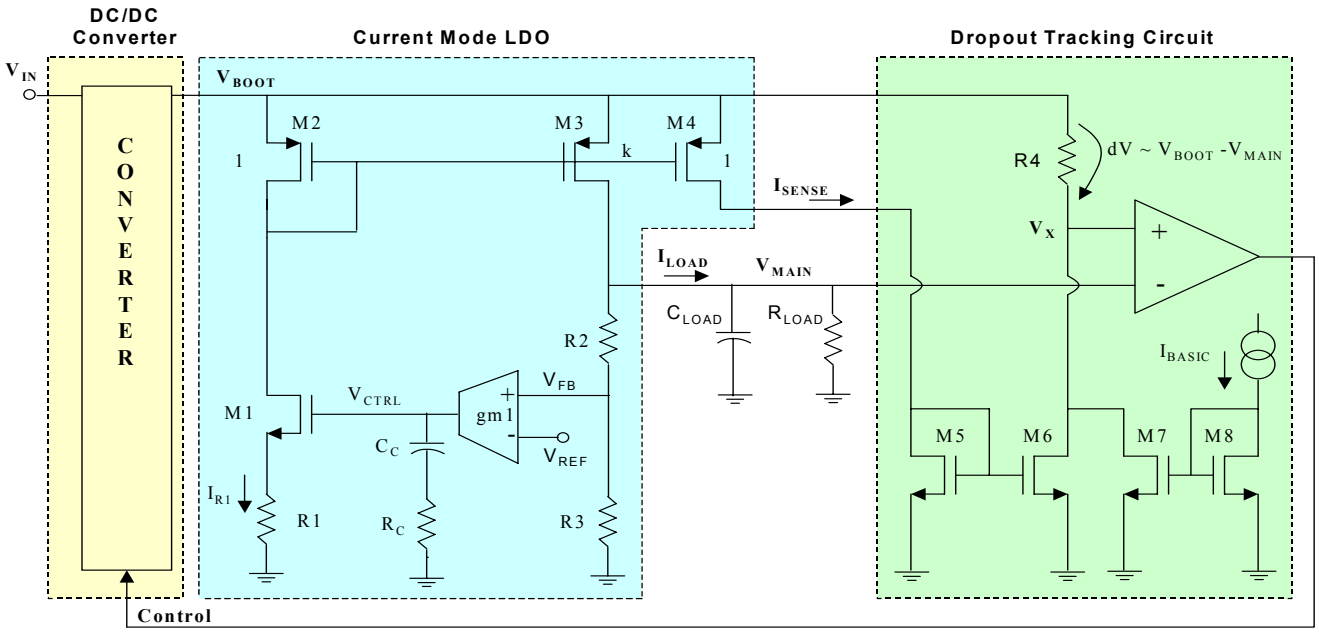

Fig. 2. Converter with the detailed circuits of the Current Mode LDO (error amplifier with output stage) and the Dropout Tracking Circuit

B. Dimension of the Dropout Tracking Circuit

This section shows the basic DC equations to dimension the dropout tracking circuit. Figure 3 illustrates the dependency of the DC/DC converter output voltage V_{BOOT} on the load current I_{LOAD}. V_{BOOT} is given by:

$$VBOOT = VMAIN + dV \quad (2).$$

When the output current I_{LOAD} is varied from zero to full load, the offset voltage dV increases proportional to the load. The consequence is that the converter output voltage V_{BOOT} rises with increasing I_{LOAD}. So for higher load current the voltage drop across the LDO pass element increases.

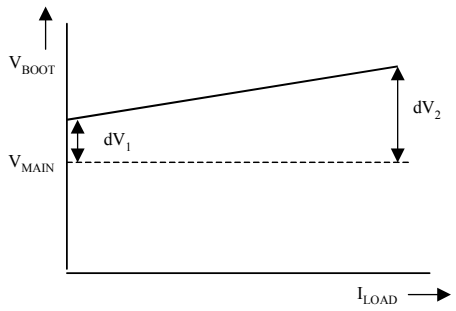

Fig. 3. Dependency of V_{BOOT} on I_{LOAD}

The offset voltage dV ($dV=V_{BOOT}-V_{MAIN}$) is equal to the drain to source voltage V_{DS} of the regulated PMOS pass-transistor M3 (see Figure 2). The basic offset dV_1 see Fig. 3 is chosen so that the power transistor M3 works in the saturation region at minimum load current. The basic offset is given by

$$dV_1 = I_{BASIC} \cdot R_4 \quad (3).$$

The maximum offset dV_2 is choosen so that the power transistor M3 works in the saturation region at maximum load. The max offset is given by

$$dV_2 = (I_{BASIC} + \frac{I_{LOAD}}{k}) \cdot R_4 \quad (4).$$

The offset voltages dV_1 and dV_2 are also visible in a principle output characteristic of the regulated transistor M3 (see Fig. 4).

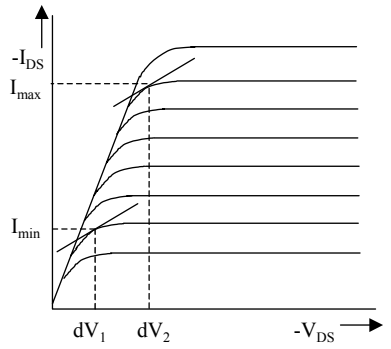

Fig. 4. Output characteristic of regulated FET M3

The operating points of transistor M3 are in the saturation region nearby the linear region. In this operation the output resistance r_0 of M3 increases and the PSRR (power supply rejection ratio) also increases to get a low output voltage ripple behavior of V_{MAIN}. The Dropout Tracking Circuit changes the V_{DS} of M3 dependent on the load current to reduce efficiency losses. In first order the efficiency losses are dependent on the ratio between the dropout voltage dV and to the output voltage V_{MAIN}. Therefore:

$$EfficiencyLoss = \frac{dV}{V_{MAIN}} \quad (5).$$

The efficiency is given by the ratio of V_{MAIN} to V_{BOOT}. A standard converter/LDO combination without dropout tracking runs with a constant dropout voltage which is defined by a fixed V_{BOOT}/V_{MAIN} ratio. Therefore the standard circuit is not optimized in efficiency. Also there is the risk that the regulated transistor could work in the linear region at heavy load which a drastically reduced ripple rejection.

III. Current Mode LDO with PMOS Passelemnt

A current mode LDO means that the PMOS passelement M3 works like a voltage controlled current source. This configuration is very attractive in combination with the dropout tracking circuit. Fig. 5 shows a comparison of current-mode (a) and the commonly used voltage mode LDO (b). In the voltage-mode LDO the output of an OTA (M1 and M2) stage directly controls the gate of the PMOS passelement [5] - [10]. The passelement M3 of the current mode LDO works in saturation region as a controlled current source. Here the transistors M2 and M3 form a current mirror with a current amplification factor k .
The drain current of M2 is generated from the combination: M1/R1 which works as a voltage to current converter which transfers the control voltage V_{CTRL} into to current I_{R1}. This current I_{R1} is then mutiplied with k into the load current I_{LOAD} of the current mode LDO.

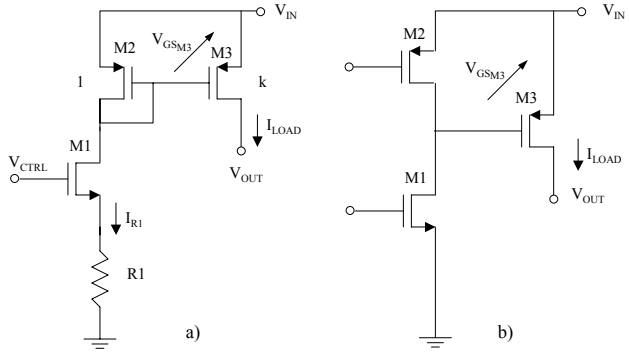

Fig. 5. a) Current Control scheme b) Voltage Control scheme

The output transistor of the current mode LDO (M3) always runs with a small value of $V_{GS} - V_T$, so V_{GSM3} is close to the threshold voltage of M3. For a first order estimation one can use the following rule:

$$(V_{GS} - V_T)_{MAX} = V_{DSSAT} \qquad (6).$$

This means for a small dropout voltage (V_{DSSAT}) the pass element M3 can only run with a small $V_{GS} - V_T$ to keep the output impedance at a high level. This ensures a high DC-gain and also a high PSRR over the total output current range since the pass-element M3 always works in saturation region. The high output impedance of M3 forms a (low-frequency) pole in combination with the load capacitance. Therefore the output stage of the current-mode LDO inherently has a high PSRR at high frequencies.

A current mode system therefore guarantees a low output voltage ripple over a wide load current- and frequency range.

In the voltage controlled scheme (b) the passelement works either in saturation or in linear region depending on the load current. V_{GSM3} changes from the threshold voltage V_T to V_{IN}. Here the DC-gain, the external pole and PSRR of M3 strongly varies over the whole output current range.

One further drawback of a voltage mode system is that there is no precise load current information on the pass element like in a current mode system where an additional mirror transistor easily can be implemented.

Since a current mode LDO pass element only works in saturation region, the transistor size is bigger for a low saturation voltage at maximum output current compared with a voltage mode system where the pass transistor is driven with the full rail to rail voltage.

Fig. 6 shows first order equations to compensate the feedback loop and to predict the two poles and the zero of the current-mode LDO section illustrated in Fig. 2. The equations are valid when the pass element is in saturation [3].

Pole 1:

$$f_1 = \frac{1}{2 \cdot \pi \cdot C_C \cdot (r_{Ogm1} + R_C)} \qquad (7)$$

Pole 2:

$$f_2 = \frac{1}{2 \cdot \pi \cdot C_{LOAD} \cdot (r_{OM3} // R_{LOAD})} \qquad (8)$$

Zero of Compensation:

$$f_Z = \frac{1}{2 \cdot \pi \cdot C_C \cdot R_C} \qquad (9)$$

DC-Gain gm1-Stage:

$$A_{I1} = g_{m1} \cdot r_{ogm1} \qquad (10)$$

DC-Gain LDO Output-Stage:

$$A_{I2} = g_{m2} \cdot (r_{OM3} // R_{LOAD}) \qquad (11)$$

with

$$g_{m2} = \frac{g_{mM1}}{1 + g_{mM1} \cdot R_1} \cdot k \qquad (12)$$

Total Open-Loop DC-Gain:

$$A_{TOT} = A_{I1} \cdot A_{I2} \cdot \frac{R_3}{R_2 + R_3} \qquad (13)$$

Gain-Bandwidth:

$$GBW = \frac{g_{m1} \cdot g_{m2} \cdot (r_{ogm1} // R_C)}{2 \cdot \pi \cdot C_{LOAD}} \cdot \frac{R_3}{R_2 + R_3} \qquad (14)$$

Fig. 6. Small Signal Parameters of the Current Mode LDO

The parameters in the equations are referred to the components in Fig. 2 ;

Additionally the following parameters have been defined:

ro_{gm1} = output resistance of gm1;

gm_{M1} = trans-conductance of M1;

ro_{M3} = output resistance of M3.

The dominant pole in the system varies with the load current. For heavy load the dominant pole is defined by the internal pole f_1 at light load it is defined by the external pole f_2. The total open loop DC-gain is the product of the gains of gm1-stage and the output-stage (source follower M1 with current mirror M2 and M3) and therefore depends on R_{LOAD}. The lowest gain is at minimum R_{LOAD}. The bode-plot in Fig. 7 shows the gain and phase for different load currents (0.1mA, 10mA, 20mA). The Phase Margin for this load current range is above 55° and the total DC-gain is about 60dB. This means a stable LDO and enough gain for a high output voltage accuracy. The results from the bode diagram for three different loads are displayed in Table I.

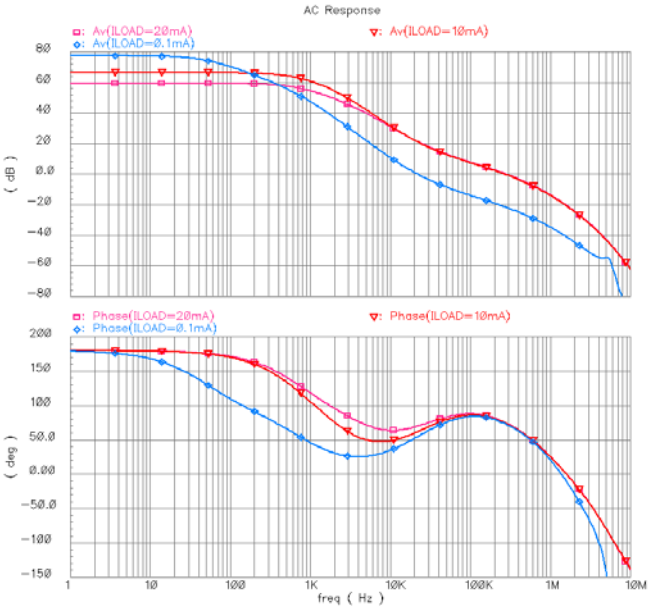

Fig. 7. Bode Plot of Current Mode LDO at different loads

TABLE I
RESULTS FROM THE BODE PLOT

PARAMETER	I_{LOAD} (0.1mA)	I_{LOAD} (10mA)	I_{LOAD} (20mA)
A_{TOT}	77dB	66dB	59dB
Gain Margin	-39dB	-21dB	-20dB
Phase Margin	55°	75°	74°
GBW	22kHz	271kHz	182kHz

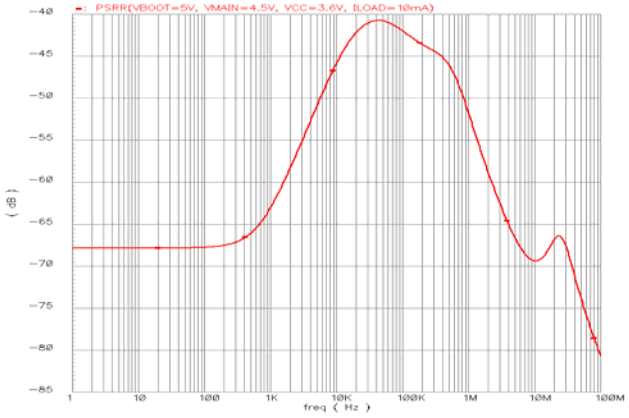

Fig. 8. Power Supply Ripple Rejection of Current Mode LDO at I_{LOAD}=10mA and dV=400mV

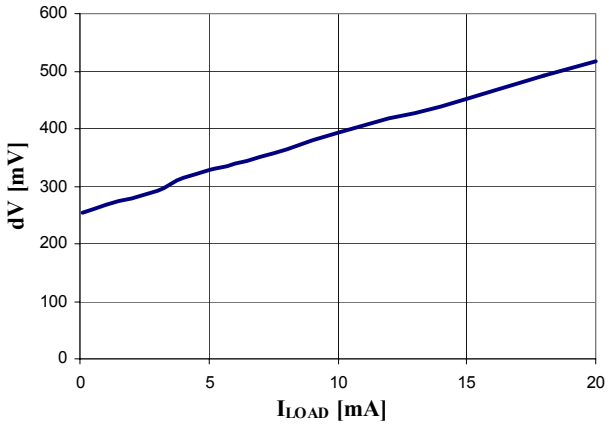

Fig. 9. Offset Voltage (Dropout) versus I_{LOAD}

An LDO with a high PSRR in the required frequency band and a fast line transient response results in a good ripple rejection ratio. This is important for a post regulator of switched mode power converters. The control loop tends to be the dominant contributor of supply rejection for low frequencies. The pass element of a current mode control LDO always works in the saturation region these results in a high output resistance. This resistance in combination with the load capacitance C_{LOAD} guarantees a high ripple rejection at high frequencies. The PSSR over frequency is shown in Fig. 8. For a converter switching frequency of 1.5MHz a PSRR of 58dB can be obtained (Fig. 8). Therefore there is no feedback loop activity necessary which results in a fast response. Due to the dropout tracking circuit the high output resistance is guaranteed over the whole load current range. The good ripple rejection at high frequencies can only be realized with low ESR load capacitors C_{LOAD}.

IV. Experimental Results

The power management system in Fig. 2 was specified for an input voltage range from V_{IN}=2.5V to 5V. Table II shows the main system parameters.

TABLE II
MAIN PARAMETERS OF POWER MANAGEMENT SYSTEM

PARAMETER	VALUE
V_{BOOT}	3.5V ... 5.8V
V_{MAIN}	3.0V ... 5.6V
V_{REF}	1.21V
I_{LOAD}	0 ... 20mA
C_{LOAD}	0.22uF

The switched mode converter was realized as a peak current controlled hysteretic boost topology with a switching frequency of 1.5MHz. The integrated system is implemented in a 3x3mm QFN Package.

The dropout tracking circuit in the TPS65120 was adjusted for a higher offset (consider comparator offset and process spread) because low ripple was more important in this application than an extremely high efficiency especially at light load. The average offset voltage over the load current is shown in Fig. 9. The accuracy of V_{MAIN} was better than 1% (including line and load regulation, V_{REF} drift, error amplifier offset, temperature coefficient). Due to the hysteretic control, the boost converter produces a relatively high output voltage ripple in the range of 100mV peak to peak. The result in Fig. 10 from a lab measurement shows a voltage ripple on V_{BOOT} of about 105mV. On the LDO output at V_{MAIN}=5V a very low ripple of about 7mV could be realized over the specified load current range.

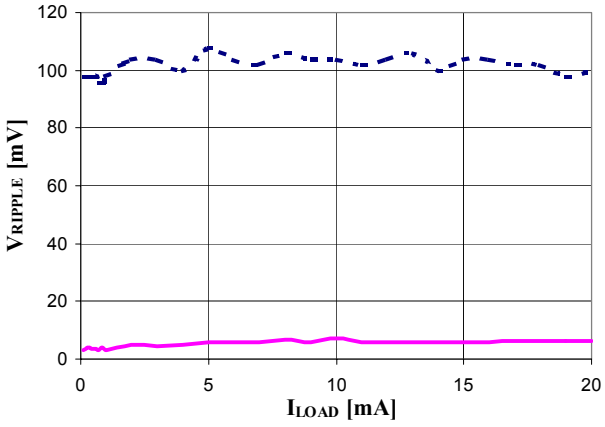

Fig. 10. Output Voltage Ripple on V_{BOOT} (dotted line) and V_{MAIN} (solid line) versus Load Current

The high efficiency of the LDO illustrated in Figure 11 is due to the dropout tracking regulation circuit minimizing the difference between V_{BOOT} and V_{MAIN}. Fig. 12 shows a typical load current transition from zero to 10mA. The load transient plot shows a stable system with low over- and undershoots of V_{MAIN} and fast settling time. The voltage drop and overshoot on V_{MAIN} is about 1.2%.

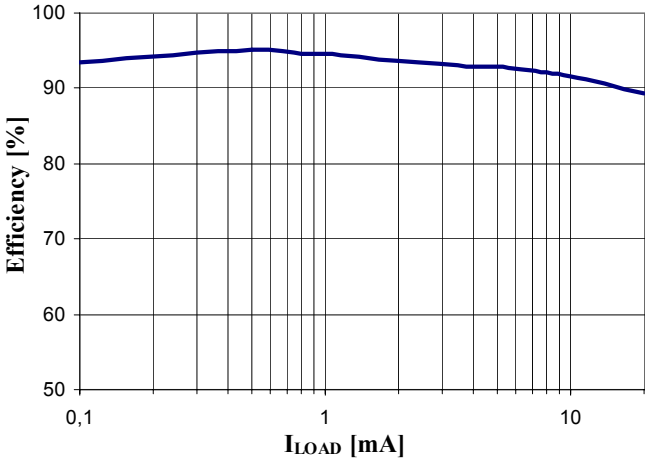

Fig. 11. LDO efficiency V_{MAIN}/V_{BOOT} versus I_{LOAD}

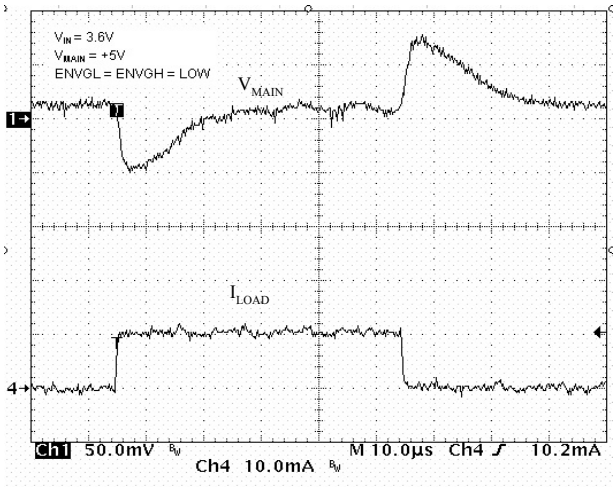

Fig. 12. Load Transient behavior on V_{MAIN} =5V
(Ch1: 50mV/div, Ch4: 10mA/div, time: 10us/div)

V. Conclusion

With a combination of dropout tracking circuit and current mode LDO an extremely low output voltage ripple (compared with a converter only) is possible. The LDO dropout is minimized such that a high power supply rejection can be guaranteed at optimized efficiency. This concept is possible for all converter topologies like Buck-, Boost-Converter, Charge Pumps etc. The converter can be regulated in a PFM mode without sacrificing ripple performance. The current mode LDO output stage guarantees in combination with the load capacitance a good PSRR and a fast line transient response without any activity of the regulation loop. Since the load current is inherently limited, inside the current mode LDO the total system is short circuit protected without additional effort in the voltage converter.

References

[1] Ernst Lueder, "Liquid Crystal Displays", John Wiley & Sons, 2001

[2] T. Ying, W.H. Ki, and M. Chan, "Area Efficient CMOS Integrated Charge Pumps", ISCAS 2002, IEEE International Symposium on Circuits and Systems, Vol. 3, pp. 831-834, 2002

[3] G. Thiele and E. Bayer, "Current Mode Charge Pump, Topology, Model and Control", IEEE Power Electronics Specialists Conference, pp. 3812-3817, June 2004

[4] "TPS65120: Single-Inductor Quadruple-Output TFT LCD Power Supply", Texas Instruments, Texas Instruments Datasheet, TPS65120, 2004, http://www.ti.com/

[5] C. K. Chava and J. Silva-Martinez, "A Frequency Compensation Scheme for LDO Voltage Regulators", IEEE Transactions on circuits and systems: Regular Papers, Vol. 51, No. 6, pp. 1041-1050, 2004

[6] S. K. Lau, K. N. Leung and P. K. T. Mok, "Analysis of Low-Dropout Regulator Topologies for Low-Voltage Regulators", IEEE Conference on Electron Devices and Solid-State Circuits, pp. 379-382, 2003

[7] G. A. Rincon-Mora and P. E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator", IEEE Journal of Solid-State Circuits, Vol. 33, No. 1, pp. 36-44, 1998

[8] H.J. Shin, S.K. Reynolds, K.R. Wrenner, T. Rajeevakumar, S. Gowda and D.J. Pearson, "Low-Dropout On-Chip Voltage Regulator for Low-Power Circuits", IEEE Symposium on Low Power Electronics, pp. 76-77, 1994

[9] W. Chen, W.H. Ki and P.K.T. Mok, "Dual-Loop Feedback for Fast Low Dropout Regulators", IEEE Power Electronics Specialists Conference, Vol. 3, pp. 1265-1269, June 2001

[10] D. Heisley and B.Wank, "DMOS delivers dramatic performance gains to LDO regulators", EDN, Vol. 45, pp. 141-150, June 2002, http://www.ednmag.com