A Fast Transient Response Capless LDO Regulator Achieving -78 dB of PSR Up to 2 MHz

Xiang Cheng, Huihua Liu, Jingzhi Zhang, Yiming Yu, Yunqiu Wu, Chenxi Zhao, Kai Kang*
School of Electronic Science and Engineering
University of Electronic Science and Technology of China, Chengdu 611731, China
*Email: kangkai@uestc.edu.cn

2024 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-3099-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCAS58744.2024.10558458

***Abstract*—This paper presents a fast transient response capless low-dropout (LDO) regulator in 65 nm CMOS process for system-on-chip (SOC). The LDO regulator utilizes a feedforward ripple cancellation circuit (FFRCC) to achieve high power supply rejection (PSR), and a voltage damper is used to enhance transient response. Besides, a negative capacitance circuit (NCC) is added to the gate of the power stage to expand the bandwidth of FFRCC. The proposed LDO regulator is fabricated in 65 nm CMOS technology. Its voltage recovery time is 1.1 µs and 400 ns, respectively, when the load current steps from 200 µA to 50 mA or 50 mA to 200 µA with the rise/fall time of 100 ns. Its overshoot and undershoot voltages are 114 mV and 98 mV, respectively. Moreover, the regulator achieves -78 dB PSR at 2 MHz.**

Keywords—Feedforward ripple cancellation circuit (FFRCC), power supply rejection (PSR), negative capacitance circuit (NCC), low-dropout regulator (LDO).

I. INTRODUCTION

With the development of system-on-chip (SOC) towards high integration and low noise, the power management system is required to have the characteristics of small area and wide bandwidth power ripple rejection. As a critical module in power management, the low-dropout regulator (LDO) faces many challenges. The traditional LDO is usually connected with an off-chip large capacitor to suppress power supply noise through the capacitor, but the external output capacitor needs to occupy a large area, which is not conducive to the large-scale integration of SOC. However, capless LDO usually uses frequency compensation technology to achieve loop stability without a large external output capacitors, but has poor power ripple suppression performance.

Due to the high loop gain of the LDO negative feedback loop, a typical LDO has good power supply rejection (PSR) at lower frequencies. However, as the frequency increases, the gain of the negative feedback loop decreases, and the PSR begins to degrade [1]. Given the increase in operating frequency, how to achieve a high PSR over a wide frequency range is critical. Since LDO is also used in brain-computer interface chips, it is required to have faster transient response.

Prior work on increasing power supply suppression includes pre-tuning the power supply voltage [2]. An NMOS is inserted between the power stage and the power supply as a cascode transistor to increase the impedance between the power supply and the LDO output. This method can improve the PSR of 30 dB at medium and high frequencies, but there are some disadvantages. Firstly, the gate voltage of a cascode transistor is higher than the supply voltage, which is usually achieved by using a charge pump. Therefore, in order to avoid the noise caused by the charge pump, a low-pass filter is followed, and the area is also increased. Secondly, it will increase the voltage drop on the power transistor, thereby reducing efficiency.

The feedforward ripple cancellation technique of voltage mode is demonstrated in [3], and the improvement to PSR is only achieved at the 25 mA load current and at the cost of static power consumption. For larger load current, an increase in power transistor size will require a wider bandwidth for the amplifier, resulting in an increase in static power consumption. Based on the traditional feedforward ripple elimination technology, a current mode feedforward ripple elimination technology is presented in [4], which does not use additional adder circuits, thus reducing power consumption and complexity. However, the feedforward ripple path still requires the operational transconductance amplifier (OTA), and the PSR performance of the LDO regulator is limited by the bandwidth of OTA. Another effective way to improve PSR is to use a negative capacitance circuit [5] to eliminate the parasitic capacitance at the gate of the power transistor, so that the noise at the gate of the power stage is consistent with the power supply noise, thus eliminating the leakage current at the LDO output. When the current flowing through the power transistor changes, the parasitic capacitance at the gate of the power stage will change, so the negative capacitor circuit can't eliminate the parasitic capacitance well, leading to the deterioration of the PSR performance.

In this paper, a capless LDO regulator that achieves high PSR and fast transient response compared to other capless LDO regulators. This paper is organized as follows. The proposed PSR enhancing scheme is presented in Section II. Design considerations for the fundamental circuit blocks are discussed in Section III. Simulation and experimental results of the proposed LDO regulator are presented in Sections IV and V, respectively, followed by the conclusion in Section VI.

II. PROPOSED LDO REGULATOR

The proposed capless LDO achieves high PSR performance over a wide frequency range with a smaller and simpler circuit. Fig. 1 shows the basic modules of the proposed LDO regulator composed of an error amplifier (EA), a power transistor M_P, a buffer, a voltage damper (VD), and the feedforward ripple cancellation circuit (FFRCC) and the negative capacitance circuit (NCC). R_P and C_P are the parasitic resistance and capacitance at the output node of the buffer. R_L and C_L refer to the load resistor and load capacitor, respectively. The proposed LDO regulator sets the output node of the error amplifier as the dominant pole without the additional frequency compensator. The output nodes of the buffer and the LDO regulator are both non-dominant poles. The stability of the LDO regulator is ensured by pushing the non-dominant poles to the higher frequency.

This work is supported by the National Natural Science Foundation of China (Grant No. 62025106, 62171102, 61931007).

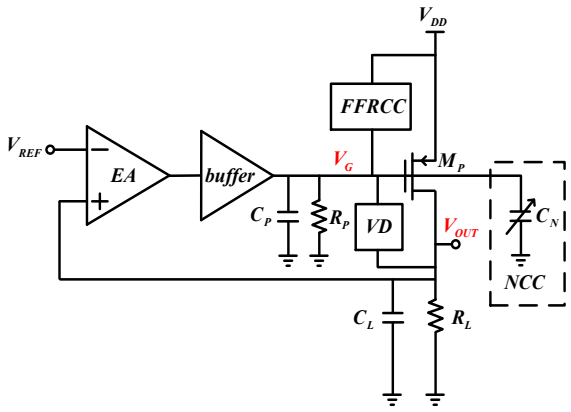

Fig. 1. Basic modules of the proposed LDO regulator.

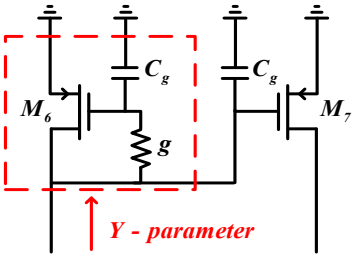

Fig. 3. Small-signal equivalent circuit of high speed current mirror.

The low frequency power supply ripple in conventional LDO regulators is effectively suppressed due to the high loop gain. High frequency power supply noise changes the small signal gate-source voltage of M_P to generate leakage current. The PSR performance is degraded by affecting the output voltage of the LDO regulator. FFRCC introduces a feedforward path between the power supply and the gate of the M_P to replicate the high frequency power supply ripple to the gate of the M_P, thereby reducing the leakage current from the power supply to the regulator output. NCC is modeled as a capacitor with a negative value. It is used to eliminate a part of the capacitance at the output node of the feedforward path in order to extend the bandwidth of the feedforward path.

III. Circuit Implementation

A. Feedforward Ripple Cancellation Circuit

Fig. 4 shows the schematic of the feedforward ripple cancellation circuit. Since I_2 is an ideal current source, no small signal current flows into this current source due to its infinite output impedance. Therefore, the small signal voltage at node V1 is approximately equal to the power supply ripple and is denoted as vdd. The vdd includes the low and high frequencies of the power supply noise and is expressed as

$$vdd = vdd,lpf + vdd,hpf \tag{1}$$

where vdd,lpf and vdd,hpf are the low and high frequency parts of the power ripple, respectively. The small signal voltage at node V1 reaches V2 after passing through a low-pass filter composed of the resistor R4 and capacitor C3 with a low cut-off frequency. Thus small signal gate-source voltage of M_2 can be derived as

$$|v_{gs2}| = vdd - vdd,lpf = vdd,hpf \tag{2}$$

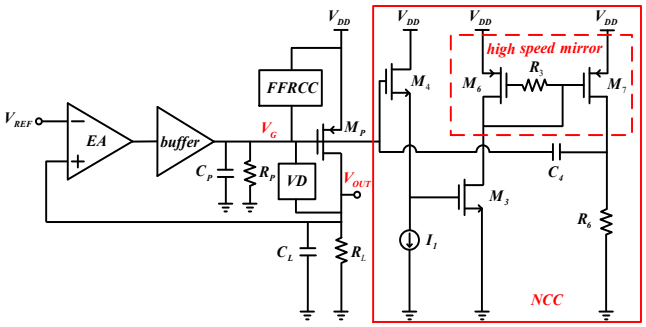

Fig. 2. Implementation of NCC with fundamental blocks.

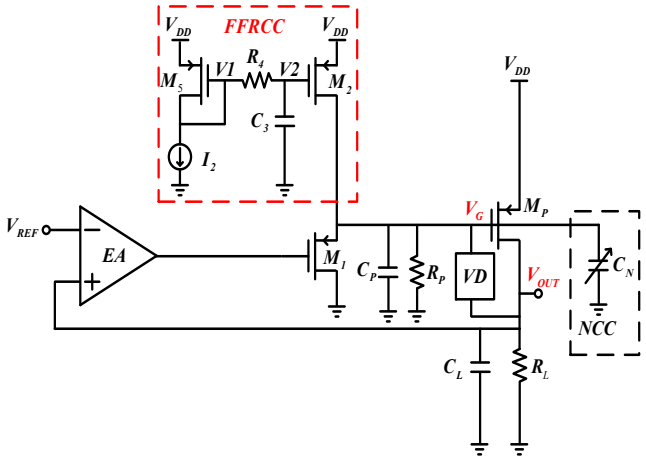

Fig. 4. Implementation of FFRCC with basic modules.

The output node V_G of the feedforward path is connected to the gate of the power transistor M_P. The small signal voltage of the gate of M_P can be expressed as

$$V_G = g_{m2} \times |v_{gs2}| \times \left(\frac{1}{g_{m1}} // \frac{1}{s(C_P+C_N)}\right) \tag{3}$$

where g_{m2} and g_{m1} are the transconductances of PMOS transistor M_2 and M_1, respectively, and C_P is the parasitic capacitance at the gate of M_P. This equation shows that, as long as $C_P + C_N = 0$, the small signal voltage V_G can be insensitive to frequency variations. The objective is to make V_G = vdd,hpf, thereby helping to improve the PSR of the LDO. This can be achieved by adjusting the term g_{m2}/g_{m1} to close to unity. Therefore, the small signal gate-source voltage of the power transistor M_P is equal to zero at high frequency, which effectively reduces the leakage current of M_P.

B. Negative Capacitance Circuit

The schematic diagram of the negative capacitance circuit (NCC) is shown in Fig. 2. The NCC includes the source follower composed of M_4 and I_1, and the in-phase amplifier composed of M_3, M_6, M_7, R_3 and R_6. The capacitor C_4, the source follower and the in-phase amplifier are equivalent to a negative capacitor at the gate of M_P. The value of the capacitance can be given by

$$C_N = (1 - g_{m7} \times R_6) \times C_4 \tag{4}$$

where g_{m7} is the transconductance of the PMOS transistor M_7. Fig. 3 shows the small-signal equivalent circuit of high speed current mirror. M_6 and M_7 have the same size and the transconductances are both equal to g_m. Besides, g is the

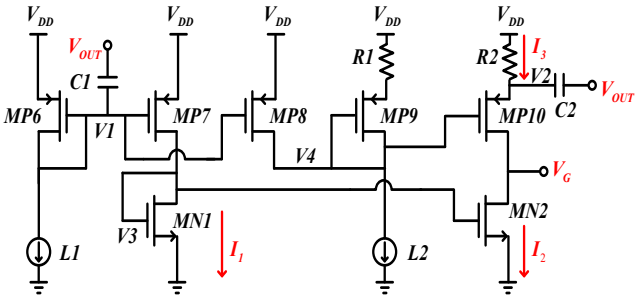

Fig. 5. Detailed circuit diagram of the proposed VD.

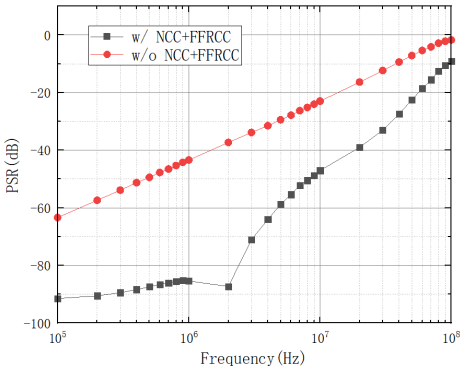

Fig. 6. Simulated PSR performance of the proposed LDO regulator with and without NCC and FFRCC at 25 mA load condition.

the admittance of the resistance. The Y-parameter of the small signal circuit in the red dotted box can be written as

$$Y = \frac{g \cdot sC_g}{g+sC_g} + \frac{g \cdot g_m}{g+sC_g} + g_{ds} = \frac{g \cdot (g_m+sC_g)}{g+sC_g} + g_{ds} \qquad (5)$$

where g_{ds} is the reciprocal of the channel resistance of M_6. The above expression indicates that, if $g_m = g$, the Y-parameter can be insensitive to frequency variations. If there is no the resistor, C_g contributes to the Y-parameter. Therefore, the resistor is used to eliminate the parasitic capacitance at the gate of M_6, pushing the pole to the higher frequency. Compared with the negative capacitance achieved by closed loop negative feedback [4], the negative capacitance circuit can't achieve an accurate capacitance value. However, it can eliminate a part of the capacitance at the output node of the feedforward path over a wide frequency range at the expense of low cost.

C. Voltage Damper

The fast load transient response performance is one of the most important characteristics of the capless LDO regulator because it cannot absorb the voltage peak at the output node by using a large decoupling capacitor when the load current changes [6]-[10].

The schematic diagram of the voltage damper (VD) is shown in Fig. 5. V_{OUT} is the output of the LDO regulator, coupled to V1 and V2 nodes by the capacitors C1 and C2. The V_G is connected to the gate of the power stage in order to charge and discharge the gate parasitic capacitance. When the output current of the LDO regulator increases instantaneously, the power transistor M_P cannot provide sufficient current in time, and the output voltage of the LDO circuit will decrease. According to the characteristics that the

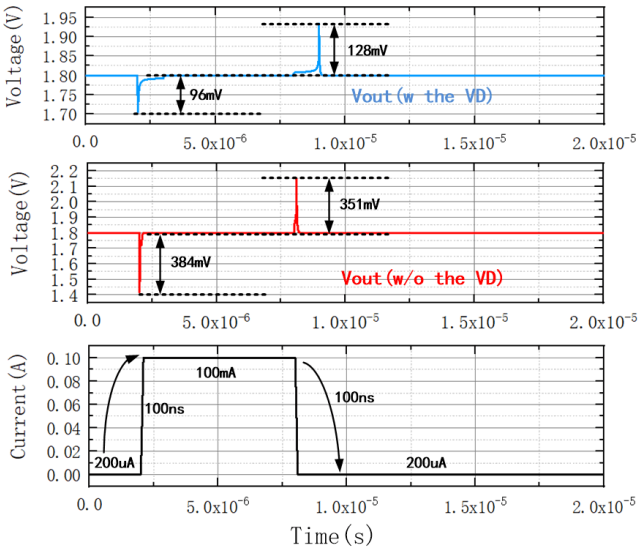

Fig. 7. Simulated load transient response of the proposed LDO regulator with and without VD.

voltage at both ends of the capacitor cannot change abruptly, the voltage V1 of the capacitor C1 and the voltage V2 of the capacitor C2 will decrease correspondingly. At this time, the source-drain current of PMOS transistor MP7 increase correspondingly. After current mirroring, the drain-source current I_1 of MN1 and the drain-source current I_2 of MN2 will also increase correspondingly. At the same time, the source-gate voltage of MP10 and the source-drain current I_3 decrease correspondingly. Since the current flowing into the gate of the power stage is the difference between the source-drain current I_3 of the MP10 and the drain-source current I_2 of MN2, the current (I_3 - I_2) flowing into the gate of the power transistor decreases at this moment, resulting in the decrease in the gate voltage of the power stage. So the increased source-drain current of the power transistor will quickly charge the load capacitor C_L. The output voltage of the LDO regulator is restored to the set value.

IV. Simulation Results

Fig. 6 shows the simulated PSR performance of the proposed LDO regulator with and without NCC and FFRCC at a load current of 25 mA. By reasonably adjusting the transconductance ratio of M_2 and M_1 in Fig. 4, and reasonably adjusting NCC, good PSR performance can be obtained over a wide frequency range. The PSR of the proposed LDO regulator is -89 dB at 1 MHz, and the PSR performance of the proposed regulator is nearly 50 dB higher than the traditional LDO regulator without NCC and FFRCC.

Simulations of the transient response of the proposed LDO regulator with and without VD are shown in Fig. 7. In both cases, the step load current is applied to V_{OUT} from 200 µA to 100 mA with the rise/fall time of 100 ns, and the proposed LDO regulator has the overshoot voltage of 128 mV and the undershoot voltage of 96 mV.

V. Experimental Results

The proposed LDO regulator is fabricated in a 65 nm CMOS. Fig. 8 shows the die microphotograph of the propos-

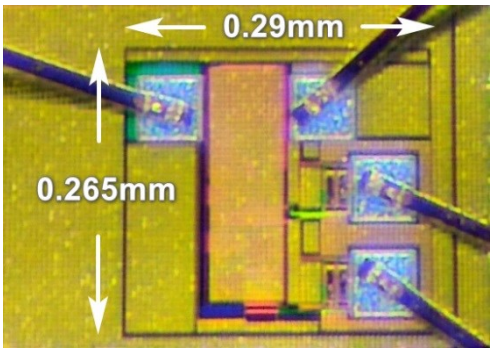

Fig. 8. Microphotograph of the proposed LDO regulator.

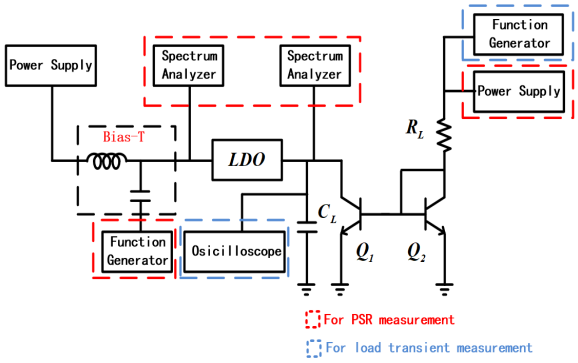

Fig. 9. Measurement setup [4].

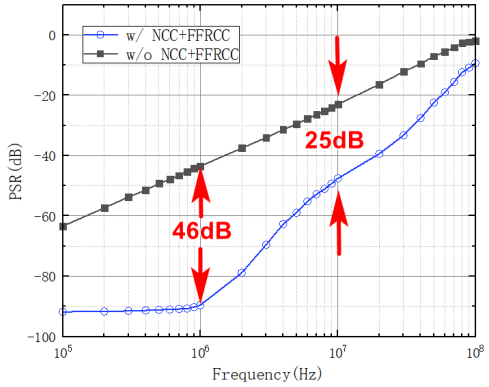

Fig. 10. Measured PSR performance of the proposed LDO regulator with and without NCC and FFRCC at 25 mA load condition.

ed LDO regulator. The active area of the proposed LDO regulator is 0.039 mm^2. The nominal input and output voltage for the LDO regulator are 2 V and 1.8 V, respectively, and the maximum current is 50 mA. The test scheme of PSR and load transient response is shown in Fig. 9. To inject the power ripple, the power supply and the function generator are connected by using a bias tee.

The measured PSR performance of the proposed LDO regulator with and without NCC and FFRCC at a load current of 25 mA is shown in Fig. 10. The PSR of the proposed LDO regulator is less than -40 dB in the frequency range of 0.1 to 10 MHz, compared with the LDO regulator without NCC and FFRCC. Its PSR at 1 MHz and 10 MHz are improved by 46 dB and 25 dB, respectively. The transient response characteristics of the LDO regulator is shown in Fig. 11. The LDO regulator shows the overshoot and the undershoot voltages of 114 and 98 mV, respectively, and the settling time of 400 ns and 1.1 µs when the step load

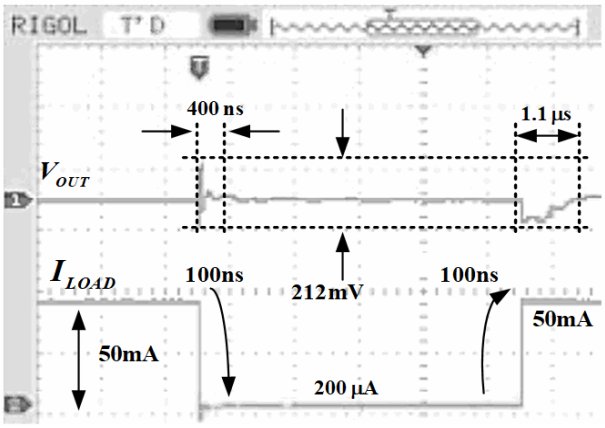

Fig. 11. Measured load transient response of the proposed LDO regulator.

TABLE I. Performance Comparison

parameter	[5]	[11]	[13]	***This work***
process	0.18µm	65nm	65nm	65nm
Power Transistor	PMOS	PMOS	PMOS	PMOS
I_{LOAD} (mA)	100	25	10	50
I_Q (µA)	71 - 101	8 - 297.5	50 - 90	82 - 110
C_{LOAD} (pF)	100	120 / 240	140	10
Input voltage (V)	1.8 - 2.2	1.2	1.15	2
Output voltage (V)	1.6	1	1	1.8
$\Delta Vout$ / $Vout$ (mV/V)	131	225	82	118
PSR	I_{LOAD}=50mA -76dB@ 1MHz -50dB@ 2MHz	I_{LOAD}=25mA -52dB@ 1MHz	-24dB@ 1MHz -12dB@ 5MHz	I_{LOAD}=25mA -91dB@ 1kHz -82dB@ 1MHz -78dB@ 2MHz
Area	0.033mm^2	0.087mm^2	0.023mm^2	0.039mm^2

current is applied to the output of the proposed LDO regulator from 0.2 to 50 mA with the rise/fall time of 100 ns.

Table I compares the proposed LDO regulator with the state-of-the-art works. As can be seen, the proposed LDO regulator has the good PSR performance and transient response performance. The active area of the proposed LDO regulator is 0.039 mm^2.

VI. Conclusion

In this work, a fast transient response capless LDO regulator fabricated in 65 nm CMOS technology is presented. The LDO regulator utilizes FFRCC and NCC to achieve high PSR. With the FFRCC and NCC, 25-46 dB of PSR improvement is observed in the 0.1-10 MHz. The voltage damper is used to enhance the transient response performance of the LDO regulator. The overshoot and undershoot voltages are 114 mV and 98 mV, respectively.

REFERENCES

[1] C. -J. Park, M. Onabajo and J. Silva-Martinez, "External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4–4 MHz Range," in IEEE Journal of Solid-State Circuits, vol. 49, no. 2, pp. 486-501, Feb. 2014.

[2] H V. Gupta and G. A. Rincon-Mora, "A 5mA 0.6μm CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance," 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, San Francisco, CA, USA, 2007, pp. 520-521.

[3] M. El-Nozahi, A. Amer, J. Torres, K. Entesari and E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique," in IEEE Journal of Solid-State Circuits, vol. 45, no. 3, pp. 565-577, March 2010.

[4] K. Joshi, S. Manandhar and B. Bakkaloglu, "A 5.6 μ A Wide Bandwidth, High Power Supply Rejection Linear Low-Dropout Regulator With 68 dB of PSR Up To 2 MHz," in IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2151-2160, Aug. 2020.

[5] A. S. J. Yun, J. S. Yun and Y. S. Kim, "Capless LDO Regulator Achieving −76 dB PSR and 96.3 fs FOM," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 10, pp. 1147-1151, Oct. 2017.

[6] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," in IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 933-940, April 2005.

[7] Y. -H. Lam and W. -H. Ki, "A 0.9V 0.35 μm Adaptively Biased CMOS LDO Regulator with Fast Transient Response," 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, San Francisco, CA, USA, 2008, pp. 442-626.

[8] P. Y. Or and K. N. Leung, "An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection," in IEEE Journal of Solid-State Circuits, vol. 45, no. 2, pp. 458-466, Feb. 2010.

[9] C. Zhan and W. -H. Ki, "An Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator With Subthreshold Undershoot-Reduction for SoC," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 5, pp. 1119-1131, May 2012.

[10] M. R. Valero Bernal, S. Celma, N. Medrano and B. Calvo, "An Ultralow-Power Low-Voltage Class-AB Fully Differential OpAmp for Long-Life Autonomous Portable Equipment," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, no. 10, pp. 643-647, Oct. 2012.

[11] Y. Lim, J. Lee, S. Park, Y. Jo and J. Choi, "An External Capacitorless Low-Dropout Regulator With High PSR at All Frequencies From 10 kHz to 1 GHz Using an Adaptive Supply-Ripple Cancellation Technique," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2675-2685, Sept. 2018.

[12] J. Guo and K. N. Leung, "A 25mA CMOS LDO with −85dB PSRR at 2.5MHz," 2013 IEEE Asian Solid-State Circuits Conference (A-SSCC), Singapore, 2013, pp. 381-384.

[13] Y. Lu, Y. Wang, Q. Pan, W. -H. Ki and C. P. Yue, "A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 707-716, March 2015.