Comp E 475

Microprocessors

Assignment 4: Instruction Data

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10/11/2020

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Task Description

In this assignment we have to write a 'skeleton' for ARM instruction decoder module. With 2 inputs, one of which is clock and another is register where instruction itself is taken from, and 2 outputs for instruction type and data instruction type. 3 and 4 bit length, respectively. We have to synthesize the code, and upload the project on git, having at least 3 commits.

Solution

First, I created module with all the input/outputs mentioned in the project requirements. See on figure 1/

```
1
2  module INSTR_DATA(
3     input clk,
4     input wire[31:0] instruction,
5     output reg[2:0] instr_type,
6     output reg[3:0] data_instr_type
7      );
8
```

Figure 1 module instantiation

Instruction type is determined by 27th and 26th bits of our 32bit input. I used short conditional statement to write the logic of it, which can be seen on figure 2.

```
instr_type = instruction[27] && !instruction[26] ? 2'b11 :
                    !instruction[27] && instruction[26] ? 2'b10 :
                    !instruction[27] && !instruction[26] ? 2'b01:
                    2'b00;
```

Figure 2 instruction type logic

And data instruction is determined by more than just two bits and is more complicated, logic can be seen in figure 3.

```
data_instr_type = instruction[25] ? 3'b001 :
                        !instruction[25] && !instruction[4] ? 3'b010 :
                        instruction[25] && !instruction[7] && instruction[4] ? 3'b011 :
                        !instruction[25] && !instruction[24] && !instruction[7] &&
                        instruction[6] && instruction[5] && !instruction[4] ? 3'b100 :
                        3'b000;
```

Figure 3 data instruction type logic

Those bit numbers are taken from our lecture slides.

Whole code can be seen in attached Verilog file.

Simulation & Verification

We did not have to create simulation or implement this code on board, we needed just a combinational logic.

Comparison

The code synthesis report shown us some warnings due to following reason: Not all bits of our instruction input were used to determine the output logic.

Conclusion

This assignment was a first try to see how machine code is read as an instruction and we had to come up with a logic to control output based on such an instruction. The assignment was interesting and educational, as we also learned and practiced using github.