LINEAR FILTERS

1. Theoretical Considerations

Linear filters are devices composed of shift registers and XOR gates (modulo-2 adders), which are capable of processing binary (0 and 1) sequences for various purposes like coding, decoding, selection etc.

Linear filters are often used as circuits for multiplication and division of polynomials with binary coefficients, used for example for implementing cyclical codes.

For multiplication and division, the input and output sequences represent the coefficients of the polynomials in decreasing order of the powers of x.

Let us consider a general multiplication circuit. The structure of the circuit is determined by the polynomial:

$$g(x) = g_m x^m \oplus g_{m-1} x^{m-1} \oplus ... \oplus g_0, \text{ unde } g_m = g_0 = 1, \text{ iar } g_i \in \{0,1\},\ i = \overline{1, m-1}$$

At the input of this circuit, a second polynomial is applied:

$$a(x) = a_n x^n \oplus a_{n-1} x^{n-1} \oplus \ldots \oplus a_0, a_i \in \{0,1\}, i = \overline{0, n}$$

Multiplying the polynomial $a(x)$ with the polynomial $g(x)$ is achieved by applying the coefficients of the polynomial $a(x)$, in decreasing order of the powers of *x*, one coefficient for each clock impulse, at the input of the multiplication circuit depicted in Fig.1.

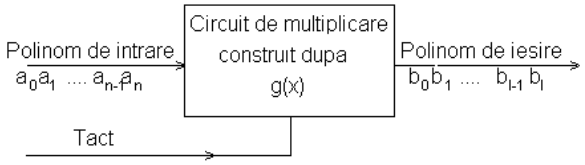

Figure1

At every clock impulse, at the output of the circuit there will be the coefficients of the output polynomial, $b(x) = g(x) \cdot a(x)$, also in decreasing order of the powers of *x*.

The division operation takes place similarly, and in this case the output of the circuit is the quotient of the division.

Fig. 2, 3, 4, 5 present the schematics of some multiplication and division circuits, as follows:

- fig.2: Multiplication circuit with the XOR gates outside the binary cells;
- fig.3: Multiplication circuit with the XOR gates in-between the binary cells;
- fig.4: Division circuit with the XOR gates outside the binary cells;
- fig.5: Division circuit with the XOR gates in-between the binary cells.

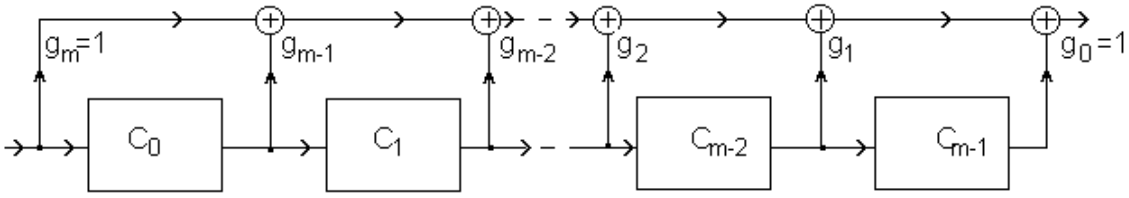

Figura 2

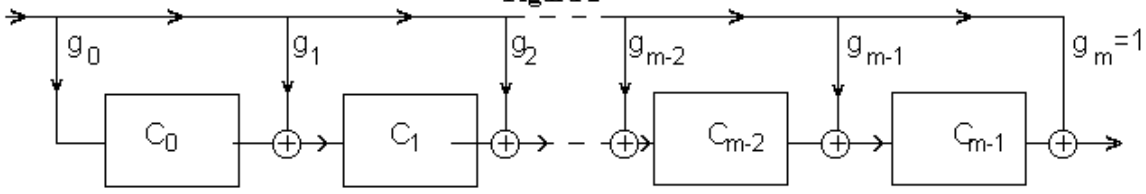

Figura 3

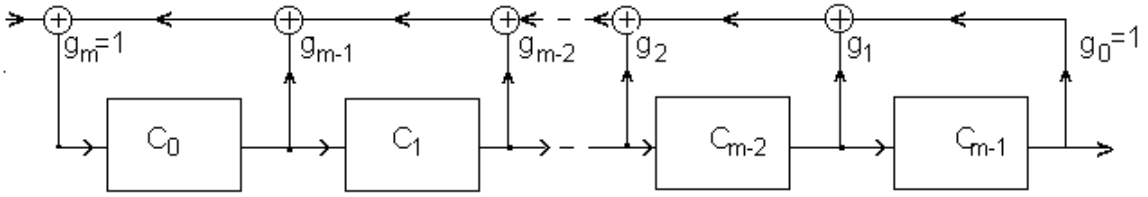

Figura 4

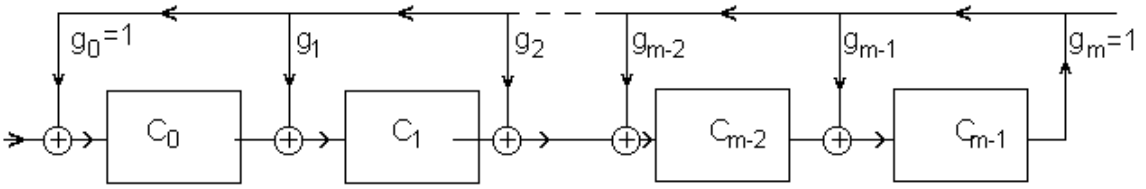

Figura 5

All circuits are constructed after the polynomial:

$$g(x) = g_m x^m \oplus g_{m-1} x^{m-1} \oplus ... \oplus g_0 .$$

Regarding the multiplication and division operations, the following remarks can be stated:

- for multiplication, the degree of $b(x) = g(x) \cdot a(x)$ is $m+n$ (therefore it has $m+n+1$ coefficients), where m is the degree of $g(x)$ and n the degree of $a(x)$. Consequently, after applying the $(n+1)$ coefficients at the input, one must further apply m 0's, in order to allow all coefficients of $b(x)$ to be produced;

- for division, when the last coefficient is applied at the input, the last coefficient of the output is obtained;

- the division operation may produce a remainder or not. If the division has no remainder, after division the cells $C_{m-1}...C_0$ will have state "0". If the division operation produces a non-zero remainder, then after the division the cells $C_{m-1}...C_0$ will not all have state "0", as follows:

a) for the circuit with XOR gates in-between the cells, the remainder is found in the binary cells, with the coefficient of the term with degree *m-1* in cell C_{m-1}, the one of

degree m-2 in cell C_{m-2} etc.

b) for the circuit with the XOR gates outside the binary cells, the remainder is stored in a modified form in the cells.

2. Circuit implementation

The multiplication and division circuits presented above can be implemented with flip-flop circuits (FF) of type D, also known as binary cells, and XOR gates. If the generator polynomial of a circuit has degree 4, the circuits contain four D flip-flops and four XOR gates. Each XOR gate has two inputs and one output. For a binary cell, D is the input and Q is the output. Sometimes a D flip-flop has a second output, denoted as $\overline{Q}$, which is the inverted value of Q. This output is not represented in the circuit schematics shown before, because it is not used. Therefore, the block schematic of a D flip-flop is the one in Fig. 6.

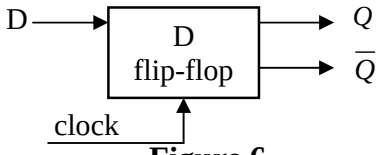

Figure 6

Denoting with *k* the current time, the functioning equation of a D flip-flop is:

$$Q^{(k)} = D^{(k-1)},$$

which means that the circuit applies a delay of one sample to the input signal.

For implementing the circuits in Fig. 2, 3, 4, 5, each coefficient of the polynomial is interpreted as follows:

- $g_i = 1$ means that there is an electrical connection;
- $g_i = 0$ means no electrical connection.

Assuming that the circuit's *clock signal* is applied *automatically* from a clock generator, the input sequence must be applied synchronous with the clock signal, and for this purpose a separate circuit is provided(see Fig.7). In this case the outputs of the flip-flops can be visualized using an oscilloscope.

The circuit in Fig. 7 contains a feedback shift-register composed of four flip-flops A_1-A_4 driven by the same clock signal as the binary cells in the previous circuits. The circuit is initialized with the sequence 1000. After initialization, the states of the register will be 0100, 0010, 0001, 1000...etc. Making various connections from the outputs of the flip-flops $A_1 \div A_4$ to the OR gate, various sequences can be obtained at the output. For example, to obtain the sequence 1001 (representing the polynomial $x^3 \oplus 1$), the outputs of A_1 and A_4 must be connected to the OR gate.

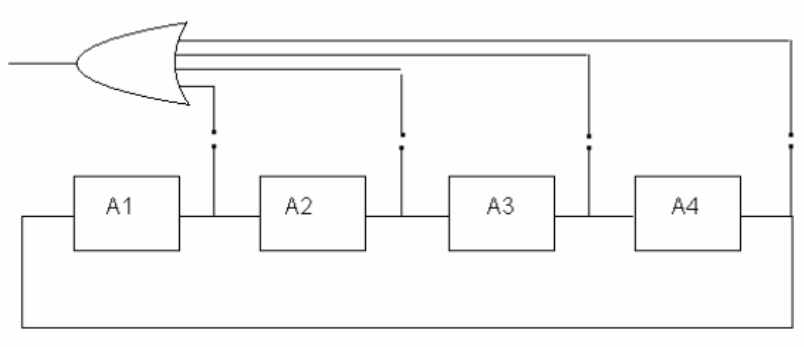

Figure 7

3. Practical exercises

3.1. Draw the schematic of a multiplication circuit based on the polynomial $g(x) = x^3 \oplus x^2 \oplus 1$ (using the model in Fig.2), after identifying the values of the polynomial coefficients $g_i, i = \overline{0,3}$.

3.2. Write the functioning equations of the circuit, based on the functioning equation of a D flip-flop, and fill Table 1. The input polynomial is $a(x) = x^4 \oplus x \oplus 1$.

Table 1.

Clock	Input sequence	Binary cell states	Output sequence
	a_k x^k	C_0 C_1 C_2	b_k x^k
0	0 -	0 0 0	0 -
1	1 x^4		x^7
2	0 x^3		x^6
3	0 x^2		x^5
4	1 x^1		x^4
5	1 x^0		x^3
6	0 -		x^2
7	0 -		x^1
8	0 -		x^0

Check the obtained result by performing the multiplication of the polynomials by hand. The multiplication rules are the usual ones, except that summing the coefficients for the same power of *x* is done modulo-2 (XOR).

3.3. Draw the schematic of a division circuit based on the polynomial $g(x) = x^3 \oplus x^2 \oplus 1$ (using the model in Fig.5), after identifying the values of the

polynomial coefficients $g_i, i = \overline{0,3}$.

3.4. Write the functioning equations of the circuit, based on the functioning equation of a D flip-flop, and fill Table 2. The input polynomial is $a(x) = x^7 \oplus x^5 \oplus x^3 \oplus x^2 \oplus x \oplus 1$. Filling the table is done in the same order as in exercise **3.2.**

Check the obtained result by performing the division of the polynomials by hand.

Table 2

Clock	Input sequence	Binary cell states	Output sequence
	a_k x^k	C_0 C_1 C_2	b_k x^k
0	0 -	0 0 0	0 -
1	1 x^7		-
2	0 x^6		-
3	1 x^5		-
4	0 x^4		x^4
5	1 x^3		x^3
6	1 x^2		x^2
7	1 x^1		x^1
8	1 x^0		x^0

Remark: All the summations are done modulo-2.

3.5. Repeat exercises 3.1 and 3.2 for the multiplication circuit based on Fig. 3.

3.6. Repeat exercises 3.3 and 3.4 for the division circuit based on Fig. 4.

3.7. MATLAB -> Simulink Application:

Launch the *Matlab* application, and from the 'File->Open' menu select and open the model corresponding to the current laboratory. Check the results obtained in tables 1 and 2 (as well as the ones for exercises 3.5 and 3.6) in the following way:

- Identify the blocks in the schematic;

- With a double-click on the "Rd wksp" blocks, change the input sequence for the multiplication//division circuits, representing the coefficients of the polynomials from the previous exercises;

- Start the simulation by running 'Simulation -> Start';

- Observe the output waveforms on the oscilloscopes ("Scope") and deduce the output sequence of the circuit, and therefore the resulting polynomial. For division, also

check the remainder polynomial;

- Check the functioning of the division circuit which allows finding out the remainder (based on the model in Fig. 5) for the input polynomial $a(x) = x^7 \oplus x^6 \oplus x^5 \oplus x^3 \oplus x^2 \oplus x \oplus 1$ (the coefficients of the remainder polynomial are stored in the circuit cells at clock time $n+2=9$, i.e. after applying to the input the last coefficient of the input polynomial).