Chapter 12
PROBLEMS

1. [E, SPICE, 12.2.1] Use SPICE to compute the access time of the 512 · 512 NOR ROM of Example 12.4. **Use a simplified model** (i.e., do not include all the transistors but model their impact on word and bit lines). Compare the obtained results (row, column, and overall delay) with the results of the hand analysis.

2. [E, None, 12.2.3] For a memory containing a 4096 word · 2048 bit array of SRAM cells with a differential bit-line architecture, assume that the dynamic power consumption is dominated by charging and discharging the bit lines. Assume further that the cells are tiled at a vertical pitch of 5 μm and a horizontal pitch of 3 μm. Also assume that each cell adds a load of 3 fF to *BL* and *BL'*. Bit lines are in metal1 and are 0.6 μm wide.
   a. Compute the capacitance loading each bit line. Break it down into contributions from wiring and from memory cells.
   b. If the bit lines are precharged to 1.25 V and are allowed to develop a maximum differential voltage of 1 V (symmetric around the precharge voltage) during a read operation, what is the power consumption by the memory while reading at an access rate of 5 MHz.

3. [E, None, 12.2.3] Using the result of Eq. (12.3) and the device parameters of Table 3-2, construct a plot of $\Delta V/V_{Tn}$ vs. V_{DD} for an SRAM with a cell ratio of 1. Discuss the effect of supply voltage scaling on read upset malfunction.

4. [M, None, 12.2.3] Consider the six-transistor NMOS static memory cell of Figure 12.85 . You may ignore the body effect for this problem ($\gamma = 0$). Use $(W/L)_2 = 1.2/24$ and $(W/L)_3 = 2.4/1.2$. The threshold voltage V_{TO} of the depletion transistors equals –2 V. Assume Vdsat > Vdd (long channel device).
   a. Assume first that node *Q* is in the 1 state and node *Q* is 0. In order to write a 0 to node *Q*, bit line *BL* is lowered to 0.9 V. Determine the minimal size of transistor M_1 so that the cell just flips when this voltage is reached. Assume that the switching threshold V_M of the NMOS inverter equals 0.92 V.
   b. Assume now that $(W/L)_1 = 2.4/1.2$. Determine the maximal precharge voltage on bit line *BL* so that the cell does not flip during a read operation.
   c. Finally, suppose that the bit line has been precharged to 2 V and that the sense amplifier can detect a voltage swing of 0.5 V. Determine how long the read operation would take, given that the bit-line capacitance is 2 pF and the delay of the sense amp itself may be ignored. You may ignore the current through the depletion load M_2 for this part of the problem.

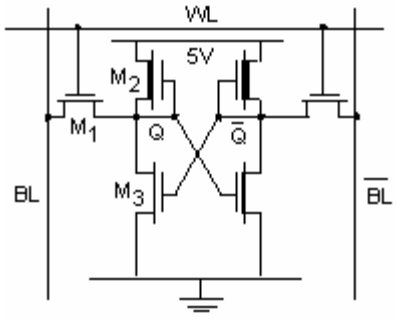

Figure 12.85 6T SRAM cell with NMOS depletion loads.

5. [E, None, 12.2.3] Draw the transistor diagram of a two-port SRAM cell. A two-port memory can read or write two independent addresses simultaneously. Discuss qualitatively how this effects the transistor sizing in the cell.

6. [M, None, 12.2.3] A two-transistor memory cell is shown in Figure 12.87. It uses two identical transistors (M_1 and M_2) with $W/L = 1.8/1.2$. Separate lines are provided for the read select (*RS*) and write select (*WS*), which both switch between 0 and 3 V. You may ignore body effect ($\gamma = 0$), channel-length modulation ($\lambda = 0$), and short-channel effects (Vdsat > Vdd) throughout this problem. Use kn' = 19.6uA/V^2, Vtn = 0.743V, kp' = 5.4uA/V^2, Vtp = -0.739V.

a. Explain the operation of the memory. Draw waveforms for *WB*, *RB*, *WS*, and *RS* for both reads and writes.

b. Determine the maximum possible current flowing into the cell during a read operation. State clearly your assumptions and simplifications.

c. Determine the size (*W*/*L*) of transistor M_3 so that the voltage on the bit line *RB* never drops below 2.5 V during a read operation.

d. Compute the time it takes to achieve a 0.5 V voltage drop on the bit line during a read operation. Assume that C_c = 50 fF and C_b = 2 pF.

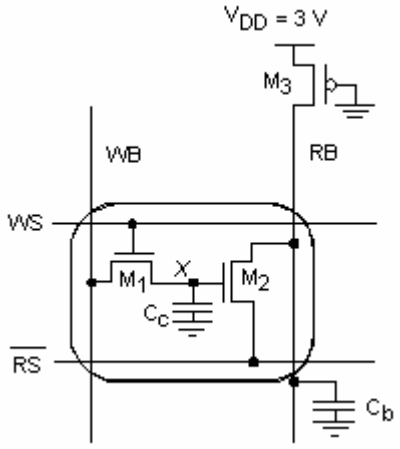

Figure 12.87 2-T memory cell.

7. [C, None, 12.2.3] Figure 12.88 shows a variant of the 1T-DRAM cell.

a. Fill in the timing diagrams for nodes *BL* and *Y* when writing a 0 and a 1 into the cell. For *WL* and *PL*, use the timing waveforms shown in the figure. Denote the voltage levels in terms of V_{DD} and V_T (ignore body effect). Ignore transient effects.

b. Describe briefly why this is an attractive approach.

c. Assume that the bit-line capacitance equals 75 fF. The transistor threshold equals 0.4 V (ignore body effect). The supply voltage equals 3 V and the bit line is pre(dis)charged to 0 V. Derive the symbolic equations needed to the derive the bit line voltages after reading a 0 and a 1. Ignore transient effects.

d. Using the results from 10c, derive the minimum cell capacitance so that the voltage difference on the bit line between reading a 0 and a 1 is larger than 150 mV.

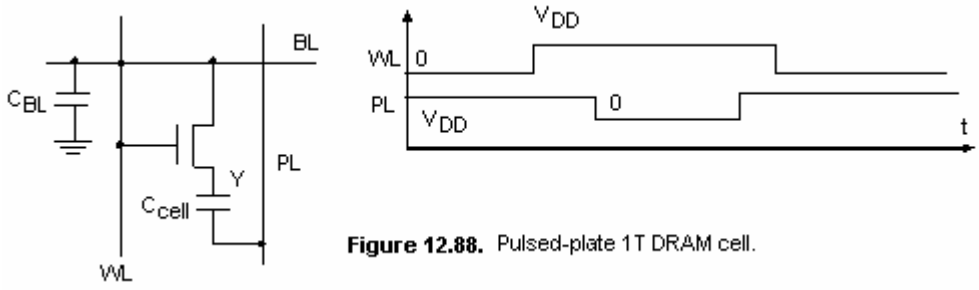

Figure 12.88. Pulsed-plate 1T DRAM cell.

8. [M, None, 12.3.2] Figure 12.89 shows a DRAM with a divided bit line. Each side of the differential sense amplifier connects to 256 DRAM cells and 1 dummy cell. The input capacitance of the sense amp is 8 fF at each input. The *BL* and *BL* lines are in metal for which the resistive and capacitive contributions can be neglected. The lumped junction capacitance of each cell is 0.8 fF. Ignore body effect.

a. Compute the effective capacitance on each bit line, C_{bit}.

b. Draw the timing diagrams corresponding to reading a 0 and a 1 from cell 1. Draw the waveforms for ϕ_p, ϕ_r, ϕ_d, ϕ_r, ϕ_d, *BL* and *BL*. Assume the sense amplifier refreshes values after reading them. Discuss the sizing of the capacitor C_d.

c. Compute the minimum values of C_c and C_d so that the sense amp sees a differential voltage of at least 60 mV.

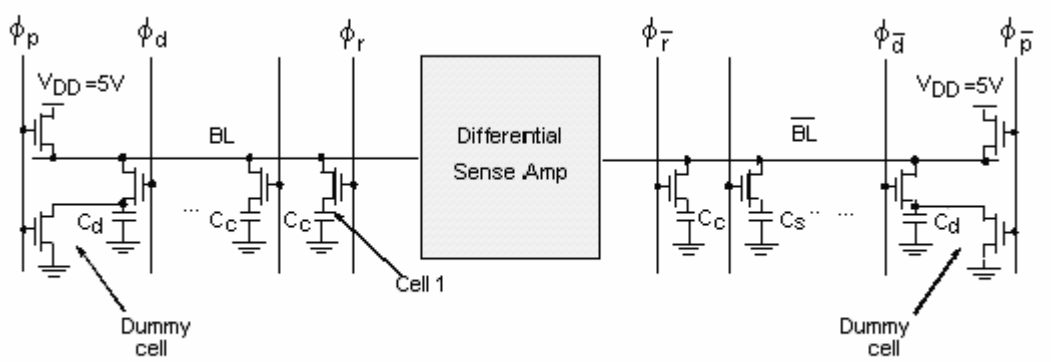

Figure 12.89 DRAM with divided bit-line structure.

9. [M, None, 12.3.1] Figure 12.90 shows a dynamic NOR row decoder (using pseudo two-phase logic) for word line 0 of a memory with 16 word lines.
   a. Explain the operation of this row decoder, showing approximate voltage waveforms for all important nodes, including the clocks. What is the purpose of gate 2?
   b. Discuss the relative advantages and disadvantages of a dynamic versus a static decoder.

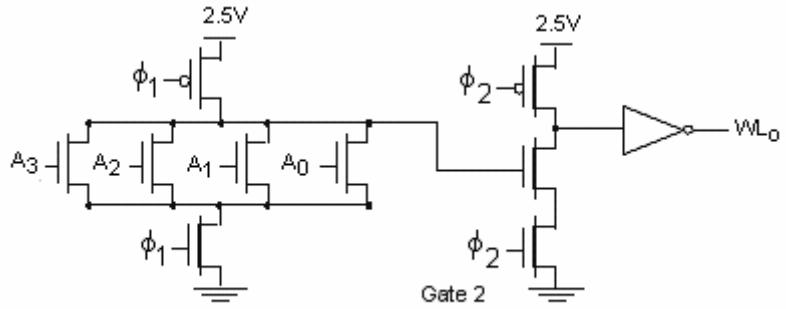

Figure 12.90 Dynamic NOR row-decoder.

10. [E, None, 12.3.1] Design a column decoder to select one out of 16 bit lines based on address bits A_3, A_2, A_1, and A_0 and their complements. Minimize the total number of transistors while limiting the maximum number of cascaded pass transistors to three. Draw a transistor-level schematic of your design.
11. [C, None, 12.3.2] A dynamic sense amplifier is shown in a Figure 12.91. The capacitance of each bit line is 1 pF, and average discharging current from the selected RAM cell equals 10 μA. The waveform applied at point *S* is shown in b. Initially, *S* is high. When *BL* reaches V_{DD} – 0.5 V (at time $t = t_1$), *S* is lowered to V_{DD} – 1.2 V and reaches this value at time $t = t_2 = t_1 + 1$ nsec. Determine the sizes of the various transistors M_1 and M_2 so that a delay of less than 3 nsec is obtained. Delay is measured starting at t_1 and is defined as the time when *BL* reaches 2.1 V. V_{DD} = 3.3 V, Vt=0.75V, kn'=19.6uA/V^2 (assume long channel). Complete the waveform for *BL*.

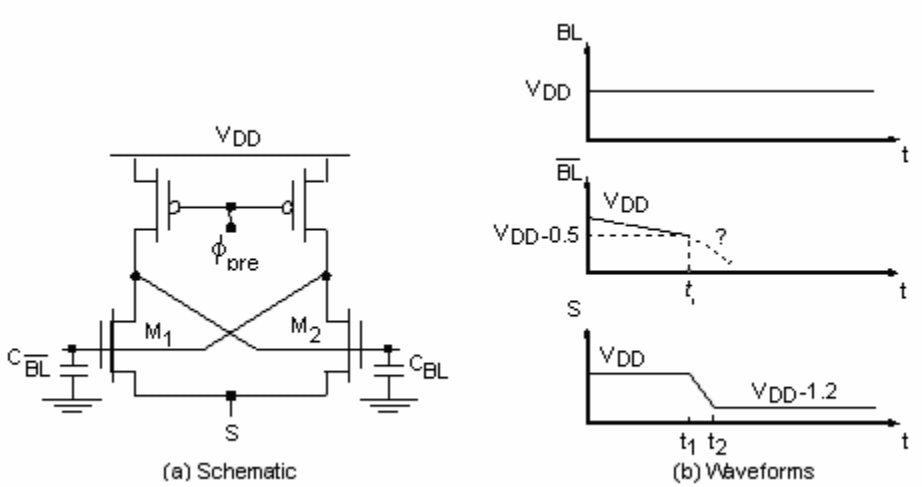

Figure 12.91 Dynamic sense amplifier.

12. [E&D, None, 12.4.2] Design a hamming-code scheme to correct a single bit in an 11-bit word. How many check-bits are needed? Design the logic needed to perform the error correction (at the gate level). It is sufficient to show the logic for a single bit.
13. [E, None, 12.6.1] Implement the following logic functions described by Eq. 12.20 using a dynamic NAND-NAND PLA. Draw the transistor diagram.

$$f_0 = x_0 x_1 + \overline{x_2} \tag{12.20}$$

$$f_1 = x_0 x_1 x_2 + \overline{x_2} + \overline{x_0}\, x_1$$

DESIGN PROBLEM

Design an SRAM array with 64 rows with each row being 32-bits wide. Use standard, minimum channel length, 6T SRAM cells with a pull-up ratio of 1 and a cell ratio of 1.2. Estimate the size of the cell. Assuming the minimum width wires with 0.1fF/μm capacitance and 0.05Ω/□ resistance, estimate the bit line and word line capacitances. Design a 6-to-64 decoder in complementary CMOS to drive this wordline load and assuming that the input capacitance is limited to a transistor width of 24λ. Input address bits are available as true and complementary. Divide the decoder in the predecoder and the final wordline decoder, and include the wire load between the two in your sizing calculation. Use dynamic bitline loads and dsign the dynamic sense amplifiers, loaded with 24λ loads. Use the 4:1 output multiplexers.