

东南大学电子科学与工程学院

实 验 报 告

课程名称： 集成电路CAD

实验名称： 四位加法器电路设计与模拟

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学 号： 06219109

实验地点： 东南大学无锡国际校区

实验时间： 2022-3-26

评定成绩：

审阅教师：

实验六 · 四位加法器电路设计与模拟

1 实验目的

- 复习全加器结构特点;
- 进一步掌握 T-SPICE 的操作;
- 掌握设计复杂电路方法及流程, 并会分析结果。

2 预习要求

- 复习 SPICE 语言, 复习前面学过的基本软件操作;
- 了解四位加法器的结构特点;
- 画出四位全加器电路图。

3 实验内容及步骤 (实验设计指标)

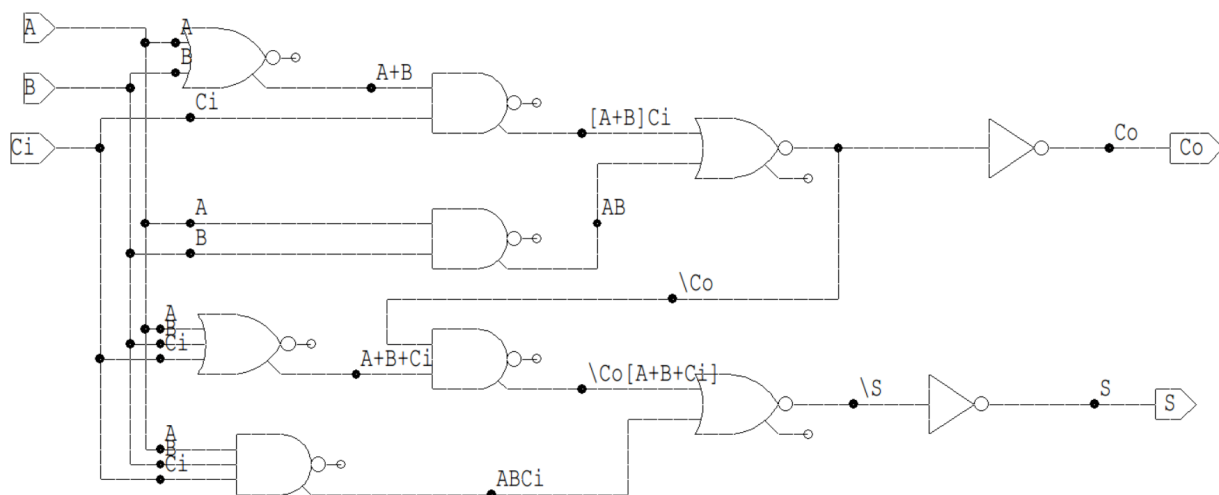
- 设计全加器电路以及符号;
- 设计四位全加器电路;
- 输出 SPICE 文件, 并仿真;
- 分析仿真结果, 验证电路的正确性。

4 设计过程

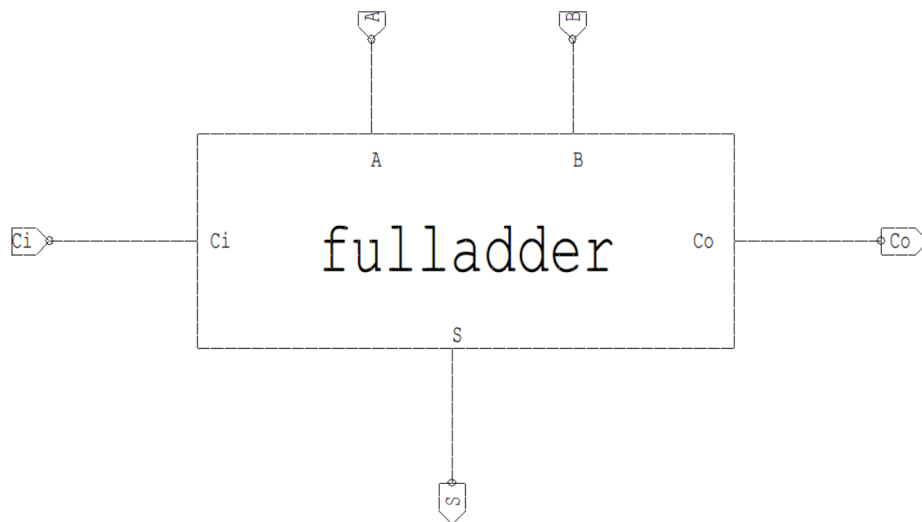
4.1 Full Adder

Full Adder 我们在数电中就已经学过, 我们可以利用一些门电路设计出, 如下图所示:

电路:

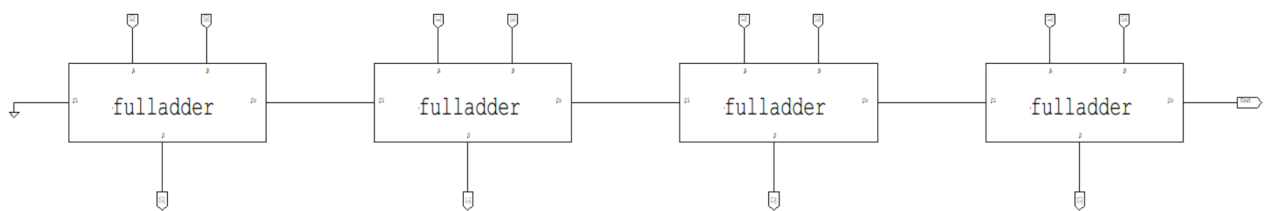


符号如下:

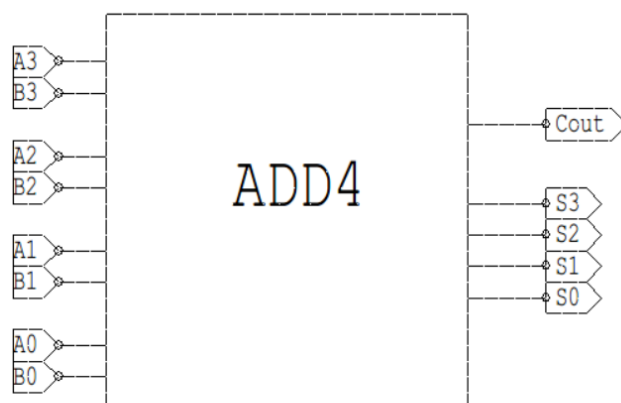


4.2 ADD4

对四位加法器来说，就是调用四个 Full Adder 进行级联。



符号如下图：



4.3 T-SPICE Simulation

输出 SPICE 文件如图

```
T-Spice - [adder.sp]
File Edit View Simulation Table Options Window Help

M1 Out1 A Vdd Vdd PMOS W='28*1' L='2*1' AS='84*1*1' AD='122*1*1' PS='34*1' PD='47*1' M=1
M2 Out1 B Vdd Vdd PMOS W='28*1' L='2*1' AS='84*1*1' AD='84*1*1' PS='34*1' PD='34*1' M=1
M3 Out1 C Vdd Vdd PMOS W='28*1' L='2*1' AS='148*1*1' AD='84*1*1' PS='68*1' PD='34*1' M=1
M7 Out2 Out1 Vdd Vdd PMOS W='28*1' L='2*1' AS='122*1*1' AD='148*1*1' PS='47*1' PD='68*1' M=1
.ENDS

.SUBCKT NOR3C A B C Out1 Out2 Gnd Vdd
M4 Out1 A Gnd Gnd NMOS W='28*1' L='2*1' AS='84*1*1' AD='122*1*1' PS='34*1' PD='47*1' M=1
M5 Out1 B Gnd Gnd NMOS W='28*1' L='2*1' AS='84*1*1' AD='84*1*1' PS='34*1' PD='34*1' M=1
M6 Out1 C Gnd Gnd NMOS W='28*1' L='2*1' AS='148*1*1' AD='84*1*1' PS='68*1' PD='34*1' M=1
M8 Out2 Out1 Gnd Gnd NMOS W='28*1' L='2*1' AS='122*1*1' AD='148*1*1' PS='47*1' PD='68*1' M=1
M1 1 A Vdd Vdd PMOS W='28*1' L='2*1' AS='84*1*1' AD='122*1*1' PS='34*1' PD='47*1' M=1
M2 2 B 1 Vdd PMOS W='28*1' L='2*1' AS='84*1*1' AD='84*1*1' PS='34*1' PD='34*1' M=1
M3 Out1 C 2 Vdd PMOS W='28*1' L='2*1' AS='148*1*1' AD='84*1*1' PS='68*1' PD='34*1' M=1
M7 Out2 Out1 Vdd Vdd PMOS W='28*1' L='2*1' AS='122*1*1' AD='148*1*1' PS='47*1' PD='68*1' M=1
.ENDS

.SUBCKT Module0 A B Ci Co S Gnd Vdd
XInv_1 \Co Co Gnd Vdd Inv
XInv_2 \S S Gnd Vdd Inv
XNAND2C_1 A+B Ci N6 [A+B]Ci Gnd Vdd NAND2C
XNAND2C_2 A B N16 AB Gnd Vdd NAND2C
XNAND2C_3 \Co A+B+Ci Gnd0 \Co[A+B+Ci] Gnd Vdd NAND2C
XNAND3C_1 A B Ci N30 ABCi Gnd Vdd NAND3C
XNOR2C_1 A B N10 A+B Gnd Vdd NOR2C
XNOR2C_2 [A+B]Ci AB \Co N1 Gnd Vdd NOR2C
XNOR2C_3 \Co[A+B+Ci] ABCi \S Gnd5 Gnd Vdd NOR2C
XNOR3C_1 A B Ci N35 A+B+Ci Gnd Vdd NOR3C
.ENDS

* Main circuit: adder
XModule0_1 A0 B0 Gnd N5 S0 Gnd Vdd Module0
XModule0_2 A1 B1 N5 N9 S1 Gnd Vdd Module0
XModule0_3 A2 B2 N9 N13 S2 Gnd Vdd Module0
XModule0_4 A3 B3 N13 Cout S3 Gnd Vdd Module0
* End of main circuit: adder
```

对电源进行设置之后，利用 T-SPICE 进行仿真，仿真状态结果如下图：

T-Spice - [Simulation Status]

File Edit View Simulation Table Options Window Help

Input fil adder.sp Output adder.out

Progres: Simulation completed
Time = 200.000000ns 100%

Total	122	Active	224	Independent	3
Total	227	Passive	0	Controlled	0

MOSFETs - 224	MOSFET geometries - 20
BJTs - 0	JFETs - 0
MESFETs - 0	Diodes - 0
Capacitors - 0	Resistors - 0
Inductors - 0	Mutual inductors - 0
Transmission lines - 0	Coupled transmission lines - 0
Voltage sources - 3	Current sources - 0
VCVS - 0	VCCS - 0
CCVS - 0	CCCS - 0
V-control switch - 0	I-control switch - 0
Macro devices - 0	Functional model instances - 0
Subcircuits - 6	Subcircuit instances - 44
Independent nodes - 112	Boundary nodes - 10
Total nodes - 122	

Warning T-SPICE : The vrange voltage range limit (5.5) for diode tables has been exceeded.
Warning T-SPICE : The vrange voltage range limit (5.5) for MOSFET tables has been exceeded.
Warning T-SPICE : The vrange voltage range limit should be set to
at least 5.53624 for best accuracy and performance.

Parsing	0.00 seconds
Setup	0.02 seconds
DC operating point	0.24 seconds
Transient Analysis	0.60 seconds

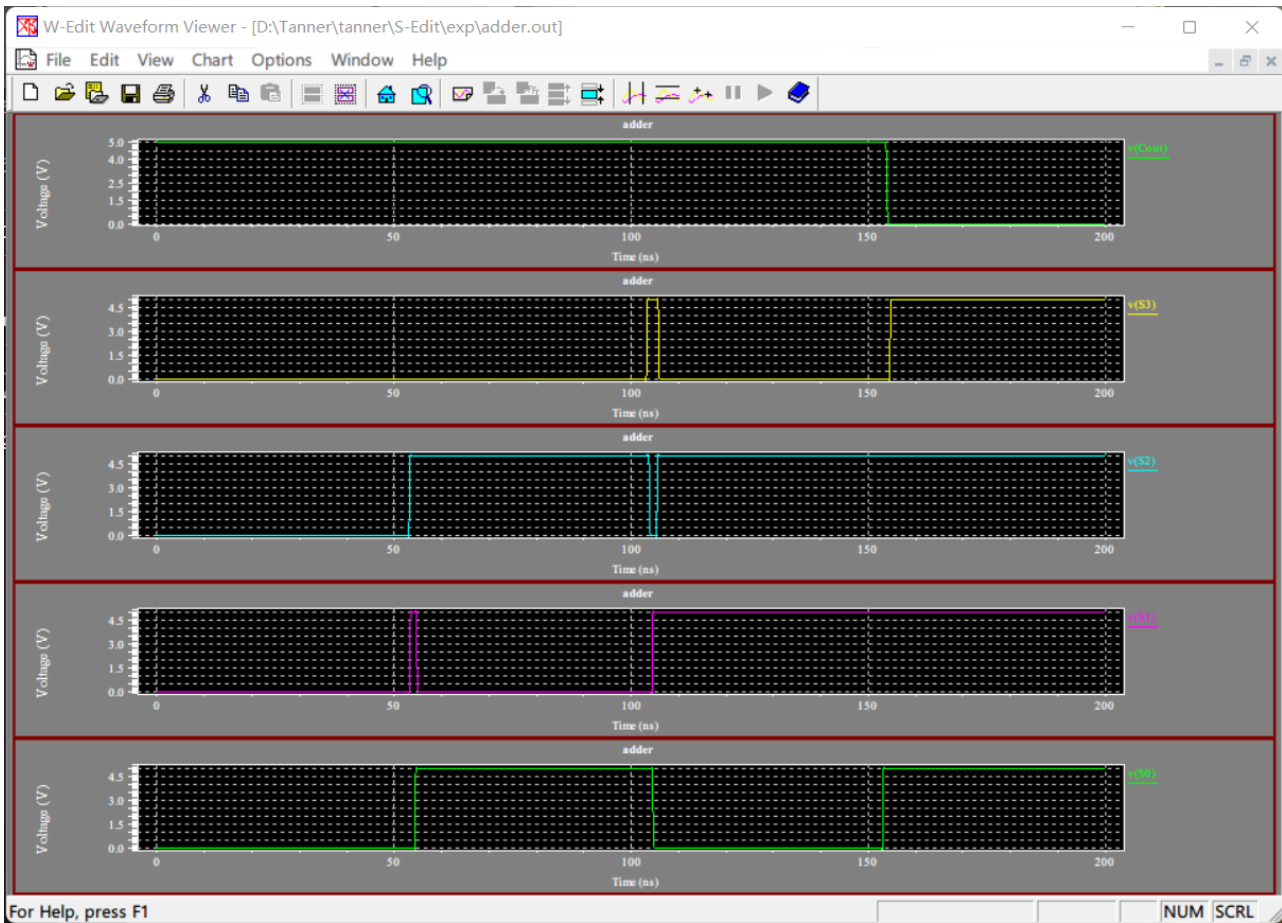
Total	0.86 seconds

我们还可以用 W-Edit 来观察实验结果。

```

1 .include "D:\Tanner\tanner\TSpice70\models\m12_125.md"
2 .param l=0.5u
3 vvdd Vdd GND 5
4 .vector A {A3 A2 A1 A0}
5 .vector B {B3 B2 B1 B0}
6 va A GND BUS ({0011 1110 1100 1010}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
7 va B GND BUS ({1101 0111 1010 0101}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
8 .tran/op 1n 200n method=bdf
9 .print tran v(S0) v(S1) v(S2) v(Cout)

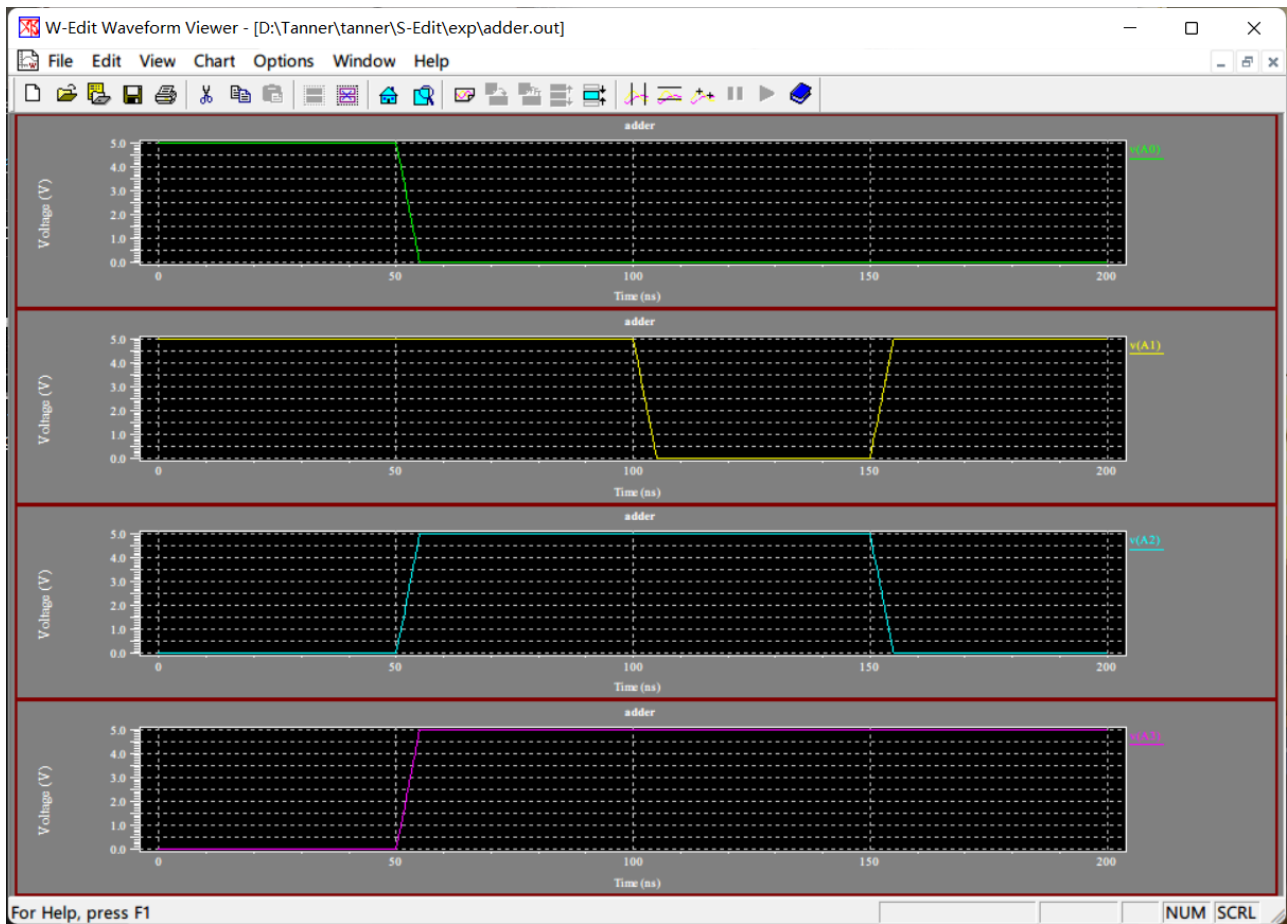
```



```

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6 va A GND BUS ({0011 1110 1100 1010}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
7 va B GND BUS ({1101 0111 1010 0101}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
8 .tran/op 1n 200n method=bdf
9 .print tran v(A3) v(A2) v(A1) v(A0)

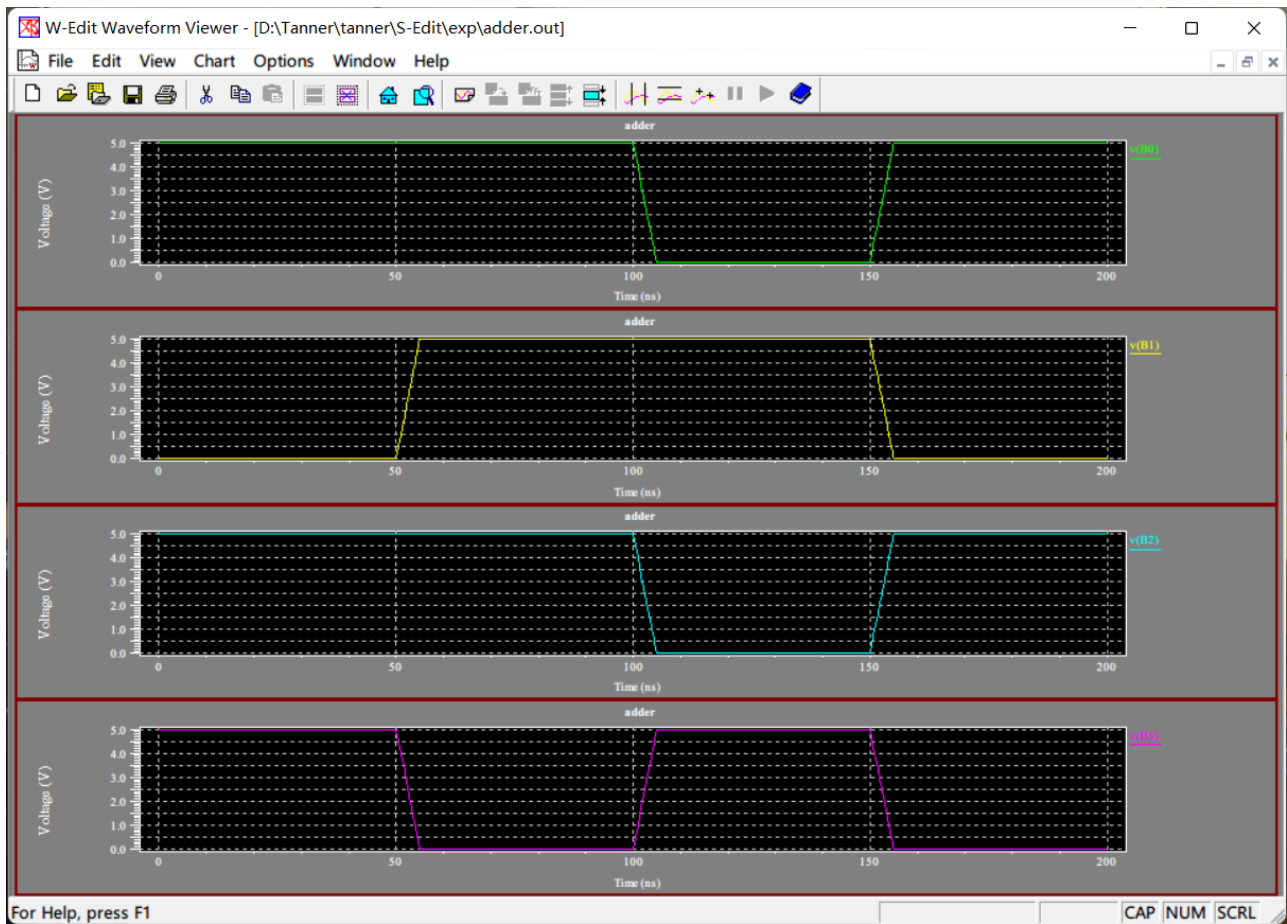
```



```

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6 va A GND BUS ({0011 1110 1100 1010}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
7 vb B GND BUS ({1101 0111 1010 0101}) lt=50n ht=50n on=5 off=0 rt=5n ft=5n)
8 .tran/op 1n 200n method=bdf
9 .print tran v(B3) v(B2) v(B1) v(B0)

```



5 实验过程中出现的问题和体会

- 学会了处理名称冲突的模块解决方式
- 学会了直接调用一些已有的模块，比如 INV，NAND3，NOR3 等