Unsupervised spiking neural networks with analog memristive devices for edge computing

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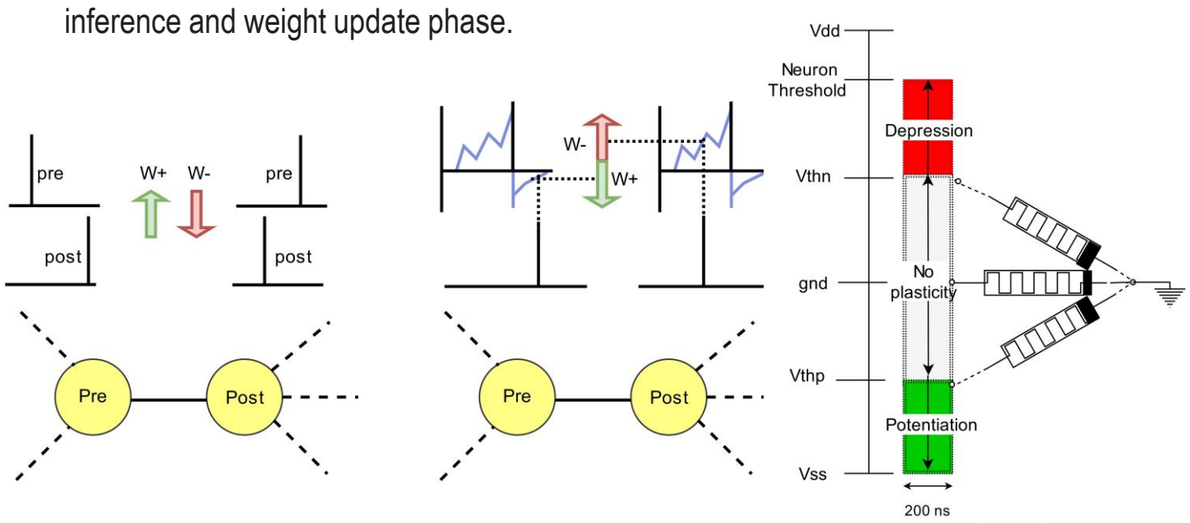
ABSTRACT

- The **UNICO** (Unsupervised spiking neural networks with analog memristive devices for edge computing) chip is a 130nm, 6mm*6mm **ASIC** intended for BEOL integration of memristors.
- **Objective**: To demonstrate on-chip learning on a CMOS-RRAM integrated SNN building block architecture and evaluate the device characteristics of 1T1R OxRAM [1] and FeRAM memory arrays.
- **Differentiating factor**: Implementation of on-chip synaptic plasticity using Voltage dependent synaptic plasticity (**VDSP**) [2] based analog conductance programming. Amplification block and digital control architecture is proposed to switch between inference and weight update phase.



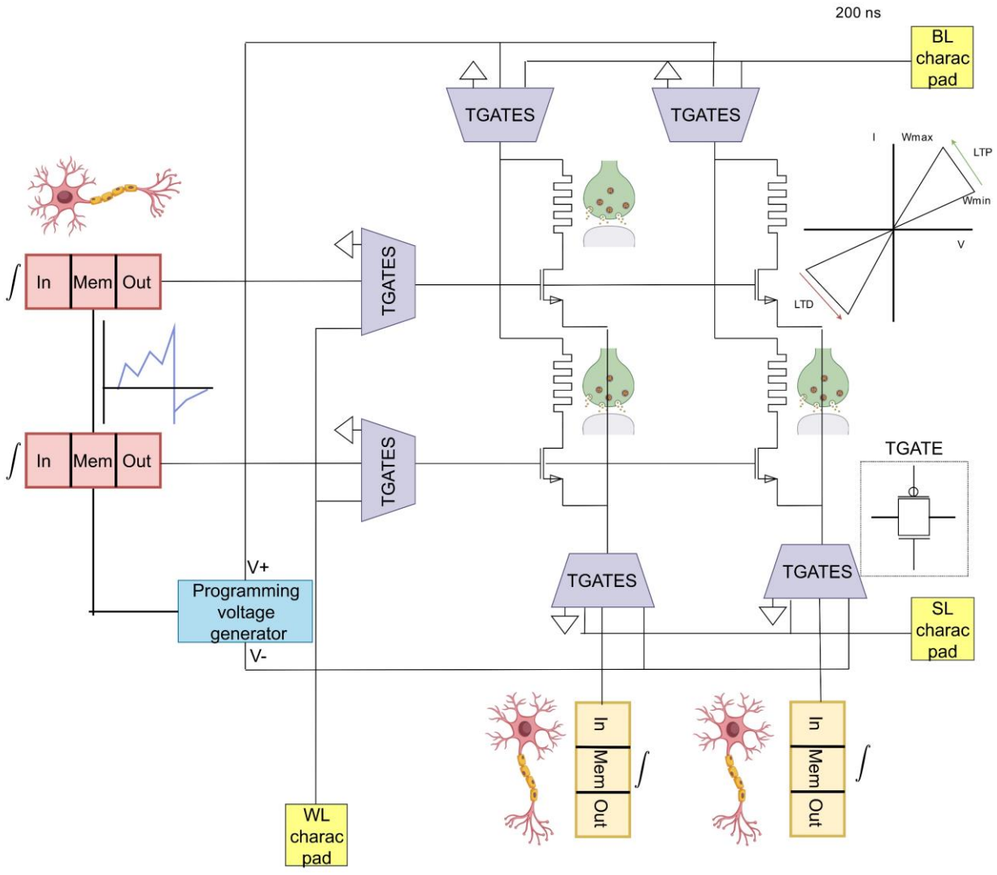


Fig. 1: VDSP and Simplified schematic representation of Neural Building block of size 2x2

Neural Building Block (NBB)

- 32 neurons and 256 synapses.
- Biological spiking neuron model.
- Leaky integrate and fire (**LIF**) neuron with **CMOS** transistors.
- **1T1R BEOL** integrated non-volatile memories with **multiple programable states**.
- Digitally programmable **lateral inhibition**
- Neuron **activity modulation** for classification layer

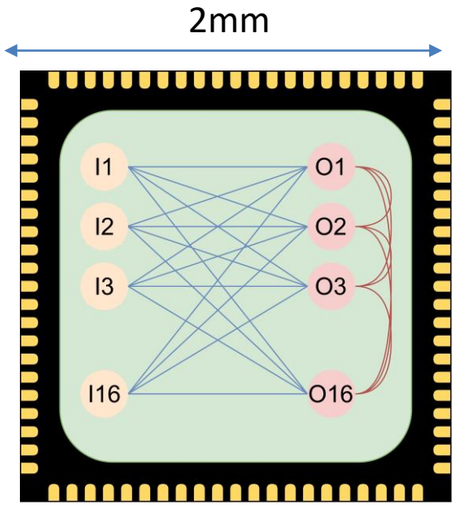


Fig. 2: CMOS chip with Neural building block with 84 IO pads.

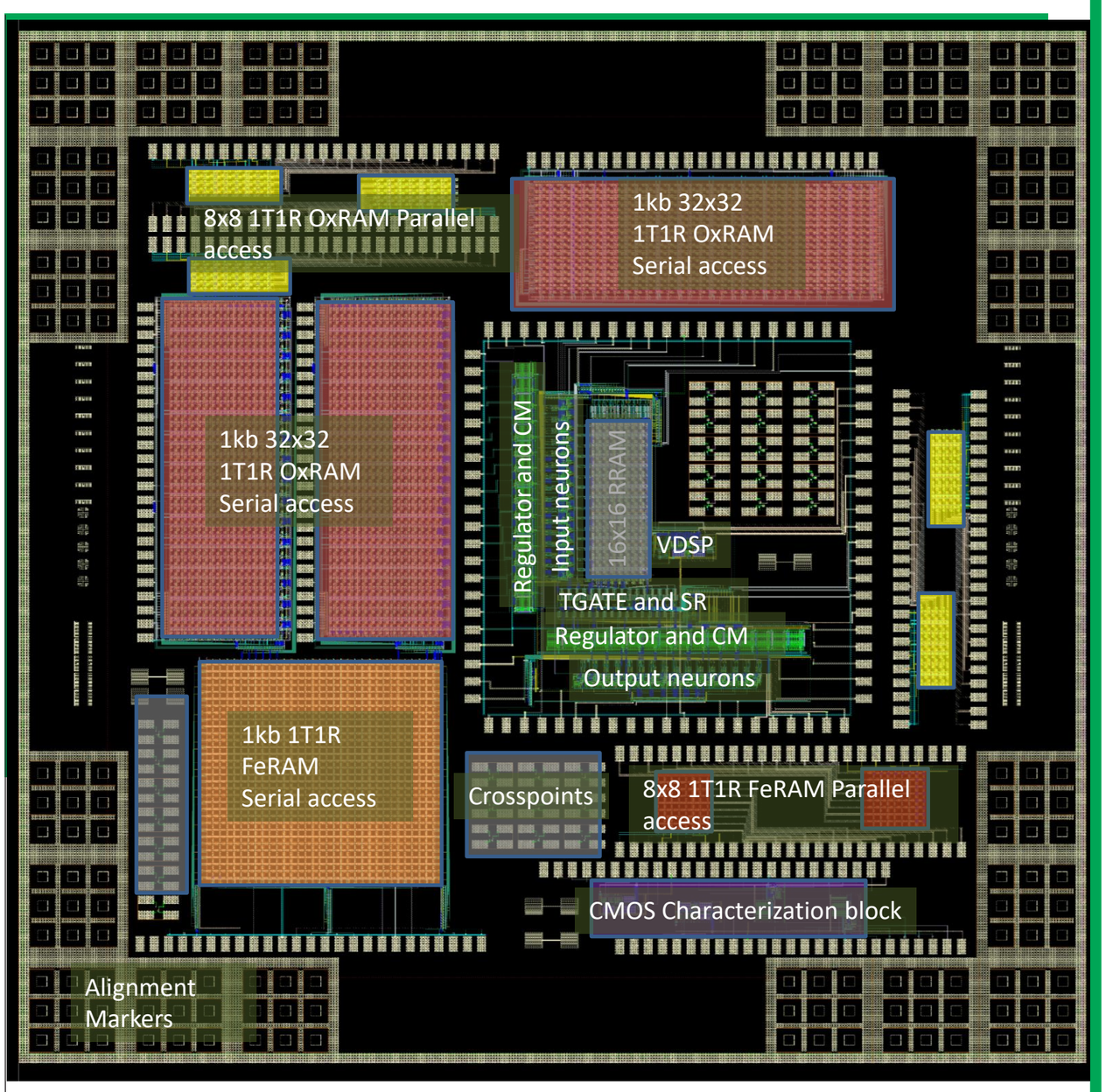


Fig. 3: Top view of CMOS chip with NBB, RRAM and CMOS characterization cells

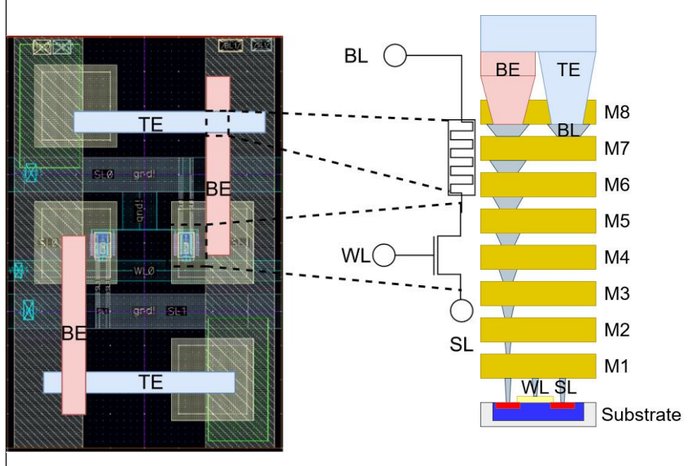


Figure 4: Layout view of two 1T1R cells and Cross-sectional view of one 1T1R cell on chip

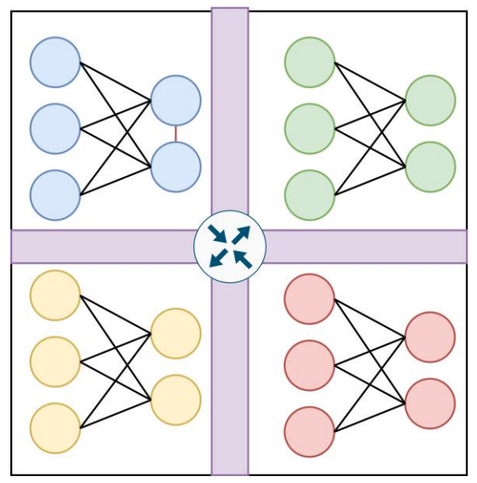


Figure 5: Neural building block approach

CONCLUSION & FUTURE WORK

- An integrated circuit for implementation of SNN with VDSP driven on-chip plasticity on an RRAM-based synaptic array was designed.
- LIF neuron, VDSP programming block, memory reading and inference circuit blocks were verified with extensive mixed-signal simulations and process mismatch analysis.
- CMC/TSMC will fabricate the chip on 130nm CMOS node, and RRAM will be integrated at 3IT, Sherbrooke and IBM, Zurich.
- Characterization of neural building blocks would validate the proposed concept of on-chip learning and estimation of system-level energy consumption of different neural operations for efficient algorithm design.
- Characterization of 1kb arrays of FeRAM and OxRAM would be used for behavioral modelling of voltage-driven current-controlled switching in 1T1R devices and enable conception and design of advanced CMOS-RRAM NBB architecture.

REFERENCES

1. El Mesoudy, Abdelouadoud, et al. "Fully CMOS-compatible passive TiO2-based memristor crossbars for in-memory computing." Microelectronic Engineering (2022): 111706.
2. Garg, Nikhil, et al. "Voltage-Dependent Synaptic Plasticity (VDSP): Unsupervised probabilistic Hebbian plasticity rule based on neurons membrane potential." arXiv preprint arXiv:2203.11022 (2022).