PUNE INSTITUTE OF COMPUTER TECHNOLOGY
DHANKAWADI, PUNE – 43.
Department of Computer Engineering
Academic Year: 2019-20 (Semester-I)
UNIT TEST II
Year: S.E.
Subject: Digital Electronics & Logic Design

Time: - 1 Hour Max. Marks: - 30

Instructions to the candidates:-

- All Questions are compulsory.

Q. No	Sub. Q. No.	Question	Marks	Unit No.	COs Covered	CO Mapping
1	**A**	Draw and explain 3 bit Asynchronous UP counter using MS-JK flip-flop, also draw timing diagram for the same	06	2	CO1 CO2	H H
	B	Compare Moore and mealy model by using example	04	2	CO1 CO2 CO3	H H H
2	**A**	Write VHDL code for full adder using data flow modeling style.	06	3	CO3	H
	B	Draw ASM chart for sequence detector which detects the pattern 010 using mealy model. (Consider overlapping)	04	3	CO2	H
3	**A**	A combinational Circuit is defined by the following $F1(A,B,C) = m \Sigma (0,1,3,7)$ $F2(A,B,C) = m \Sigma (1,2,5,6)$ Implement this circuit with PLA.	06	4	CO1 CO2	M H
	B	A combinational circuit is defined by the function $F1 = m(0,1,3,4)$ Implement this circuit with PAL.	04	4	CO1 CO2	M H

*****ALL THE BEST*****