

August 1986 Revised March 2000

DM74LS90 Decade and Binary Counters

General Description

Each of these monolithic counters contains four masterslave flip-flops and additional gating to provide a divide-bytwo counter and a three-stage binary counter for which the count cycle length is divide-by-five for the DM74LS90.

All of these counters have a gated zero reset and the DM74LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the DM74LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

Features

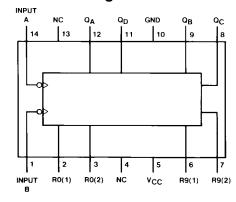
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Ordering Code:

Order Number	Package Number	Package Description
DM74LS90M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS90N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Reset/Count Truth Table

	Reset Inputs				Out	put		
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q _C	Q _B	Q_A	
Н	Н	L	Х	L	L	L	L	
Н	Н	Χ	L	L	L	L	L	
Х	X	Н	Н	Н	L	L	Н	
Х	L	Χ	L	COUNT				
L	X	L	X	COUNT				
L	X	X	L	COUNT				
Χ	L	L	Χ	COUNT				

Function Tables

BCD Count Sequence (Note 1)

Count	Output						
	Q_D	Q _C	Q _B	Q_A			
0	L	L	L	L			
1	L	L	L	Н			
2	L	L	Н	L			
3	L	L	Н	Н			
4	L	Н	L	L			
5	L	Н	L	Н			
6	L	Н	Н	L			
7	L	Н	Н	Н			
8	Н	L	L	L			
9	Н	L	L	Н			

Bi-Quinary (5-2) (Note 2)

Count	Output						
	Q _A	Q _D	Q _C	Q _B			
0	L	L	L	L			
1	L	L	L	Н			
2	L	L	Н	L			
3	L	L	Н	Н			
4	L	Н	L	L			
5	Н	L	L	L			
6	Н	L	L	Н			
7	Н	L	Н	L			
8	Н	L	Н	Н			
9	Н	Н	L	L			

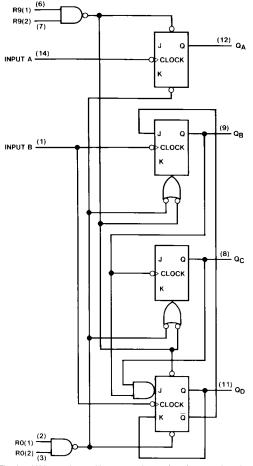
H = HIGH Level L = LOW Level X = Don't Care

Note 1: Output $\mathbf{Q}_{\mathbf{A}}$ is connected to input B for BCD count.

Note 2: Output $\mathbf{Q}_{\mathbf{D}}$ is connected to input A for bi-quinary count.

Note 3: Output $\mathbf{Q}_{\mathbf{A}}$ is connected to input \mathbf{B} .

Logic Diagram



The J and K inputs shown without connection are for reference only and are functionally at a high level.

Absolute Maximum Ratings(Note 4)

Supply Voltage Input Voltage (Reset) 7V Input Voltage (A or B) Operating Free Air Temperature Range

Storage Temperature Range

Note 4: The "Absolute Maximum Ratings" are those values beyond which 7V the Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings.

The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	•	Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input Voltage				0.8	V
I _{OH}	HIGH Level Output Current				-0.4	mA
I _{OL}	LOW Level Output Current				8	mA
f _{CLK}	Clock Frequency (Note 5)	A to Q _A	0		32	MHz
		B to Q _B	0		16	
f _{CLK}	Clock Frequency (Note 6)	A to Q _A	0		20	MHz
		B to Q _B	0		10	
t _W	Pulse Width (Note 5)	A	15			
		В	30			ns
		Reset	15			
t _W	Pulse Width (Note 6)	Α	25			
		В	50			ns
		Reset	25			
t _{REL}	Reset Release Time (Note 5)		25			ns
t _{REL}	Reset Release Time (Note 6)		35			ns
T _A	Free Air Operating Temperature	e	0		70	°C

-65°C to +150°C

Note 5: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25$ °C and $V_{CC} = 5V$.

Note 6: C_L = 50 pF, R_L = 2 k $\Omega,~T_A$ = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Condition	s	Min	Typ (Note 7)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$		2.7	3.4		٧
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IL} = Max, V_{IH} = Min$ $I_{OL} = 4 \text{ mA}, V_{CC} = Min$	(Note 8)		0.35 0.25	0.5 0.4	٧
I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$ $V_{CC} = Max$	Reset A			0.1	mA
I _{IH}	HIGH Level Input Current	$V_{I} = 5.5V$ $V_{CC} = Max, V_{I} = 2.7V$	B Reset A			0.4 20 40	μА
	Impat ourient	B A				80	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$	Reset A			-0.4 -2.4	mA
		W M (N ())	В			-3.2	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 9)		-20	1	-100	mA
I _{CC}	Supply Current voicals are at $V_{CC} = 5V$. $T_A = 25^{\circ}C$.	V _{CC} = Max (Note 7)			9	15	mA

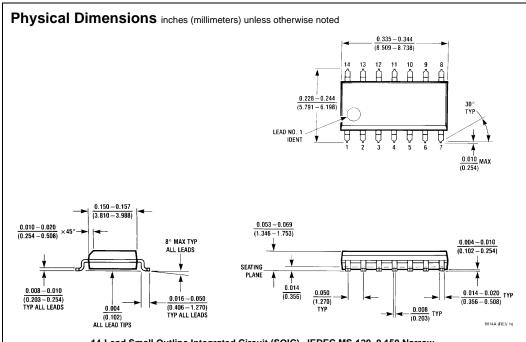
Note 7: All typicals are at $V_{CC} = 5V$, $T_A = 25$ °C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 10: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25 $^{\circ}C$

		From (Input)	$R_L = 2 k\Omega$				
Symbol	Parameter	To (Output)	C _L = 15 pF		C _L = 50 pF		Units
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock	A to Q _A	32		20		MHz
	Frequency	B to Q _B	16		10		IVITIZ
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A to Q _A		16		20	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A to Q _A		18		24	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	A to Q _D		48		52	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	A to Q _D		50		60	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	B to Q _B		16		23	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	B to Q _B		21		30	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	B to Q _C		32		37	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	B to Q _C		35		44	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	B to Q _D		32		36	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	B to Q _D		35		44	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	SET-9 to Q _A , Q _D		30		35	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	SET-9 to Q _B , Q _C		40		48	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	SET-0 to Any Q		40		52	ns



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 14 13 12 11 10 9 8 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

8.255 + 1.016

N144 (REV.F)

www.fairchildsemi.com

This datasheet has been downloaded from:

www. Data sheet Catalog.com

Datasheets for electronic components.