PUNE INSTITUTE OF COMPUTER TECHNOLOGY
DHANKAWADI, PUNE – 43.
Department of Computer Engineering
Academic Year: 2019-20 (Semester-I)
UNIT TEST I
Year: S.E.
Subject: Digital Electronics & Logic Design

Time: - 1 Hour Max. Marks: - 30

Instructions to the candidates:-

- All Questions are compulsory.
- Solve each Combinational logic design question by following Design procedures (Truth Table, K-map & Logic Diagram)

Q. No	Sub. Q. No.	Question	Marks	Unit No.	COs Covered	CO Mapping
1	A	Simplify the following logic function using K-Map $Y(A,B,C,D) = \Sigma m (0,1,2,3,5,7,8,9,11,14)$	06	1	CO1	H
	B	Design and explain 4 bit binary adder using IC7483.	04	1	CO2 CO3	H M
2	A	Design and Implement 3 bit Binary to Gray code converter using logic gate.	06	1	CO1 CO2	H H
	B	Implement Full Adder using 3:8 Decoder and draw the diagram?	04	1	CO2 CO3	H M
3	A	Implement the following function using single 4:1 mux. $F(A,B,C,D) = \Sigma m (0,2,3,6,8,9,12,14)$	06	1	CO1 CO2	M H
	B	Convert The following Flip-flop: (i) JK to T (ii) SR to D	04	2	CO1 CO2	M H

*****ALL THE BEST*****