

IIIT BANGALORE



VLS 502

Analog CMOS VLSI Design

Project Report

Submitted By:-

Arun Teja Reddy P. - MT2024507

Nikhil Bhusari - MT2024522

Shruti Chaturvedi - MT2024534

Submitted To:-

Prof. Sakshi Arora

Assistant Professor,

VLSI Lab,

International Institute of Information Technology - Bangalore

1. Specifications

In this project, we have designed a Low Dropout Regulator (LDO) considering various operating conditions. The design includes both externally compensated and internally compensated LDO configurations. The schematic shown below is specifically designed for the 45nm technology node. Our objective is to optimize the LDO design to perform effectively under both maximum and minimum load conditions.

Table 1: Specifications Summary

Specifications	Internally Compensated	Externally Compensated
V _{in}	1.4 V	1.4 V
V _{out}	1 V	1 V
PSRR	60dB	60dB
I _{load} —min	2mA	2mA
I _{load} —max	10mA	10mA
C _{load}	2nF	1uF
I _{quiescent}	50uA	50uA
Transient Duration	10us	10us

2. Purpose of an LDO

A Low Dropout Regulator (LDO) is a type of linear voltage regulator designed to maintain a constant output voltage, even when the input voltage is only slightly higher than the output voltage. The input to output differential voltage, at which the LDO fails to regulate the output is defined as the dropout voltage.

The purpose of an LDO is to ensure that electronic components get a steady voltage supply. This is especially important for sensitive devices like microprocessors, sensors, and communication modules that require a specific voltage to function correctly. LDOs also help reduce noise in the power supply, ensuring that connected devices receive clean power without interference, which is crucial in applications like audio systems or signal processing.

Key components of an LDO are :

1. Pass Transistor: The core component that controls the flow of current from the input to the output. It can be a P-channel MOSFET, N-channel MOSFET, or a bipolar transistor.
2. Error Amplifier: Compares the output voltage to a reference voltage and generates an error signal.
3. Reference Voltage (Vref): A stable and precise voltage, often generated using a bandgap reference circuit, used as a comparison standard.
4. Feedback Network: Senses the output voltage and feeds it back to the error amplifier for comparison.

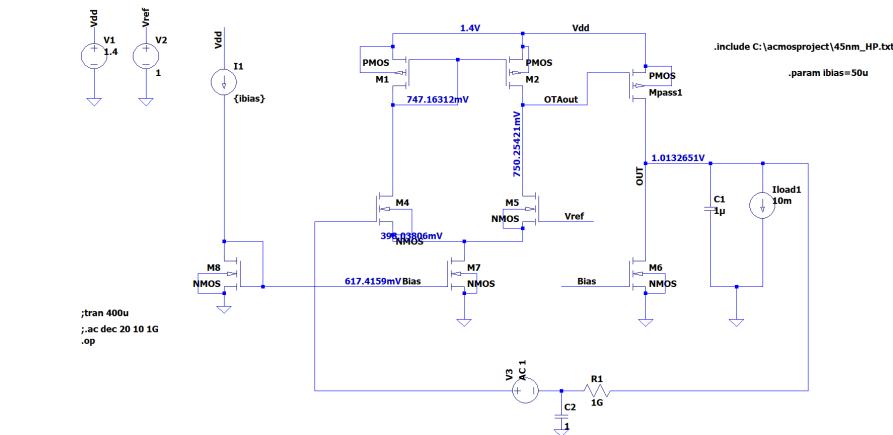


Figure 1: Our LDO schematic

3. Relevance of Techplots

The motivation for a gm/Id methodology stems from the fact that:

In deep submicron nodes the square law description of Id fails to describe device behaviour accurately, especially for short channel devices in strong inversion and also for both long and short channel devices operating in weak inversion.

In addition to this, gm is one of the most important parameters that determine device performance in terms of speed and noise.

- **Github Link:**
Technology node : 45 nm
- ft improves with shorter channel lengths
- gm/Id trade-offs highlight optimal bias points for achieving desired performance metrics
- Comparison of different FOMs at different lengths:

Table 2: Key Differences between FOMs at 180 nm and 45nm for NMOS

Length (nm)	gmro	Id/W	ft (GHz)
90	52.22	89.15	61.71
180	121.7	45.87	17.72

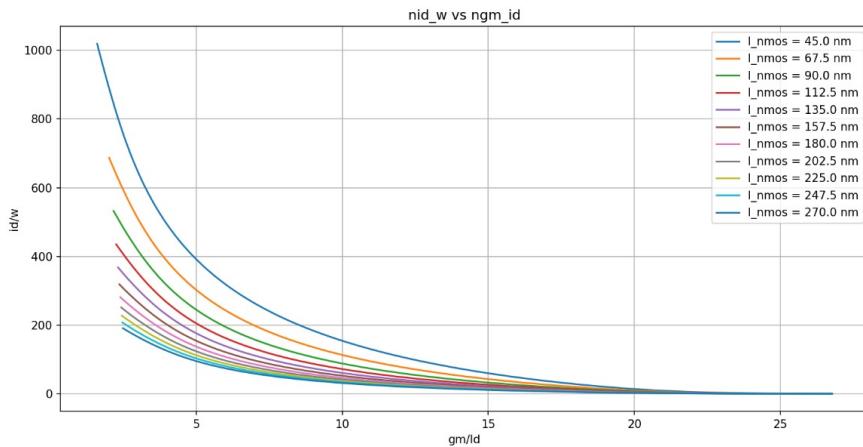


Figure 2: NMOS Techplots after Python postprocessing - Id/W

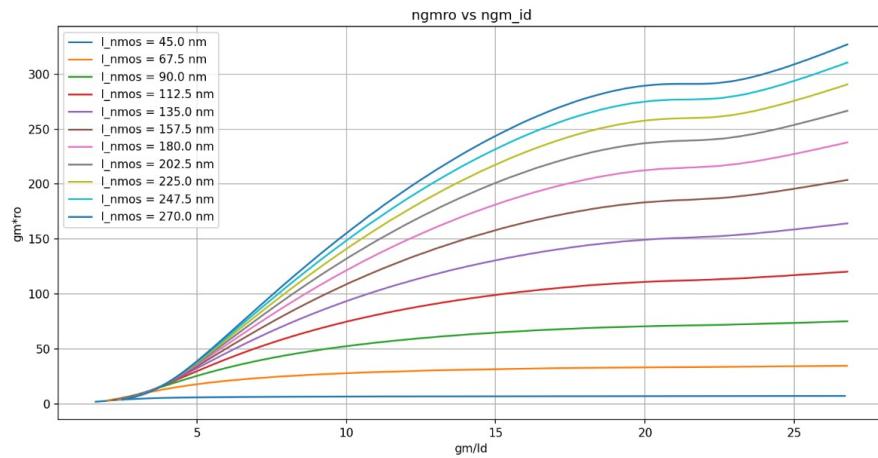


Figure 3: NMOS Techplots after Python postprocessing - gmro

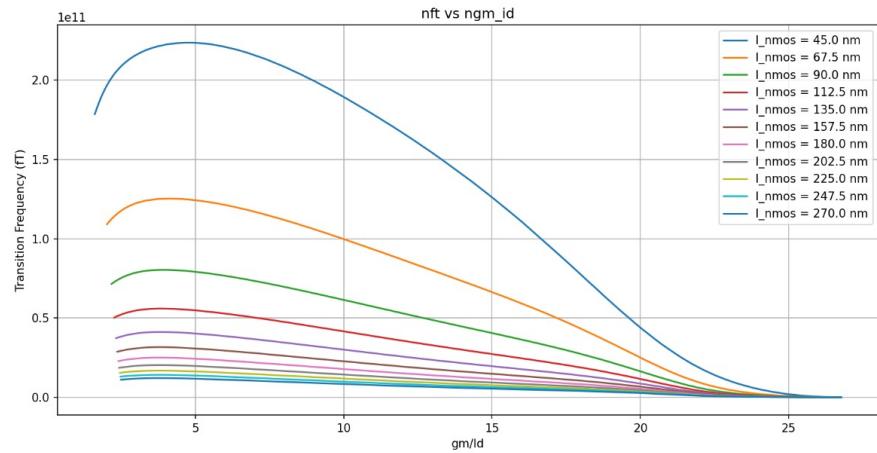


Figure 4: NMOS Techplots after Python postprocessing - fT

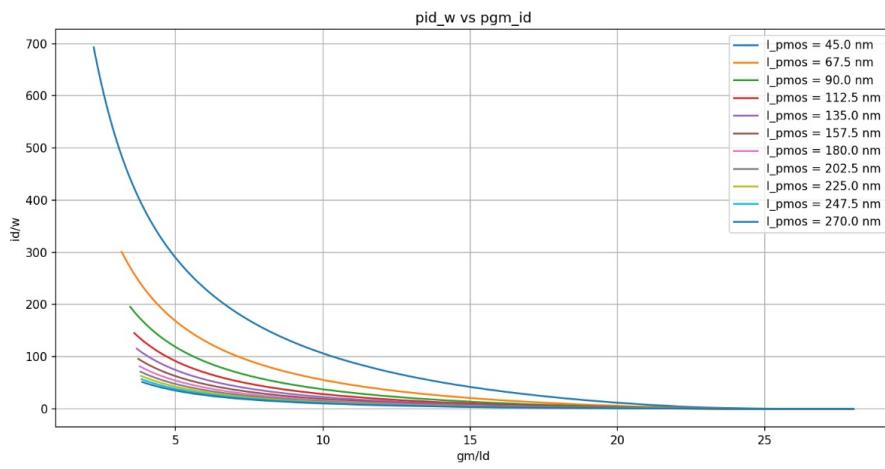


Figure 5: PMOS Techplots after Python postprocessing - Id/W

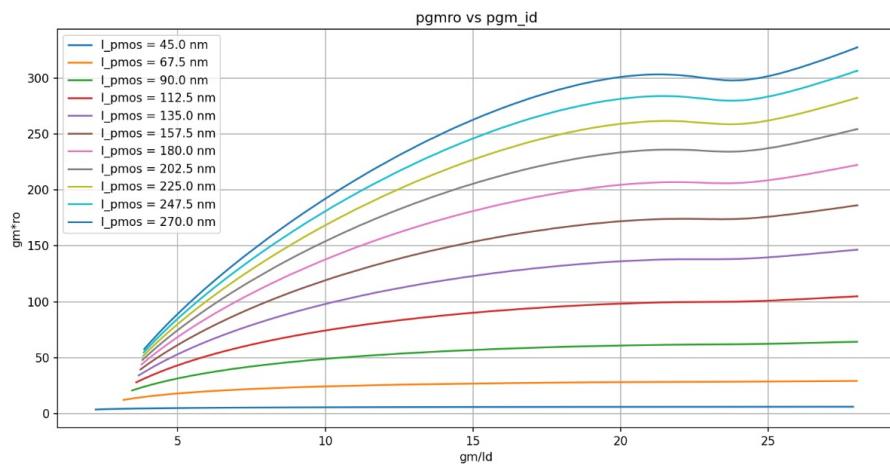


Figure 6: PMOS Techplots after Python postprocessing - gmro

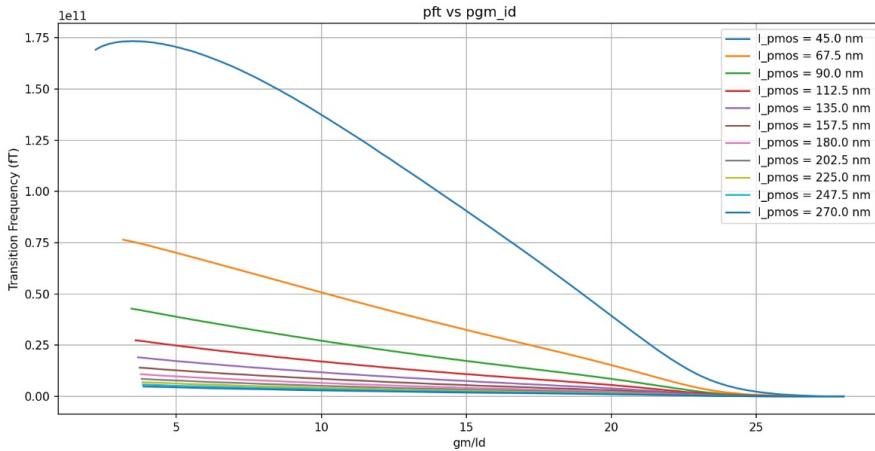


Figure 7: PMOS Techplots after Python postprocessing - fT

4. FET Sizes

Provided the dimensions of the passFET, differential amplifier, and current mirror transistors, including their small-signal parameters and figures of merit (FOMs). Additionally, analyze the loop gain behavior under both heavy-load and light-load conditions.

Table 3: FET Sizes and Parameters

Transistor	Size (W/L)	Tweaked (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	267u/90n	-	10	48.88	37.35	27.1 GHz
Diff-Amp pmos	0.669u/90n	0.61u/90n	10	48.88	37.35	27.1 GHz
Diff-Amp nmos	0.28u/90n	-	10	48.88	37.35	27.1 GHz
Current Mirror nmos	1.607u/270n	-	10	155	31.11	8.3 GHz

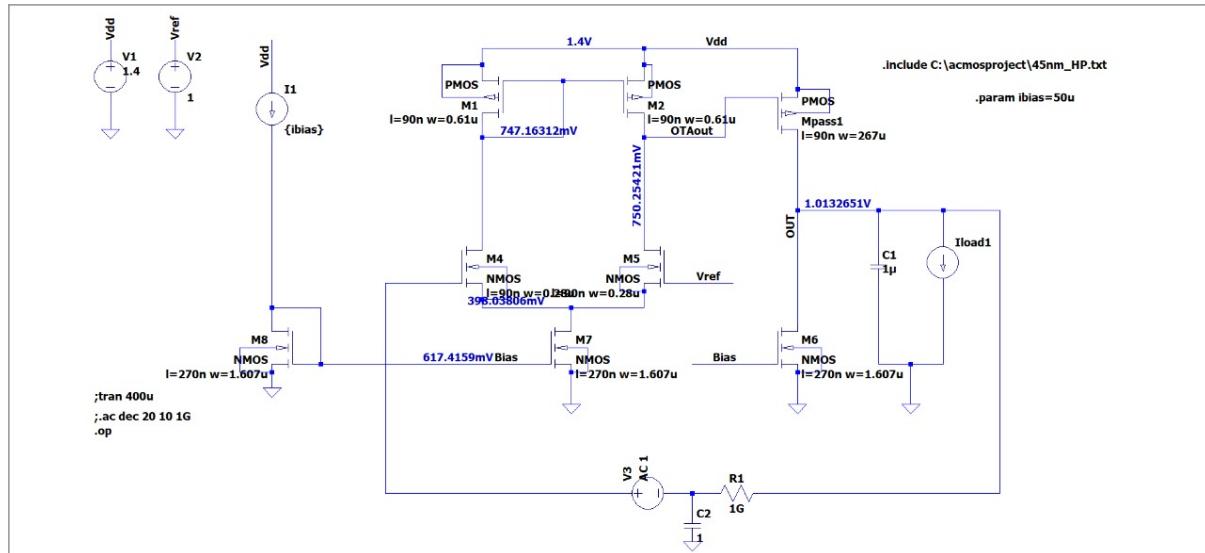


Figure 8: FET sizes and characteristics.

5. Stability Analysis

For Heavy load ($I_{load} = 10\text{mA}$) we get the following curve:

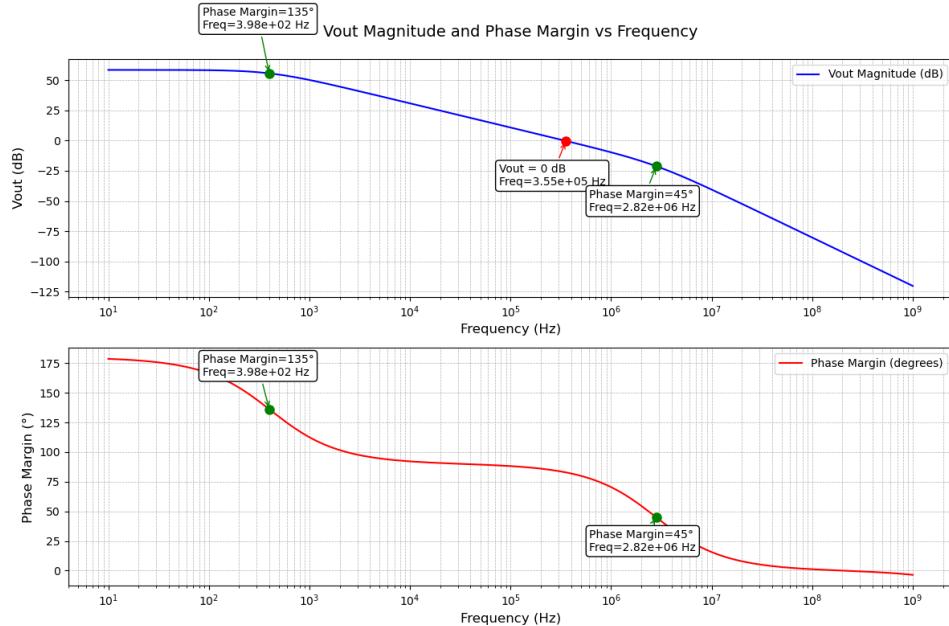


Figure 9: Stability Analysis

For Light load ($I_{load} = 2\text{mA}$) we get the following curve

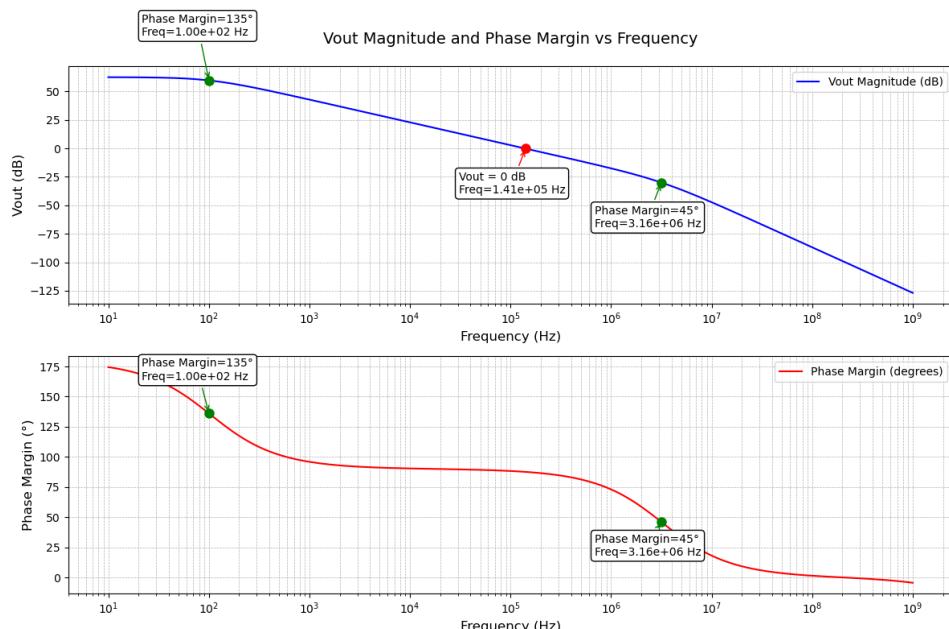


Figure 10: Stability Analysis

From the analysis, it is evident that the unity gain bandwidth is closer to the second pole in the heavy load case compared to the light load case. Additionally, the phase margin is lower for the heavy load case compared to the light load case. This indicates that under a light load, the system exhibits greater stability.

Table 4: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.7	62.32
Unity Gain Bandwidth (kHz)	355	141
Phase Margin (degrees)	82.89	87.58
Pole 1 (Hz)	411.3	101.1
Pole 2 (MHz)	2.77	3.26

6. PSRR Explanation

LDOs are critical components in the power supply of most integrated circuits (ICs), providing a stable and ripple-free fixed output voltage while isolating it from input noise. One of the key performance metrics for an LDO is the Power Supply Rejection Ratio (PSRR). The Power Supply Rejection Ratio (PSRR) is a measure of how effectively a circuit can suppress or attenuate input voltage fluctuations (ripples or noise) from appearing at its output. PSRR is mathematically defined as:

$$\text{PSRR} = 20 \log \left(\frac{V_{\text{in}}}{V_{\text{out}}} \right),$$

where V_{in} and V_{out} are the magnitudes of the input and output ripples, respectively. A higher PSRR value indicates better noise attenuation by the LDO.

The PSRR performance of an LDO can be categorized into two regions:

- **Region 1:** This includes the low to mid-frequency range, extending up to the regulator's bandwidth frequency (ω_{reg}). In this region, PSRR is primarily determined by the loop gain (LG) of the regulator, making it critical to design the feedback loop for optimal performance.
- **Region 2:** Beyond ω_{reg} , PSRR becomes independent of the loop gain and is instead influenced by factors such as output parasitics, PCB impedance, and other high-frequency effects.

By understanding and optimizing the factors affecting PSRR in these regions, designers can ensure that the LDO effectively filters input noise, delivering a clean and stable output voltage.

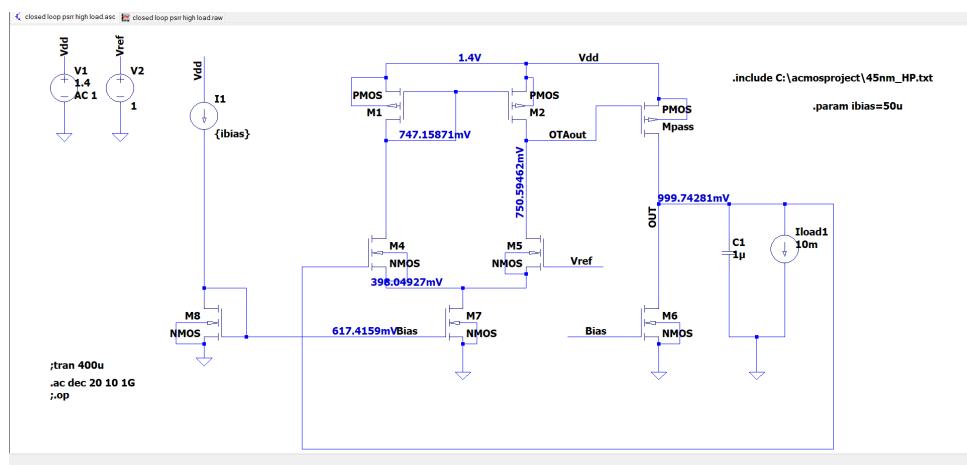


Figure 11: PSRR Schematic

7. PSRR Simulation Results

Three different schematics are used for the underlying three cases

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

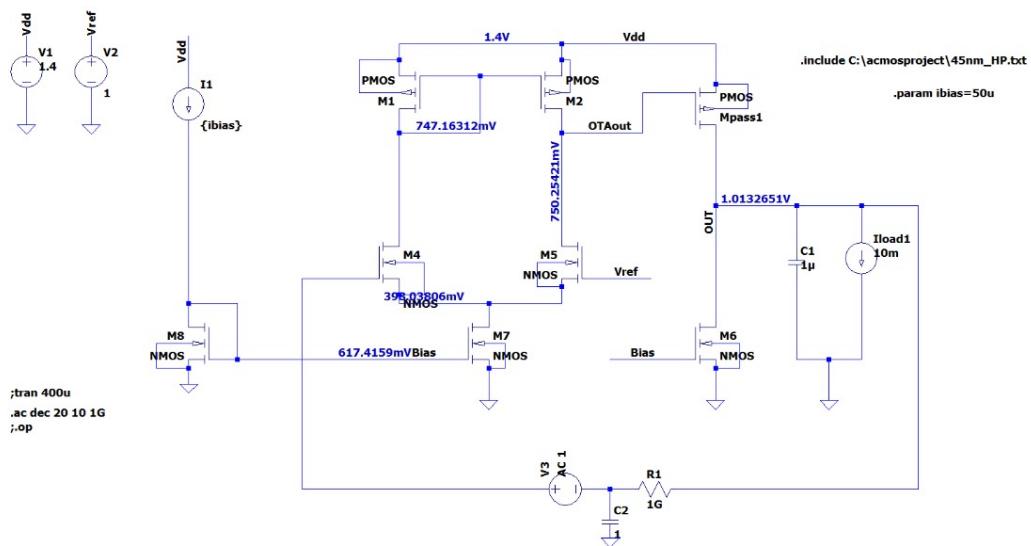


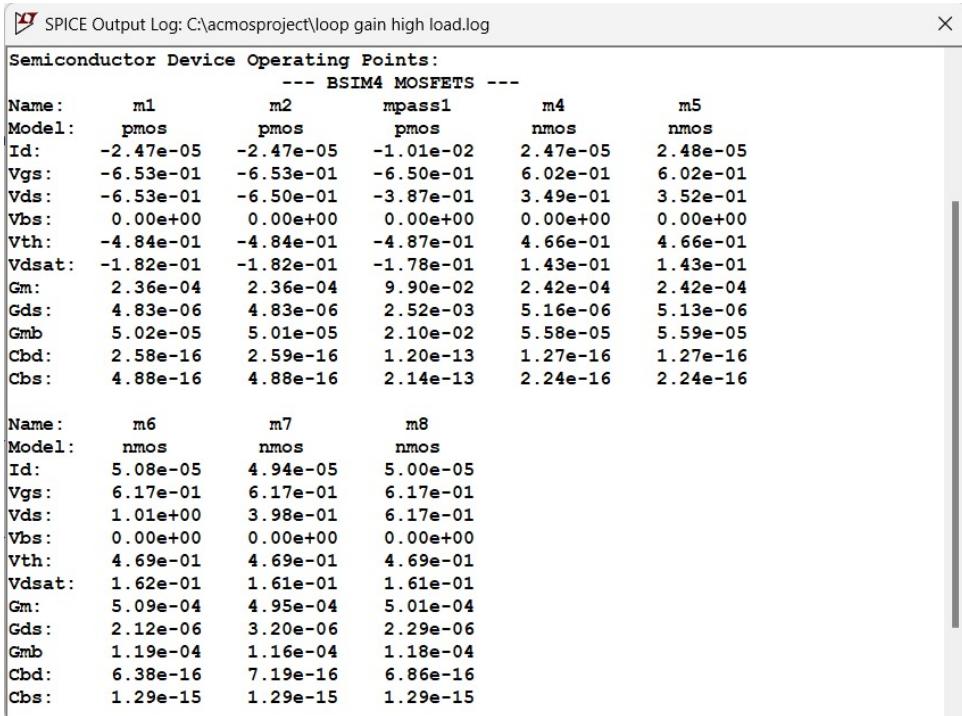
Figure 12: Schematic

Explanation of the artifact used:-

To calculate the loop gain, an RC circuit is placed in the feedback loop along with an AC source of amplitude 1V, ensuring a consistent AC voltage at the output. Simultaneously, the circuit needs to be biased by providing a DC voltage to the gate of the NMOS in the differential amplifier. The RC circuit serves this purpose by blocking DC current from flowing to the ground while directing any high-frequency AC signals at the output to the ground.

Since the resistor in the RC circuit has a very high resistance and the current entering the MOSFET gate is negligible, the voltage drop across the resistor is minimal. This setup effectively biases the circuit while enabling the calculation of the loop gain.

Output Log File:-



The screenshot shows a SPICE output log window titled "SPICE Output Log: C:\acmosproject\loop gain high load.log". The window displays "Semiconductor Device Operating Points" for "BSIM4 MOSFETS". The data is organized into two sections: one for PMOS devices (m1-m5) and one for NMOS devices (m6-m8). Each section lists parameters such as Name, Model, Id, Vgs, Vds, Vbs, Vth, Vdsat, Gm, Gds, Gmb, Cbd, and Cbs, along with their corresponding values.

Semiconductor Device Operating Points: --- BSIM4 MOSFETS ---					
Name:	m1	m2	mpass1	m4	m5
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-2.47e-05	-2.47e-05	-1.01e-02	2.47e-05	2.48e-05
Vgs:	-6.53e-01	-6.53e-01	-6.50e-01	6.02e-01	6.02e-01
Vds:	-6.53e-01	-6.50e-01	-3.87e-01	3.49e-01	3.52e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.84e-01	-4.84e-01	-4.87e-01	4.66e-01	4.66e-01
Vdsat:	-1.82e-01	-1.82e-01	-1.78e-01	1.43e-01	1.43e-01
Gm:	2.36e-04	2.36e-04	9.90e-02	2.42e-04	2.42e-04
Gds:	4.83e-06	4.83e-06	2.52e-03	5.16e-06	5.13e-06
Gmb:	5.02e-05	5.01e-05	2.10e-02	5.58e-05	5.59e-05
Cbd:	2.58e-16	2.59e-16	1.20e-13	1.27e-16	1.27e-16
Cbs:	4.88e-16	4.88e-16	2.14e-13	2.24e-16	2.24e-16
Name:	m6	m7	m8		
Model:	nmos	nmos	nmos		
Id:	5.08e-05	4.94e-05	5.00e-05		
Vgs:	6.17e-01	6.17e-01	6.17e-01		
Vds:	1.01e+00	3.98e-01	6.17e-01		
Vbs:	0.00e+00	0.00e+00	0.00e+00		
Vth:	4.69e-01	4.69e-01	4.69e-01		
Vdsat:	1.62e-01	1.61e-01	1.61e-01		
Gm:	5.09e-04	4.95e-04	5.01e-04		
Gds:	2.12e-06	3.20e-06	2.29e-06		
Gmb:	1.19e-04	1.16e-04	1.18e-04		
Cbd:	6.38e-16	7.19e-16	6.86e-16		
Cbs:	1.29e-15	1.29e-15	1.29e-15		

Figure 13: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.653	0.653	0.484	0.169	Saturation
M2	PMOS	0.649	0.653	0.484	0.169	Saturation
Mpass	PMOS	0.4	0.649	0.487	0.162	Saturation
M4	NMOS	0.349	0.602	0.466	0.136	Saturation
M5	NMOS	0.353	0.602	0.466	0.136	Saturation
M6	NMOS	1.00	0.617	0.469	0.148	Saturation
M7	NMOS	0.398	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 5: Transistor Parameters and Operating Regions

Output on Python:-

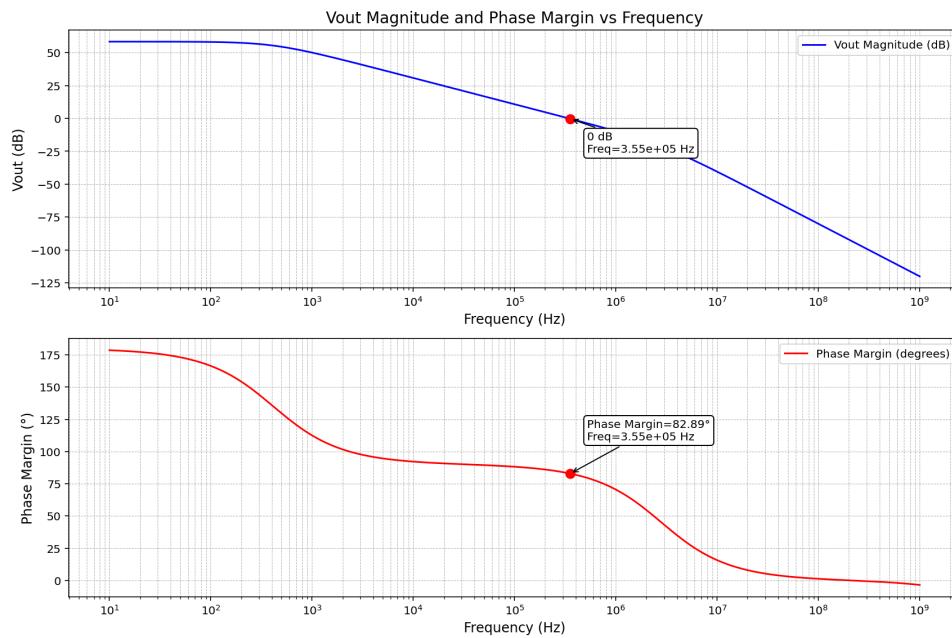


Figure 14: Output on Python

The phase margin is 82.89

The output voltage (Loop gain) comes out to be close to 58.7db . The formula for loop gain is $A_{diff} A_{pass}$ where A_{diff} is differential amplifier gain and A_{pass} is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

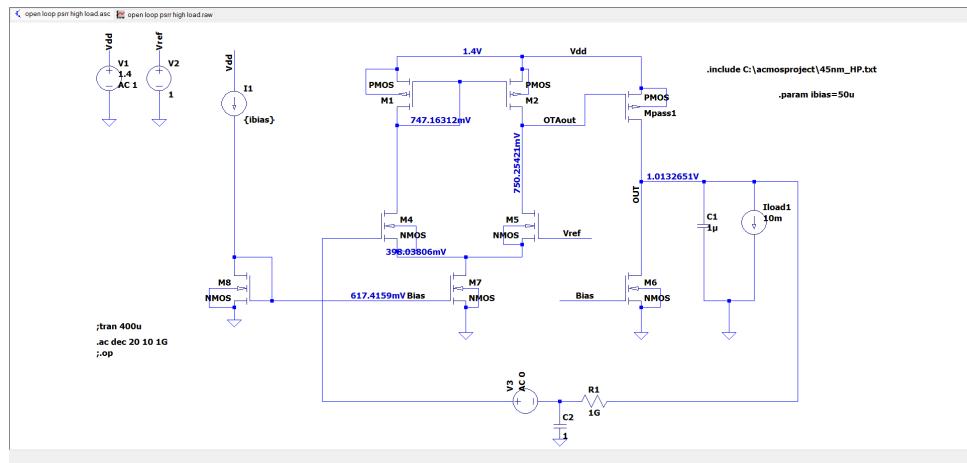


Figure 15: Schematic

Explanation of the artifact used:-

To calculate the open-loop PSRR, an AC signal is applied from the source, which in this case is VDD. We use an AC signal with an amplitude of 1 and apply it to the source of the pass transistor as well as the source of the PMOS in the differential amplifier. Ideally, we aim for poor PSRR performance in the differential amplifier, allowing the OTA output to carry all the AC noise. This ensures that the small-signal V_{sg} of the PMOS equals zero, resulting in complete noise rejection and a clean DC voltage at the LDO output.

For this analysis, an RC circuit is used to bias the differential amplifier. The presence of "AC 0" in the circuit indicates that it operates in an open-loop configuration. Based on this setup, we compute the open-loop PSRR of the circuit. Since feedback is absent, noise at the output remains significant, leading to poor rejection characteristics.

Output on Python:-

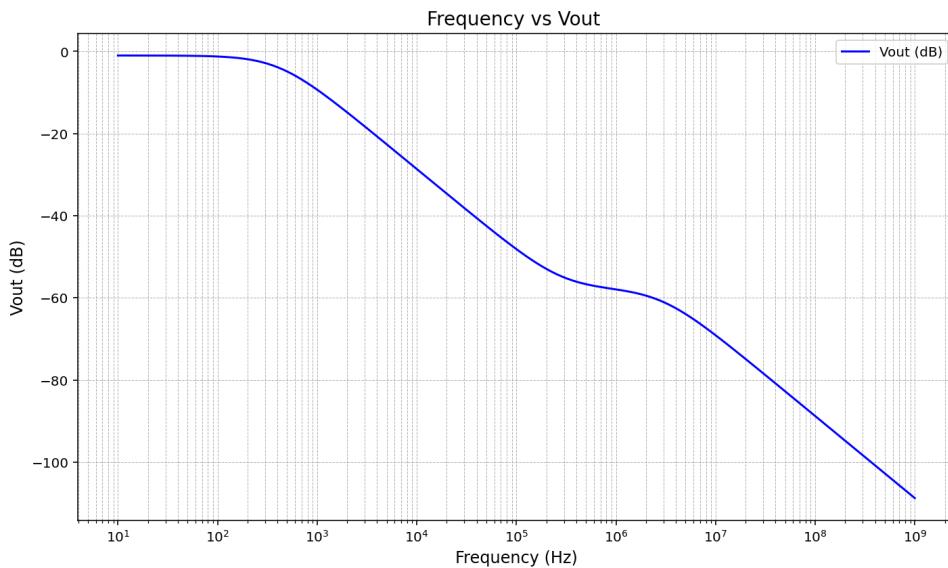


Figure 16: V_{out} vs frequency

V_{ota} vs frequency

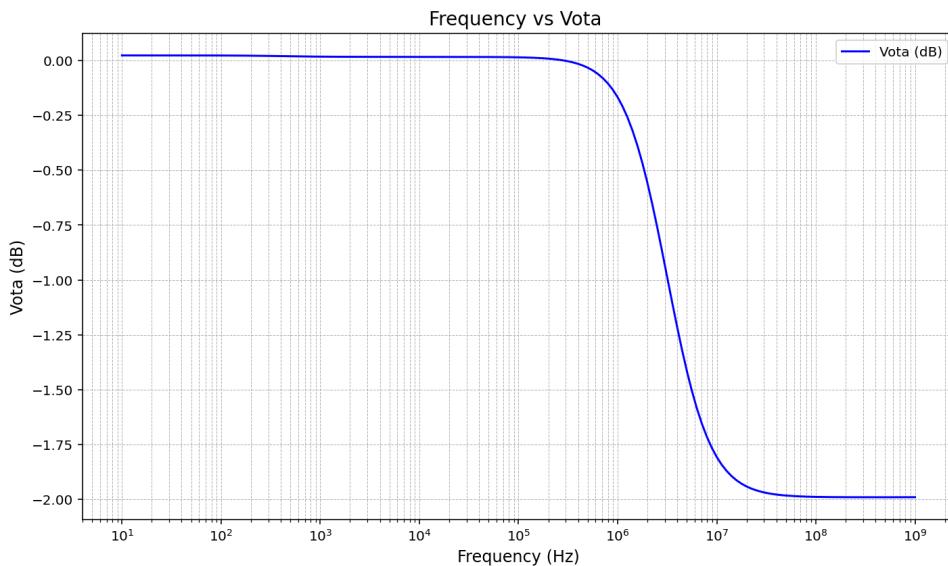


Figure 17: V_{ota} vs frequency

Note:- V_{ota} output in volts will give you the insight into what AC voltage is coming into the gate of the passfet. It should be close to VDD. The closer it is to 1v the better it is for a very bad PSRR at the output as the V_{sg} value will be close to 0.

Case 3:- Closed Loop PSRR Calculation

Schematic

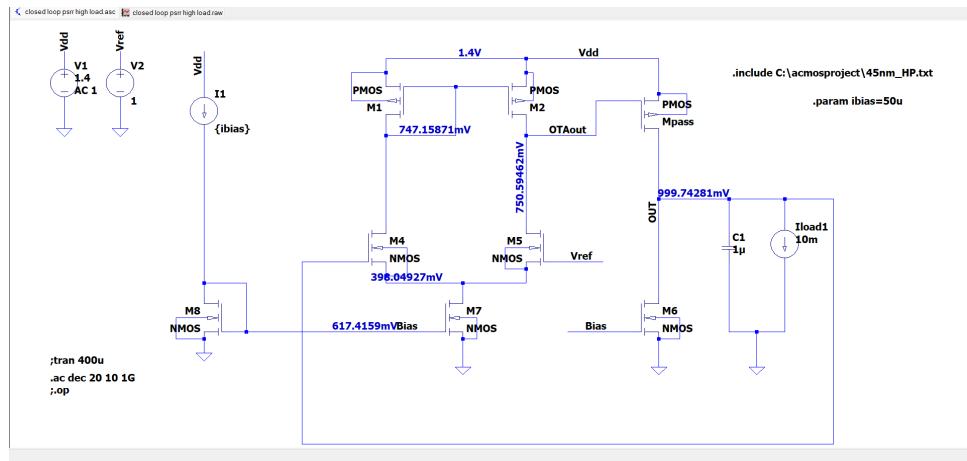


Figure 18: Schematic

Explanation of the artifact used:-

An AC signal is applied to the voltage source (VDD) in this scenario. The circuit includes feedback from the output terminal to the input of the differential amplifier, establishing the feedback path. The goal is to analyze the negative feedback, which cancels out the output voltage as part of a small-signal analysis. Based on the specified requirements (60 dB), we expect to observe a high Power Supply Rejection Ratio (PSRR), confirming the accuracy of the transistor sizing.

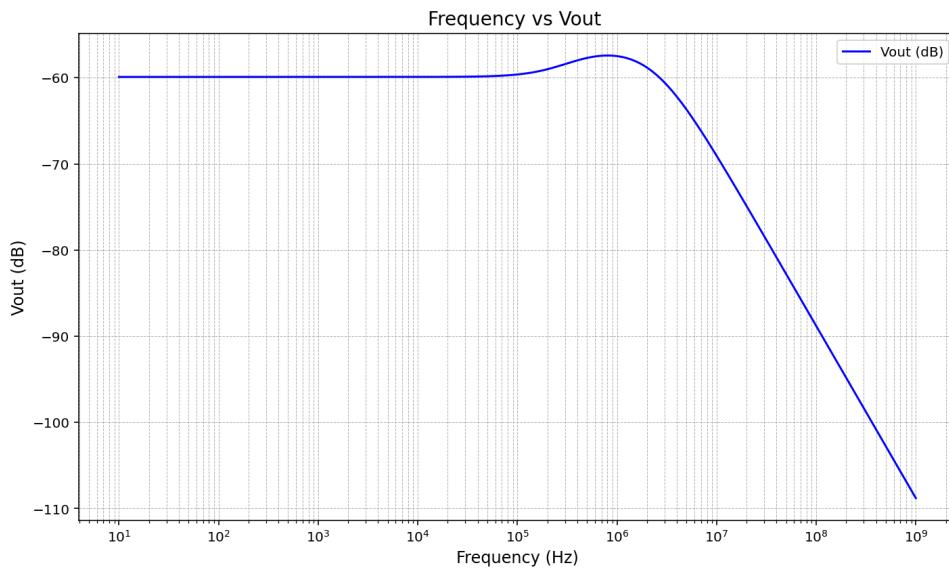
Output on Python:-

Figure 19: Vout vs frequency

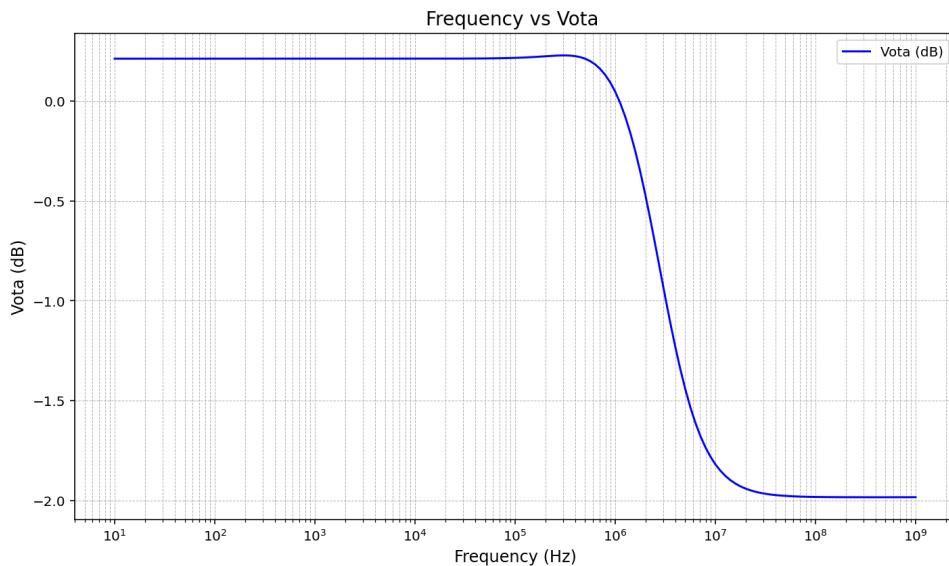
Vota vs frequency

Figure 20: Vota vs frequency

Light Load (2ma)

Case 1:- Loop gain analysis

Schematic

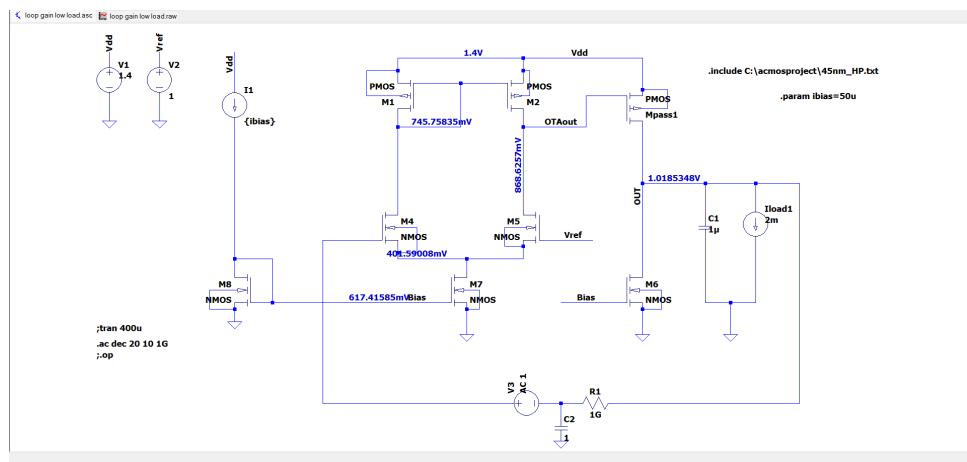


Figure 21: Schematic

Output Log File:-

```
SPICE Output Log: C:\acmosproject\closed loop psrr low load.log
--- BSIM4 MOSFETS ---
Name: m1 m2 mpass1 m4 m5
Model: pmos pmos pmos nmos nmos
Id: -2.50e-05 -2.44e-05 -2.05e-03 2.50e-05 2.44e-05
Vgs: -6.54e-01 -6.54e-01 -5.31e-01 6.03e-01 5.98e-01
Vds: -6.54e-01 -5.31e-01 -3.95e-01 3.44e-01 4.67e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth: -4.84e-01 -4.85e-01 -4.87e-01 4.66e-01 4.65e-01
Vdsat: -1.83e-01 -1.82e-01 -9.49e-02 1.44e-01 1.42e-01
Gm: 2.38e-04 2.34e-04 3.58e-02 2.43e-04 2.42e-04
Gds: 4.87e-06 5.09e-06 6.53e-04 5.29e-06 4.30e-06
Gmb: 5.05e-05 4.96e-05 7.39e-03 5.61e-05 5.59e-05
Cbd: 2.58e-16 2.65e-16 1.20e-13 1.27e-16 1.23e-16
Cbs: 4.88e-16 4.88e-16 2.14e-13 2.24e-16 2.24e-16

Name: m6 m7 m8
Model: nmos nmos nmos
Id: 5.08e-05 4.94e-05 5.00e-05
Vgs: 6.17e-01 6.17e-01 6.17e-01
Vds: 1.00e+00 4.02e-01 6.17e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00
Vth: 4.69e-01 4.69e-01 4.69e-01
Vdsat: 1.62e-01 1.61e-01 1.61e-01
Gm: 5.08e-04 4.95e-04 5.01e-04
Gds: 2.12e-06 3.17e-06 2.29e-06
Gmb: 1.19e-04 1.16e-04 1.18e-04
Cbd: 6.39e-16 7.19e-16 6.86e-16
Cbs: 1.29e-15 1.29e-15 1.29e-15
```

Figure 22: Output Log Details

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.654	0.654	0.484	0.170	Saturation
M2	PMOS	0.531	0.654	0.485	0.169	Saturation
Mpass	PMOS	0.395	0.531	0.487	0.044	Saturation
M4	NMOS	0.344	0.603	0.466	0.137	Saturation
M5	NMOS	0.467	0.598	0.465	0.133	Saturation
M6	NMOS	1.00	0.617	0.469	0.148	Saturation
M7	NMOS	0.402	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 6: Transistor Data Table

Case 1:- Loop Gain Analysis

Output on Python:-

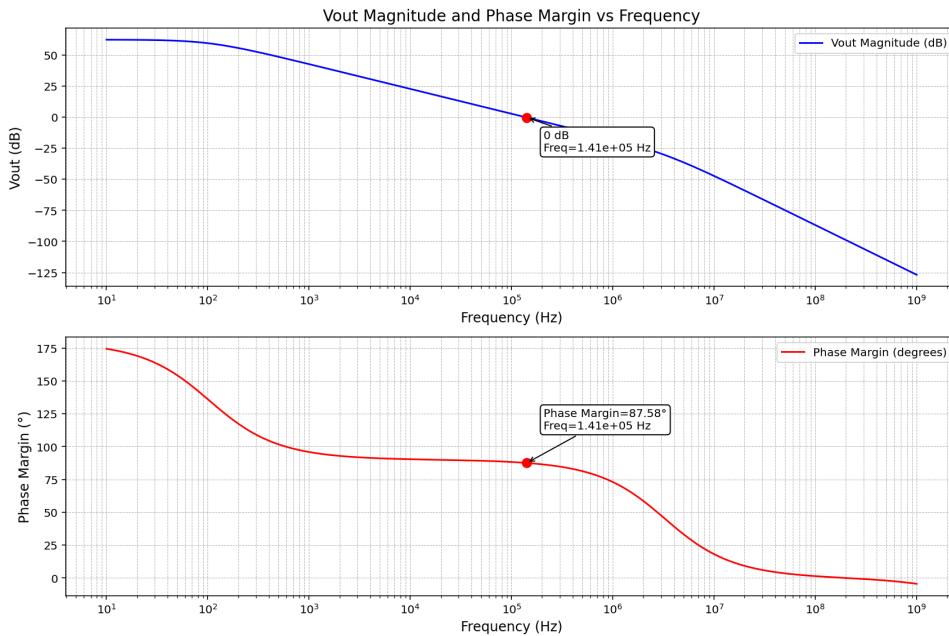


Figure 23: Output on Python

The phase margin obtained is 87.58 degrees. This value is more than that of the value obtained for heavy load. Thus proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR calculation

Schematic

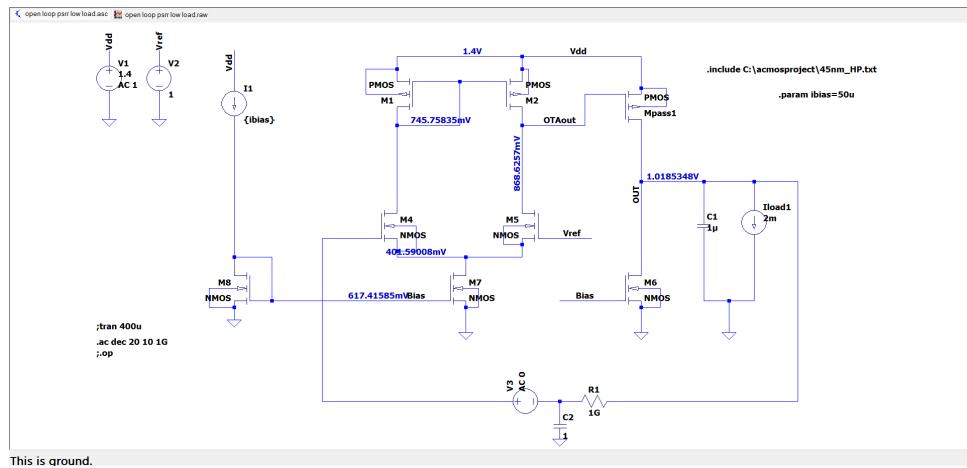


Figure 24: Schematic

Output on Python:-

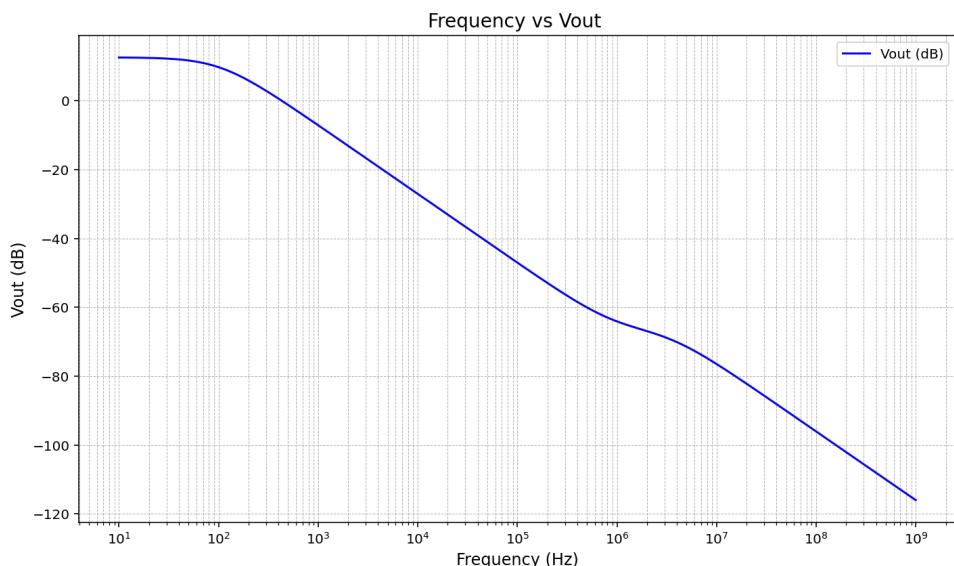


Figure 25: Vout vs frequency

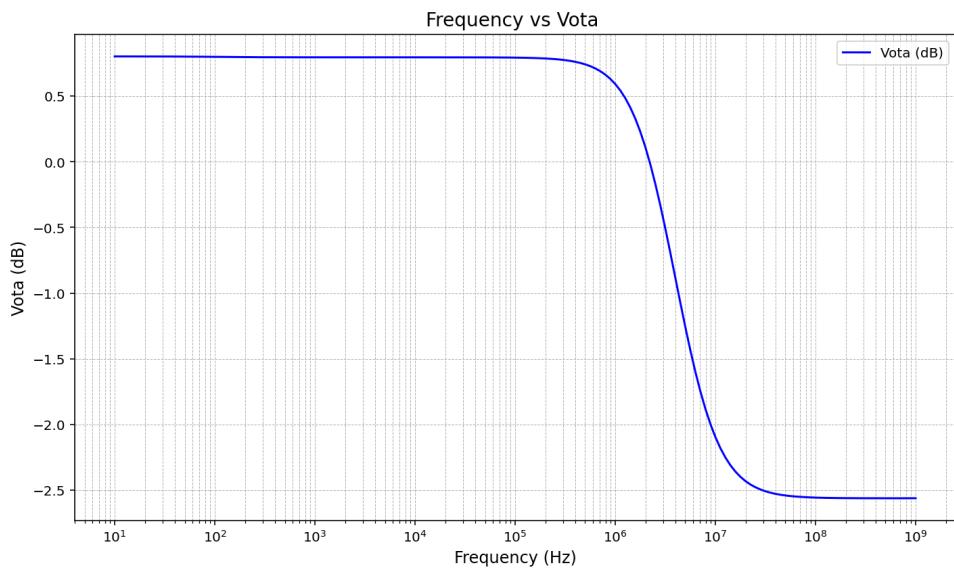


Figure 26: Vota vs frequency

Case 3:- Closed loop PSRR calculation

Schematic

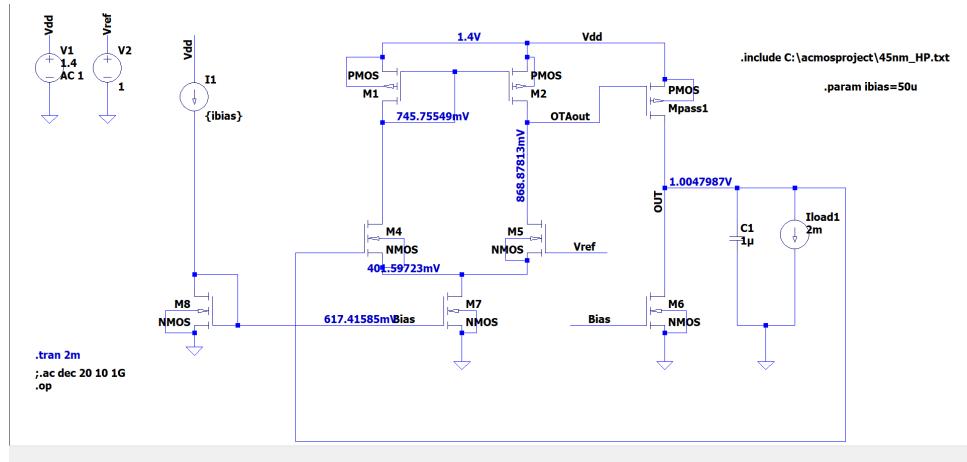


Figure 27: Schematic

Output on Python:-

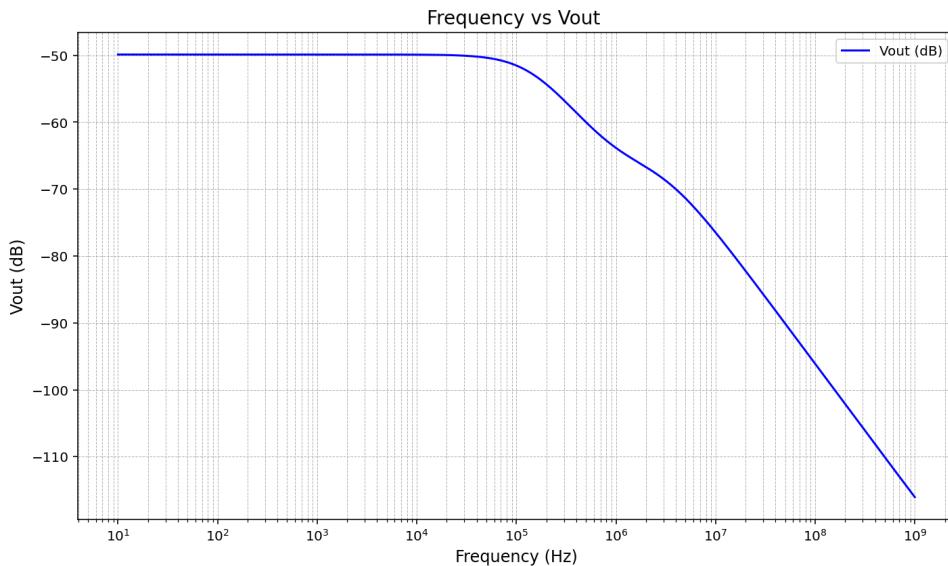


Figure 28: Vout vs frequency

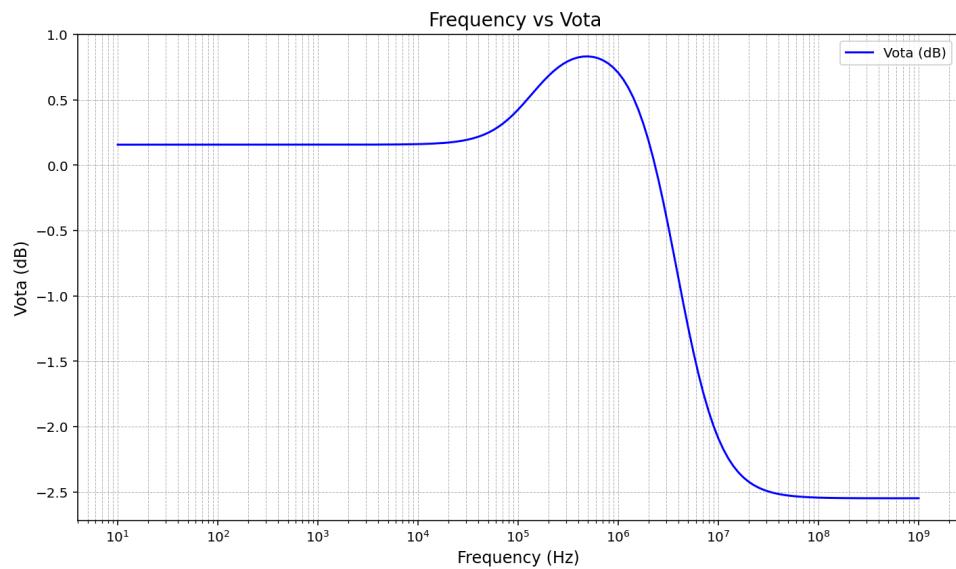


Figure 29: Vota vs frequency

8. Transient Simulation Results

A pulse signal with a rise time and fall time of 1 μ s was applied at the load. The pulse has a period of 10 ms and a 50% duty cycle. From the figure below, it is evident that the output stabilizes within the specified time range. Additionally, no overshoot or undershoot is observed in the output response.

Schematic:-

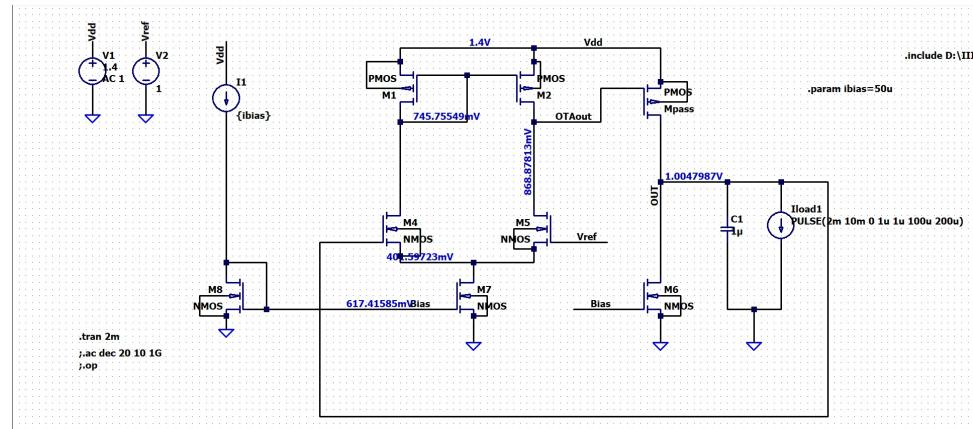


Figure 30: Schematic

Output on Python:-

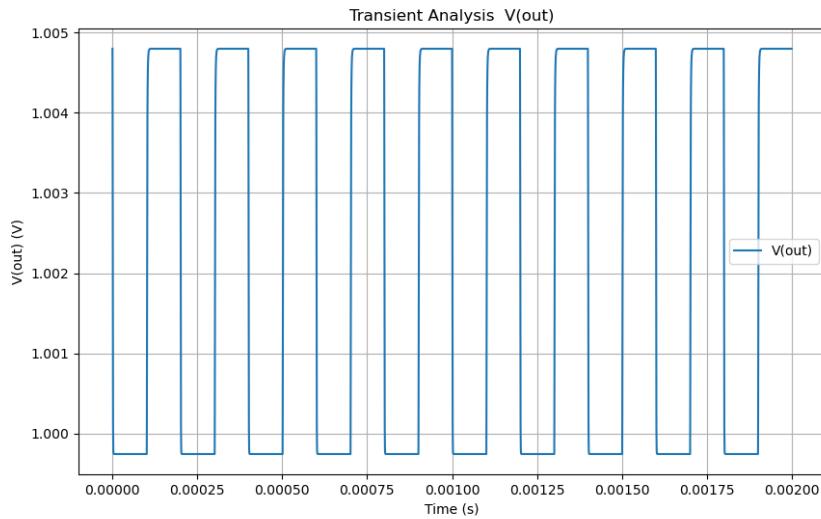


Figure 31: Vout vs time

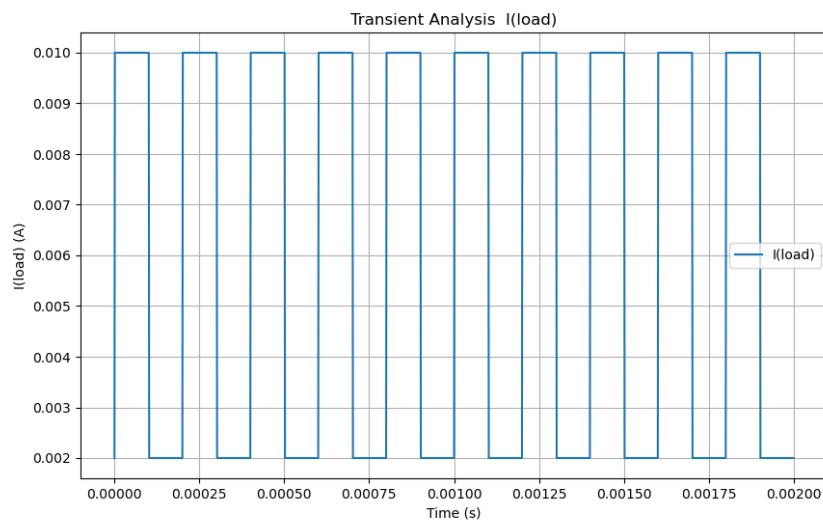
Output on Python:-

Figure 32: Iload vs time

9.Simulation vs Hand Calculations for Externally Compensated

For Heavy load, $I_{load} = 10\text{mA}$

For Passfet

Hand Calculation

- $r_o = 500 \Omega$
- $g_m = 0.1 \text{ A/V}$
- W_{p1} (first pole location) = $2\pi f = 2.00\text{k}$
- $g_m r_o = 50$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 406.5 \Omega$
- $g_m = 0.0991 \text{ A/V}$
- W_{p1} (first pole location) = $2\pi f = 2.46\text{k}$
- $g_m r_o = 40.28$

Table 7: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
$r_o (\Omega)$	406.5	500	18.69%
$g_m (\text{A/V})$	0.0991	0.1	0.9%
$W_{p1} (\text{Hz})$	2.46k	2.00k	-22.9%
$g_m r_o$	40.28	50	19.43%

For Light load, Iload = 2mA

For Passfet

Hand Calculation

- $r_o = 2500 \Omega$
- $g_m = 0.02 \text{ A/V}$
- W_{p1} (first pole location) = $= 2\pi f = 0.4\text{k}$
- $g_m r_o = 50$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 1531.39 \Omega$
- $g_m = 0.0358 \text{ A/V}$
- W_{p1} (first pole location) = $2\pi f = 0.653\text{k}$
- $g_m r_o = 54.82$

Table 8: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
ro ()	1531.39	2500	38.8%
gm (A/V)	0.0358	0.02	-79%
Wp1 (Hz)	0.653k	0.4k	-38.7%
gmro	40.28	50	-9.64%

Internally Compensated LDO

Three different schematics are used for the underlying three cases

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

Stability Analysis

For Heavy load ($I_{load} = 10\text{mA}$) we get the following curve:

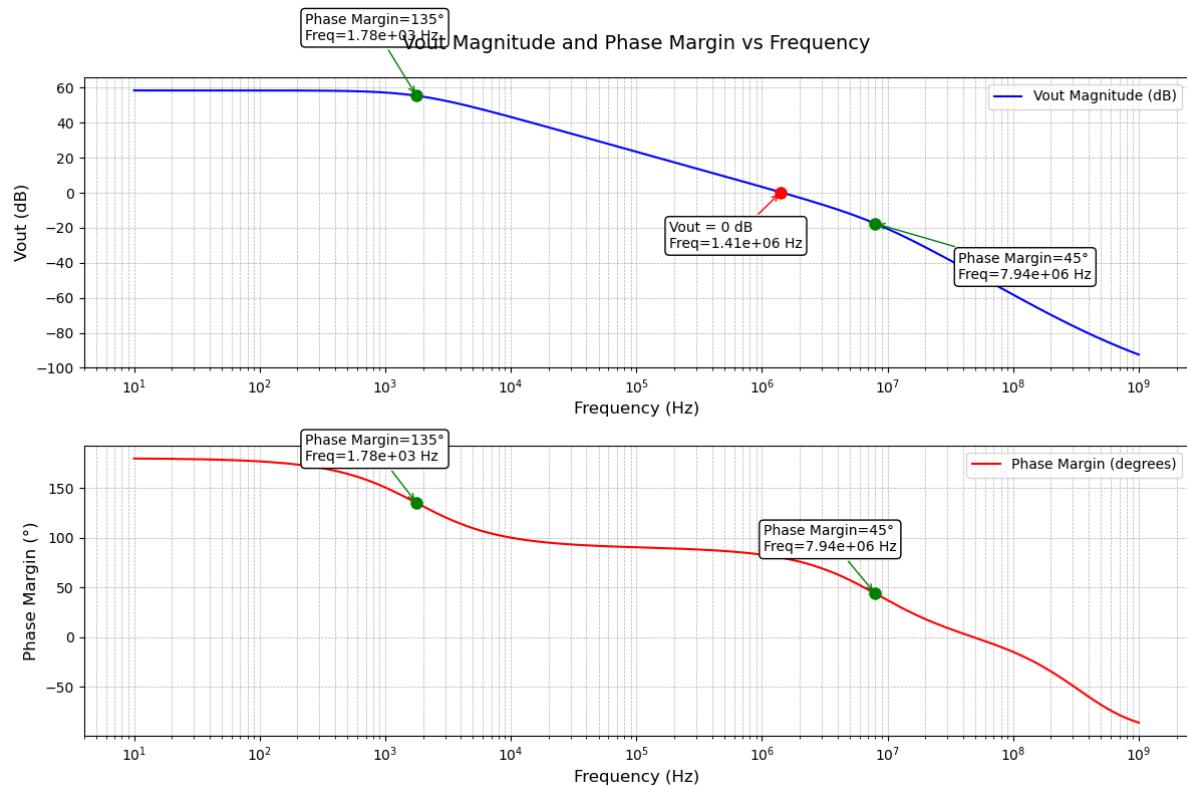


Figure 33: Stability Analysis

For Light load ($I_{load} = 2\text{mA}$) we get the following curve

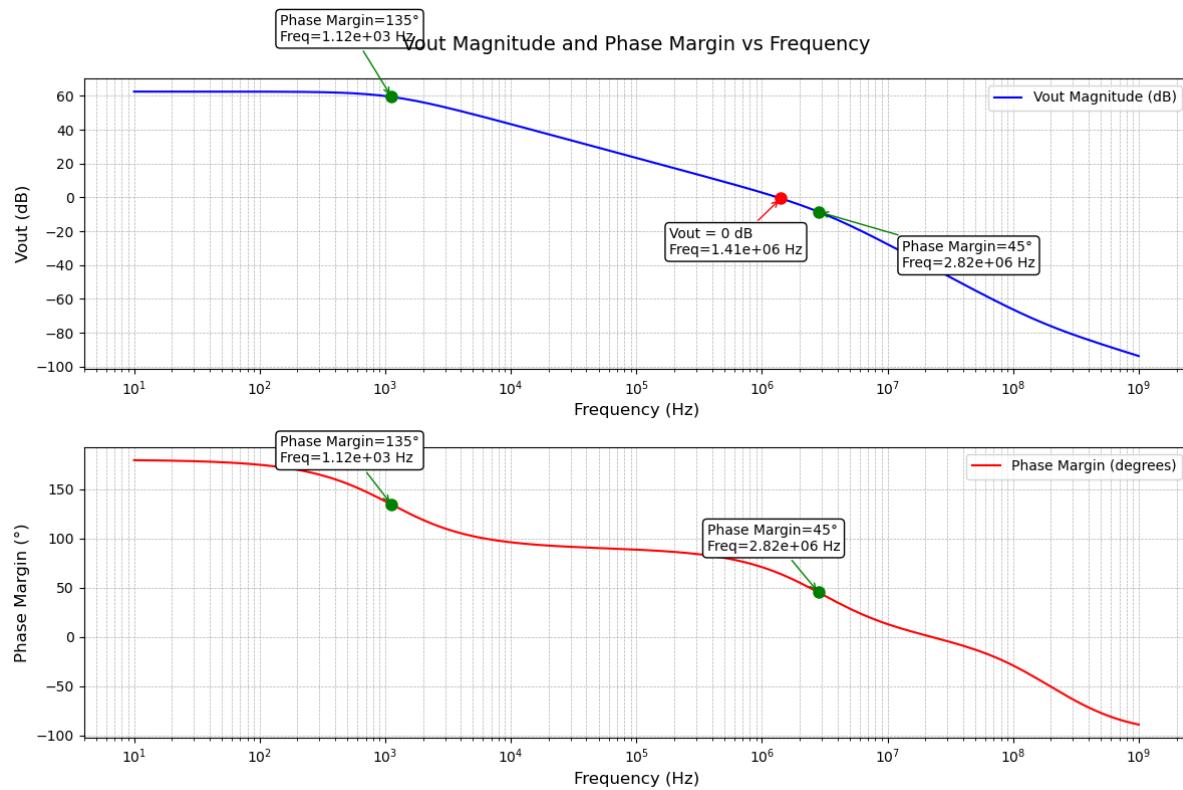


Figure 34: Stability Analysis

Light Load (2mA)

Schematic

Case 1:- Loop gain analysis:-

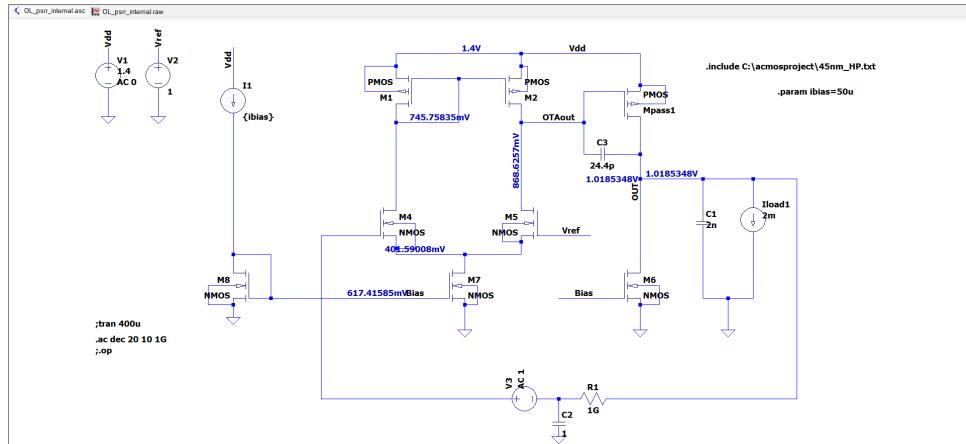


Figure 35: Schematic

Output Log File:-

```
SPICE Output Log: C:\acmosproject\CL_psrr_internal.log
--- BSIM4 MOSFETS ---
Name: m1 m2 mpass1 m4 m5
Model: pmos pmos pmos nmos nmos
Id: -2.50e-05 -2.44e-05 -2.05e-03 2.50e-05 2.44e-05
Vgs: -6.54e-01 -6.54e-01 -5.31e-01 6.03e-01 5.98e-01
Vds: -6.54e-01 -5.31e-01 -3.95e-01 3.44e-01 4.67e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth: -4.84e-01 -4.85e-01 -4.87e-01 4.66e-01 4.65e-01
Vdsat: -1.83e-01 -1.82e-01 -9.49e-02 1.44e-01 1.42e-01
Gm: 2.38e-04 2.34e-04 3.58e-02 2.43e-04 2.42e-04
Gds: 4.87e-06 5.09e-06 6.53e-04 5.29e-06 4.30e-06
Gmb: 5.05e-05 4.96e-05 7.39e-03 5.61e-05 5.59e-05
Cbd: 2.58e-16 2.65e-16 1.20e-13 1.27e-16 1.23e-16
Cbs: 4.88e-16 4.88e-16 2.14e-13 2.24e-16 2.24e-16

Name: m6 m7 m8
Model: nmos nmos nmos
Id: 5.08e-05 4.94e-05 5.00e-05
Vgs: 6.17e-01 6.17e-01 6.17e-01
Vds: 1.00e+00 4.02e-01 6.17e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00
Vth: 4.69e-01 4.69e-01 4.69e-01
Vdsat: 1.62e-01 1.61e-01 1.61e-01
Gm: 5.08e-04 4.95e-04 5.01e-04
Gds: 2.12e-06 3.17e-06 2.29e-06
Gmb: 1.19e-04 1.16e-04 1.18e-04
Cbd: 6.39e-16 7.19e-16 6.86e-16
Cbs: 1.29e-15 1.29e-15 1.29e-15
```

Figure 36: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.654	0.654	0.484	0.170	Saturation
M2	PMOS	0.531	0.654	0.485	0.169	Saturation
Mpass	PMOS	0.395	0.531	0.487	0.044	Saturation
M4	NMOS	0.344	0.603	0.466	0.137	Saturation
M5	NMOS	0.467	0.598	0.465	0.133	Saturation
M6	NMOS	1.00	0.617	0.469	0.148	Saturation
M7	NMOS	0.402	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 9: Transistor Parameters and Operating Regions

Output on Python:-

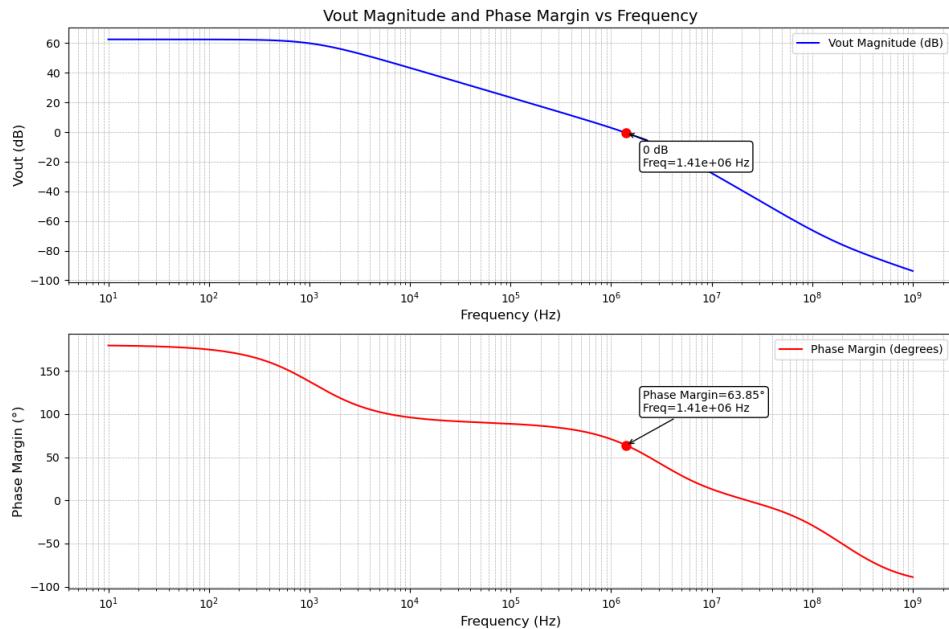


Figure 37: Vout and Phase Margin vs frequency

From above plot we can see Phase Margin = 63.58°

Case 2:- Open Loop PSRR calculation

Schematic

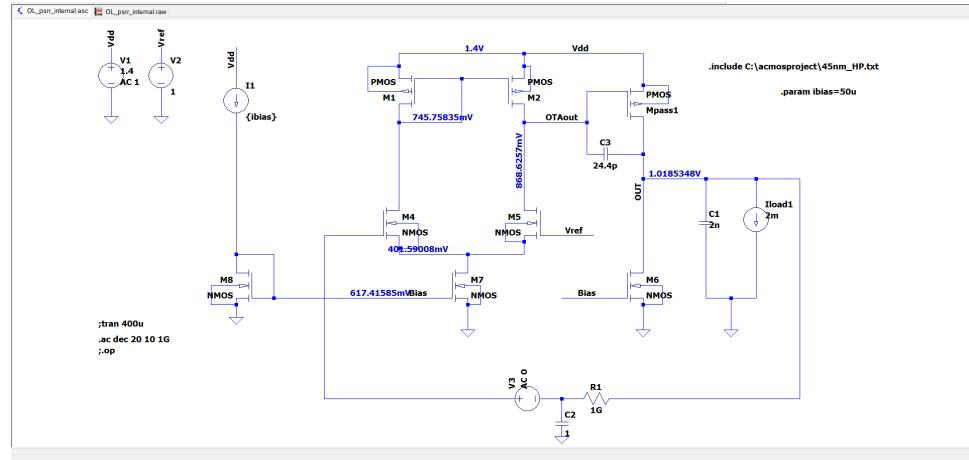


Figure 38: Schematic

Output on Python:-

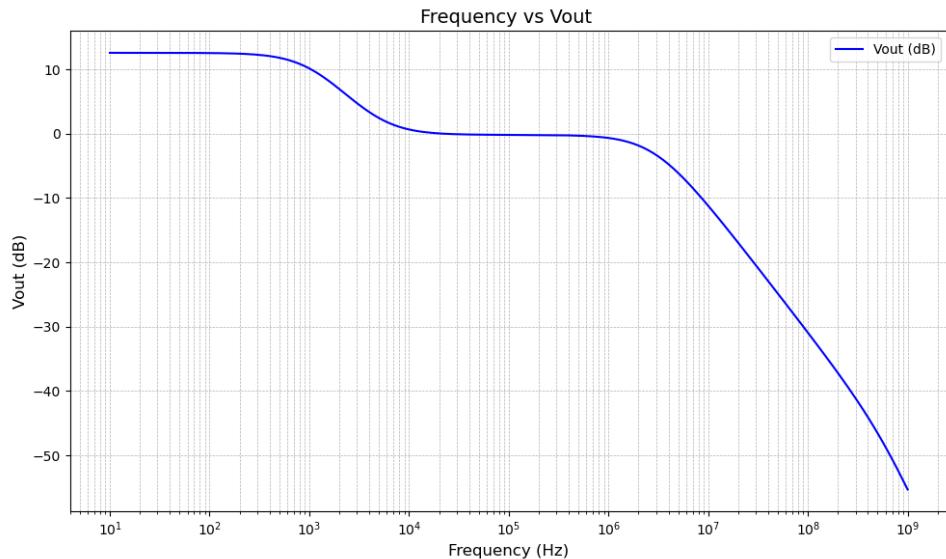


Figure 39: Vout vs frequency

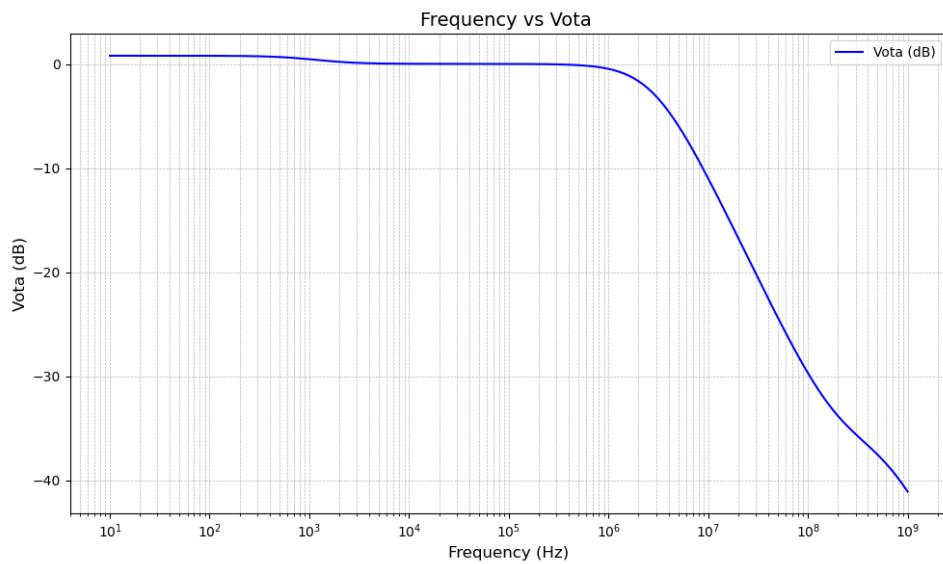


Figure 40: Vota vs frequency

Case 3:- Closed loop PSRR calculation

Schematic

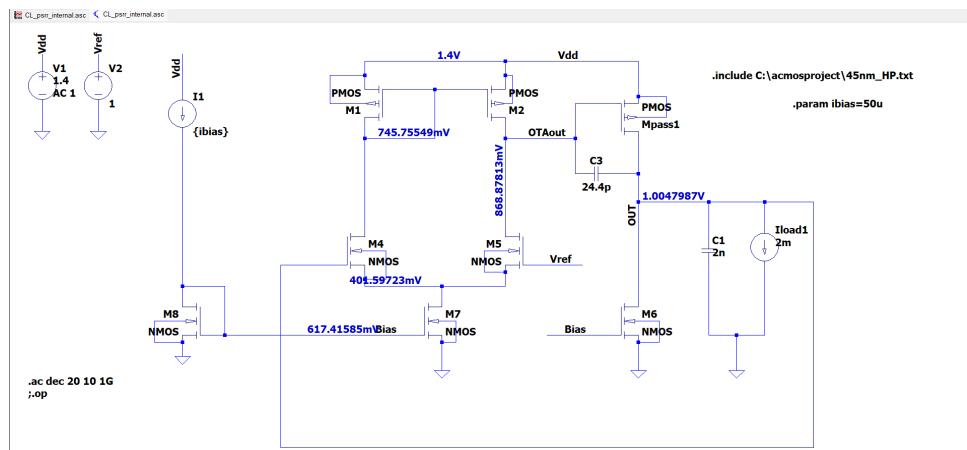


Figure 41: Schematic

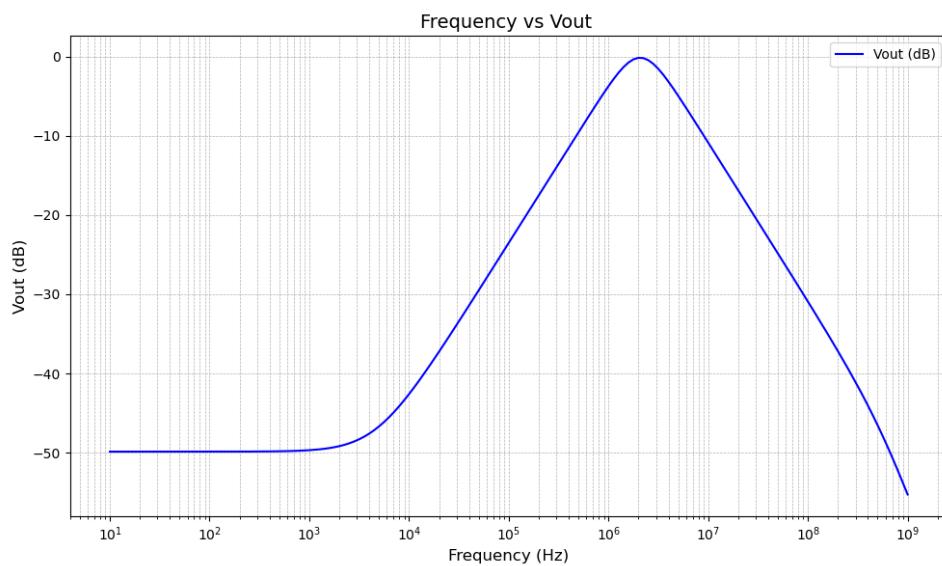
Output on Python:-

Figure 42: Vout vs frequency

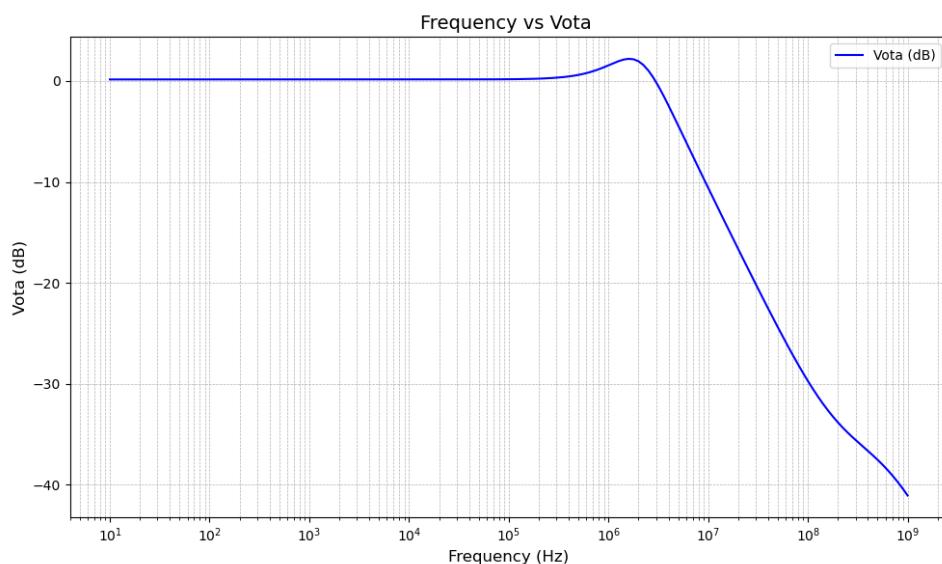


Figure 43: Vota vs frequency

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

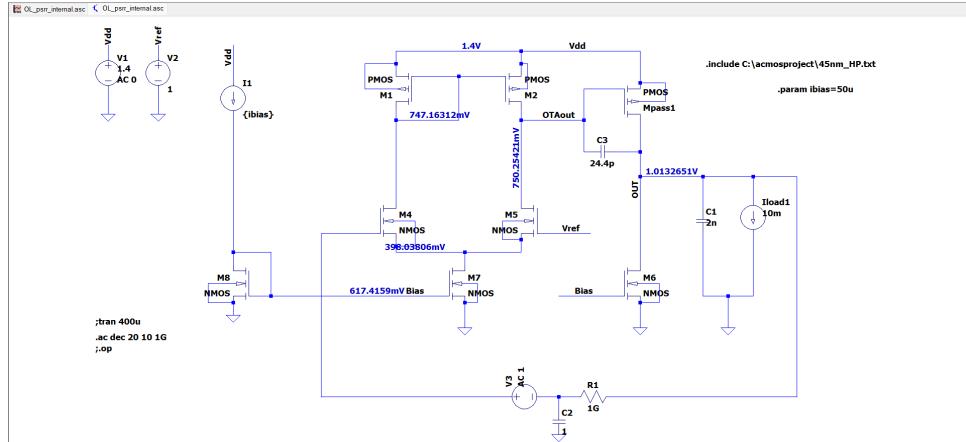


Figure 44: Schematic

Explanation of the artifact used:-

Output Log File:-

--- BSIM4 MOSFETS ---					
Name:	m1	m2	mpass1	m4	m5
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-2.47e-05	-2.47e-05	-1.01e-02	2.47e-05	2.48e-05
Vgs:	-6.53e-01	-6.53e-01	-6.49e-01	6.02e-01	6.02e-01
Vds:	-6.53e-01	-6.49e-01	-4.00e-01	3.49e-01	3.53e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.84e-01	-4.84e-01	-4.87e-01	4.66e-01	4.66e-01
Vdsat:	-1.82e-01	-1.82e-01	-1.77e-01	1.43e-01	1.43e-01
Gm:	2.36e-04	2.36e-04	9.91e-02	2.42e-04	2.42e-04
Gds:	4.83e-06	4.83e-06	2.46e-03	5.16e-06	5.13e-06
Gmb:	5.02e-05	5.01e-05	2.10e-02	5.58e-05	5.59e-05
Cbd:	2.58e-16	2.59e-16	1.19e-13	1.27e-16	1.27e-16
Cbs:	4.88e-16	4.88e-16	2.14e-13	2.24e-16	2.24e-16
Name:	m6	m7	m8		
Model:	nmos	nmos	nmos		
Id:	5.08e-05	4.94e-05	5.00e-05		
Vgs:	6.17e-01	6.17e-01	6.17e-01		
Vds:	1.00e+00	3.98e-01	6.17e-01		
Vbs:	0.00e+00	0.00e+00	0.00e+00		
Vth:	4.69e-01	4.69e-01	4.69e-01		
Vdsat:	1.62e-01	1.61e-01	1.61e-01		
Gm:	5.08e-04	4.95e-04	5.01e-04		
Gds:	2.11e-06	3.20e-06	2.29e-06		
Gmb:	1.19e-04	1.16e-04	1.18e-04		
Cbd:	6.39e-16	7.19e-16	6.86e-16		
Cbs:	1.29e-15	1.29e-15	1.29e-15		

Figure 45: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.653	0.653	0.484	0.169	Saturation
M2	PMOS	0.649	0.653	0.484	0.169	Saturation
Mpass	PMOS	0.400	0.649	0.487	0.162	Saturation
M4	NMOS	0.349	0.602	0.466	0.136	Saturation
M5	NMOS	0.353	0.602	0.466	0.136	Saturation
M6	NMOS	1.000	0.617	0.469	0.148	Saturation
M7	NMOS	0.398	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 10: Updated Transistor Parameters and Operating Regions

Output on Python:-

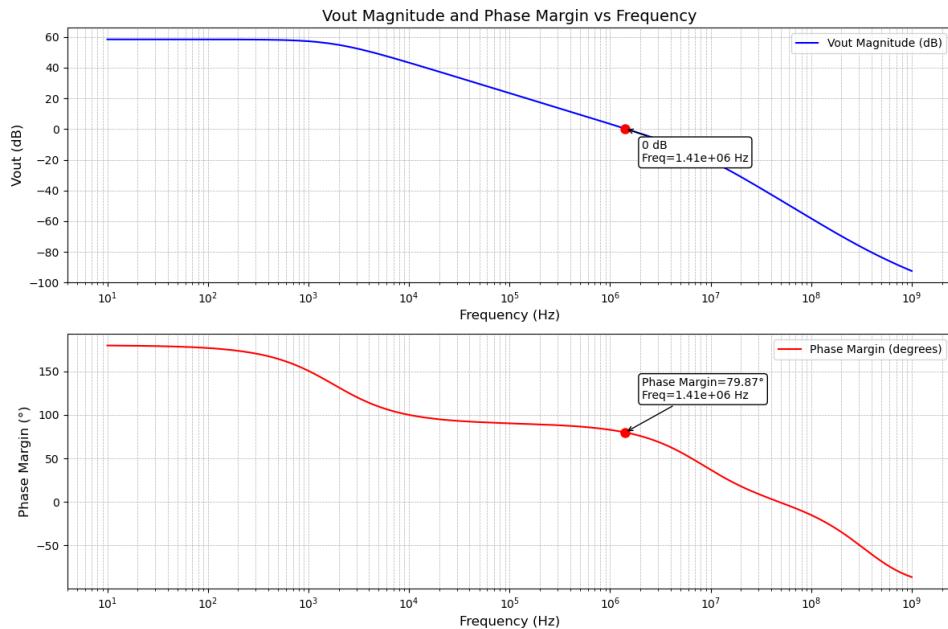


Figure 46: Vout and Phase Margin vs frequency

Case 2:- Open Loop PSRR calculation

Schematic

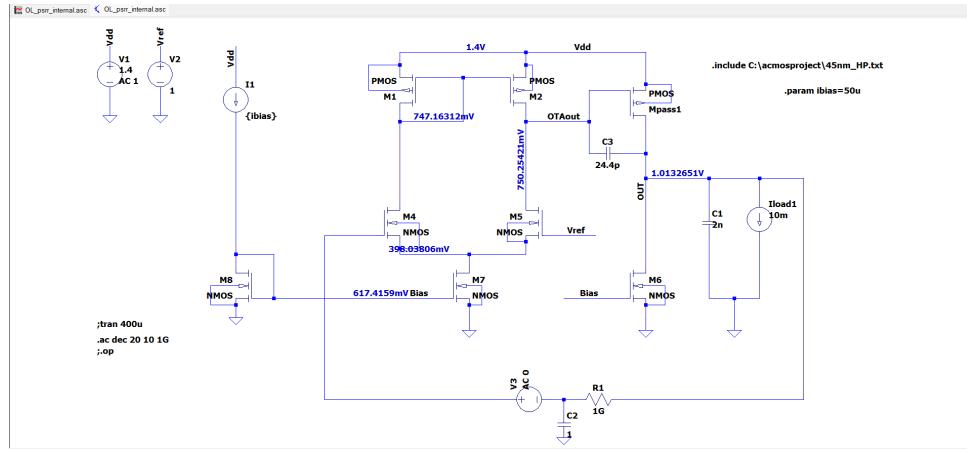


Figure 47: Schematic

Output on Python:-

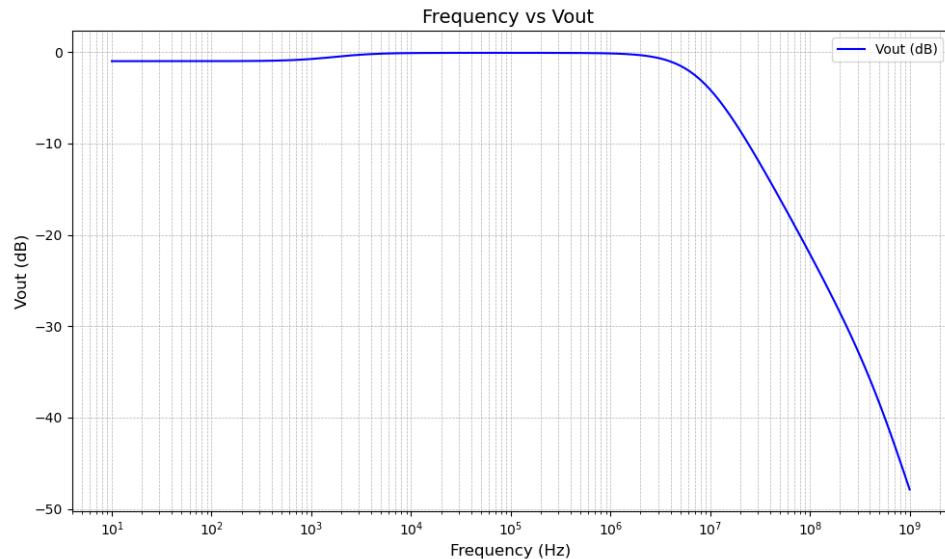


Figure 48: Vout vs frequency

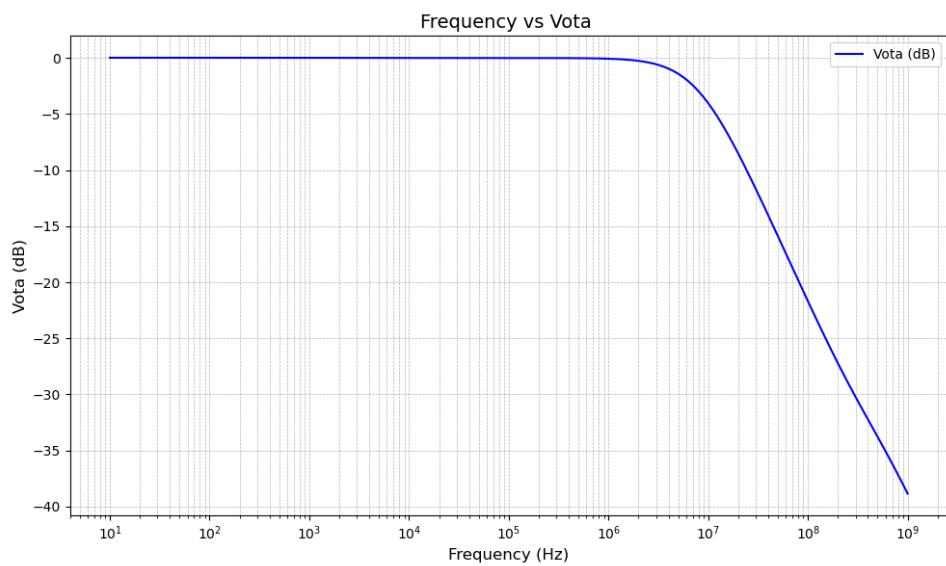


Figure 49: Vota vs frequency

Case 3:- Closed loop PSRR calculation

Schematic

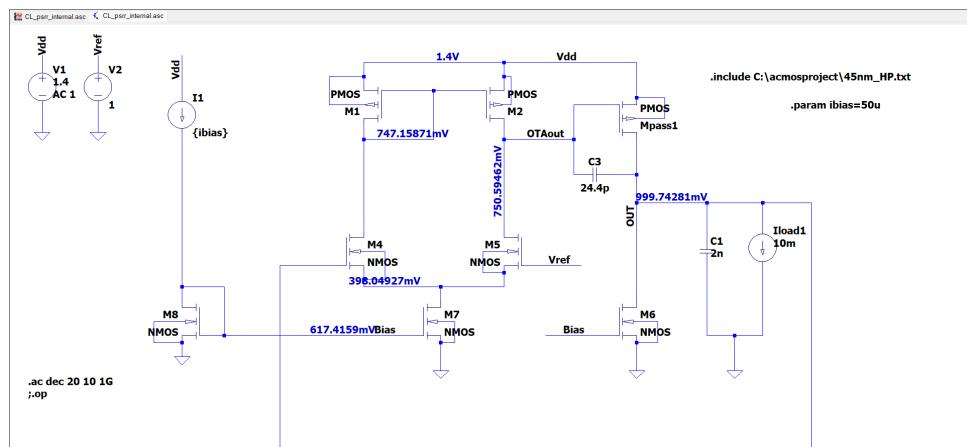


Figure 50: Schematic

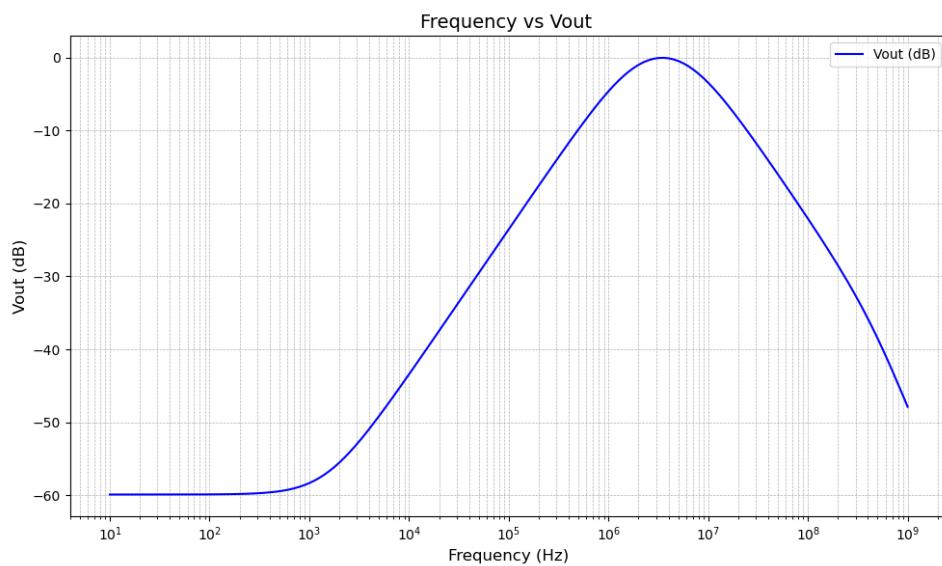
Output on Python:-

Figure 51: Vout vs frequency

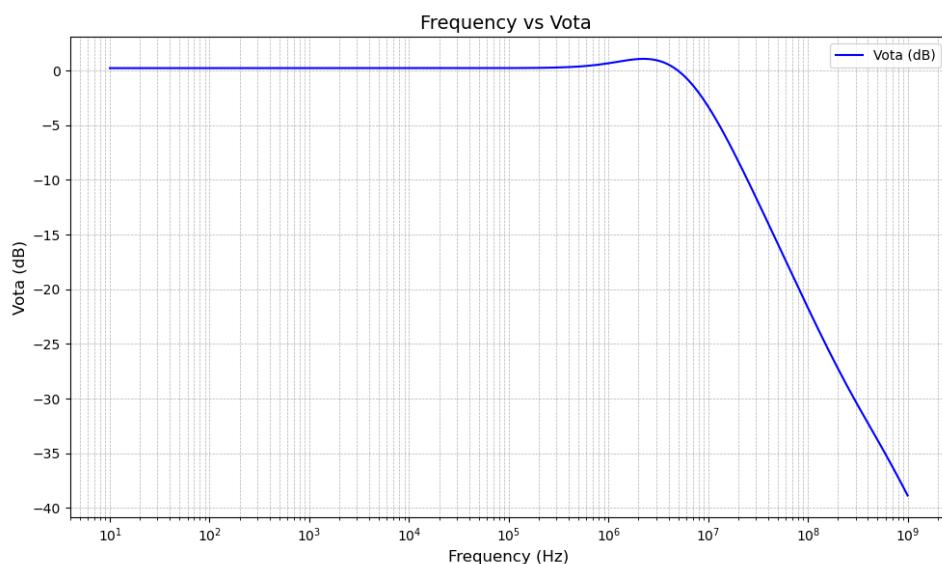


Figure 52: Vota vs frequency

Transient Analysis

Schematic

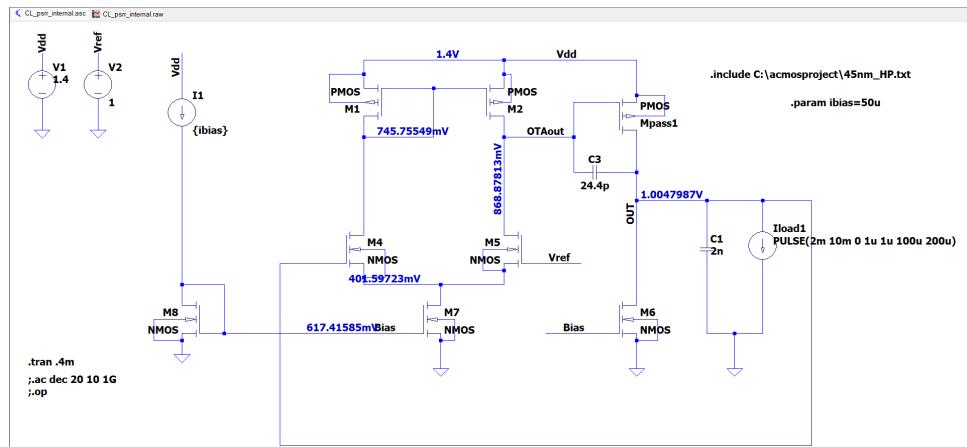


Figure 53: Schematic

Output on Python:-

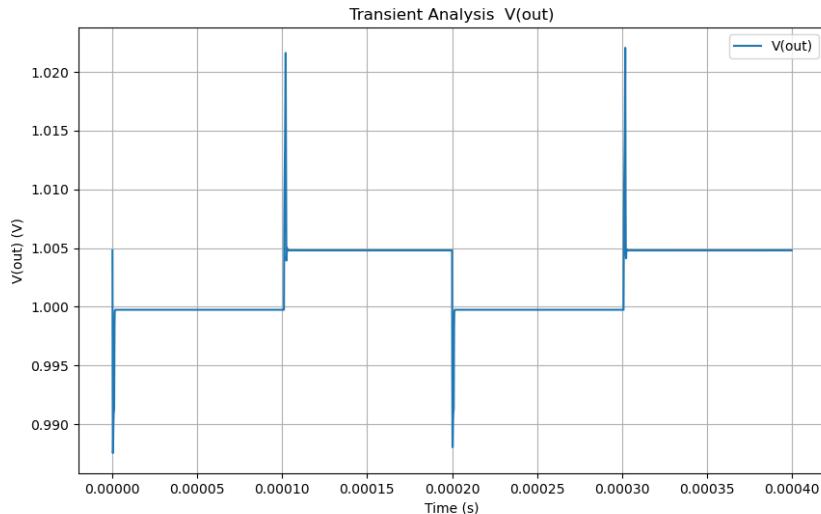


Figure 54: Vout vs time

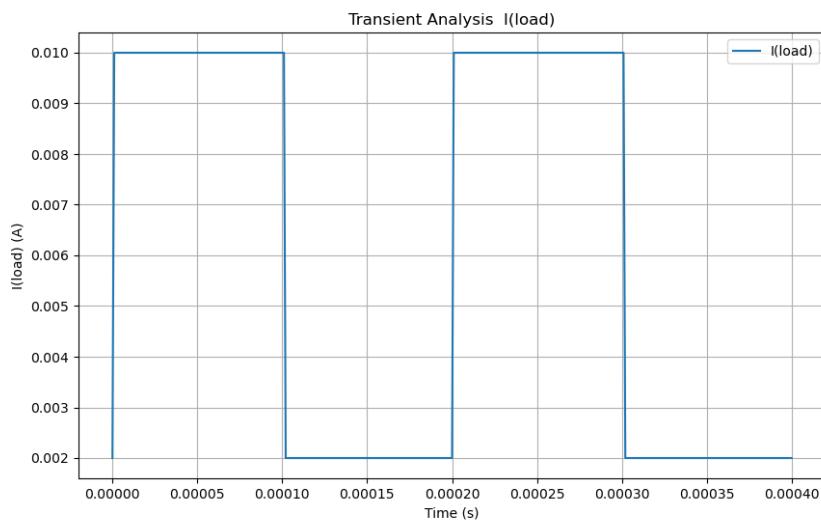
Output on Python:-

Figure 55: Iload vs time

Simulation vs Hand Calculations for Internally Compensated

For OTA

Hand Calculation

- $r_o \text{diff} = 80K \Omega$
- $(g_m) \text{diff} = 0.00025 \text{ A/V}$
- W_{p1} (first pole location) = $2\pi f = 8\text{kHz}$
- $(g_m r_o) \text{diff} = 20$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 100.4K \Omega$
- $(g_m) \text{diff} = 0.00023 \text{ A/V}$
- W_{p1} (first pole location) = $2\pi f = 10\text{kHz}$
- $(g_m r_o) \text{diff} = 23.092$

Table 11: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
rodiff ()	100.4k	80k	-25.5%
(gm)diff (A/V)	0.00023	0.00025	8%
Wp1 (Hz)	8kHz	10kHz	20%
gmro (diff)	23.092	20	-15.4%

Externally Compensated LDO with Gain = 2000

In this section, we have analyzed the performance of the LDO for an overall gain of 2000 in order to compare all the metrics with that of gain 1000.

The sizing of the FETs has been meticulously selected to achieve a trade-off between power efficiency, output current drive capability, and loop stability. The detailed sizing is mentioned below, ensuring alignment with the process node specifications and operational requirements of the circuit.

FET Sizes

Provided the dimensions of the passFET, differential amplifier, and current mirror transistors, including their small-signal parameters and figures of merit (FOMs). Additionally, analyze the loop gain behavior under both heavy-load and light-load conditions.

Table 12: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	267u/90n	10	48.88	37.35	27.1 GHz
Diff-Amp pmos	1.109u/135n	10	98.18	22.53	11.6 GHz
Diff-Amp nmos	0.414u/135n	10	93.59	60.29	29.9 GHz
Current Mirror nmos	1.607u/270n	10	155	31.11	8.3 GHz

Three different schematics are used for the underlying three cases

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

Stability Analysis

For Heavy load ($I_{load} = 10\text{mA}$) we get the following curve:

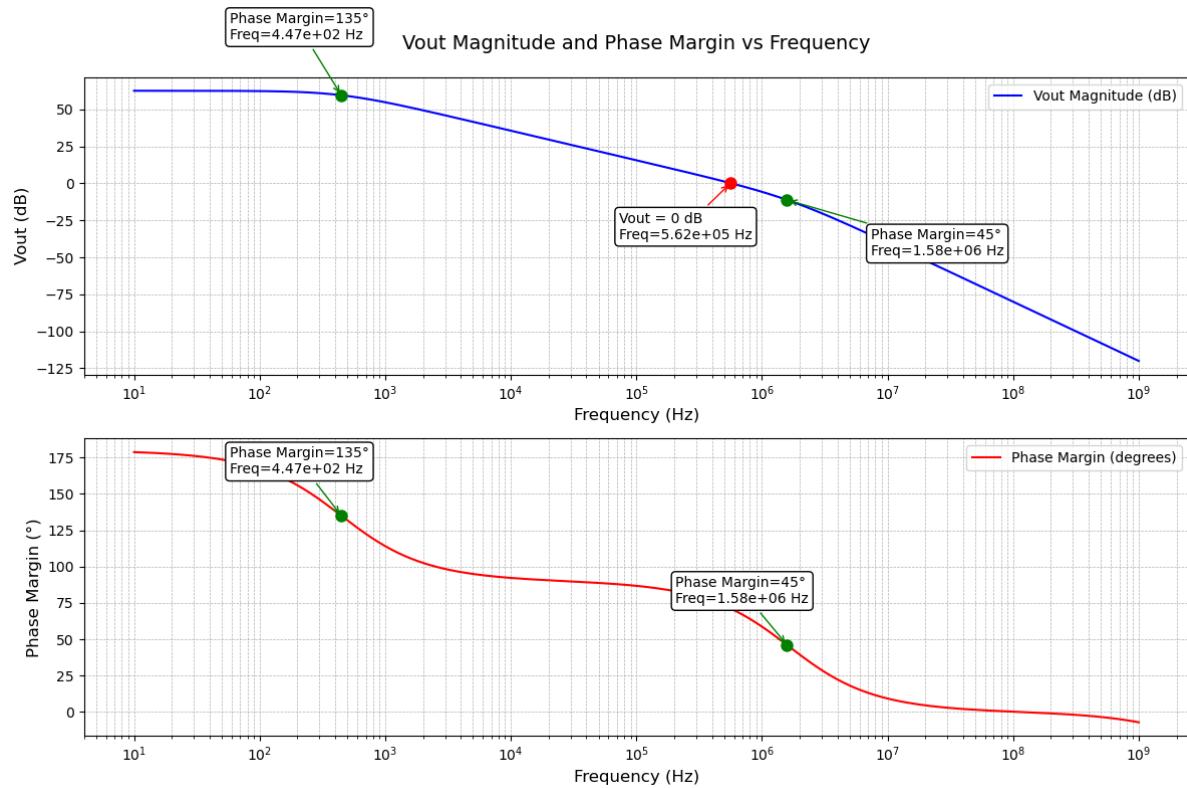


Figure 56: Stability Analysis

For Light load ($I_{load} = 2\text{mA}$) we get the following curve

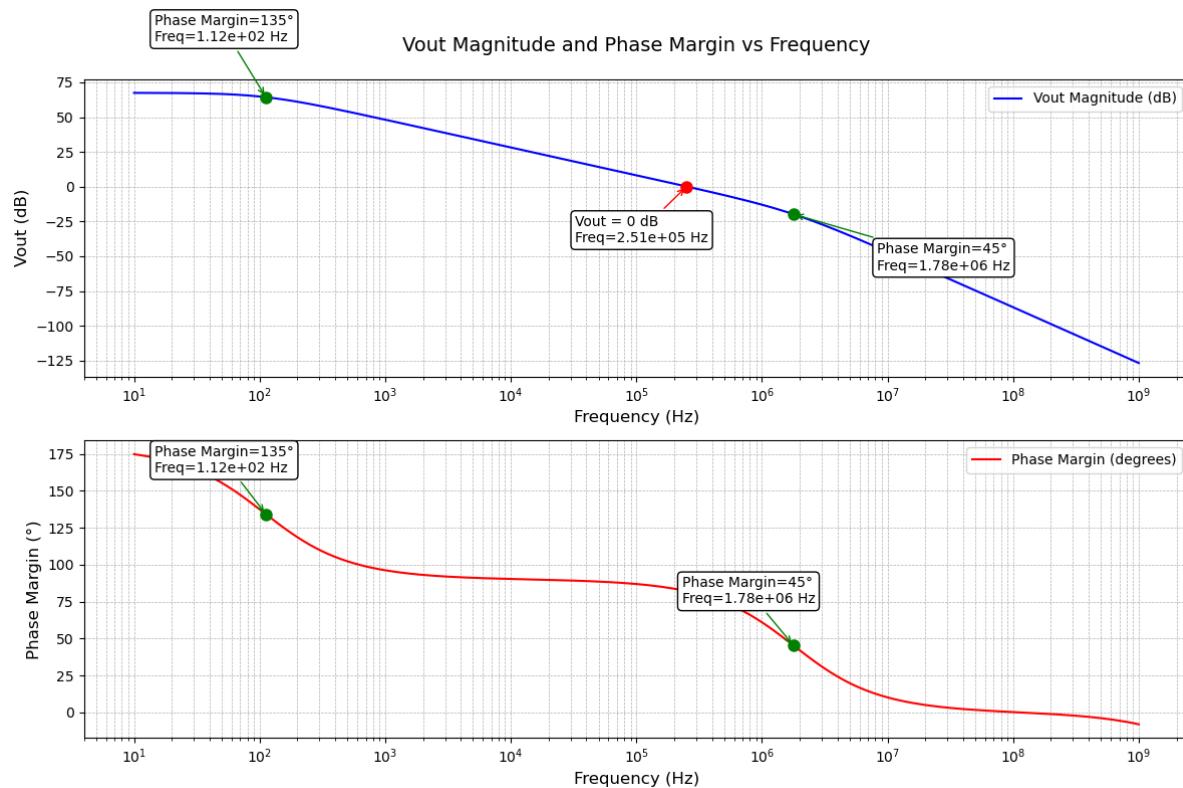


Figure 57: Stability Analysis

Light Load (2mA)

Schematic

Case 1:- Loop gain analysis:-

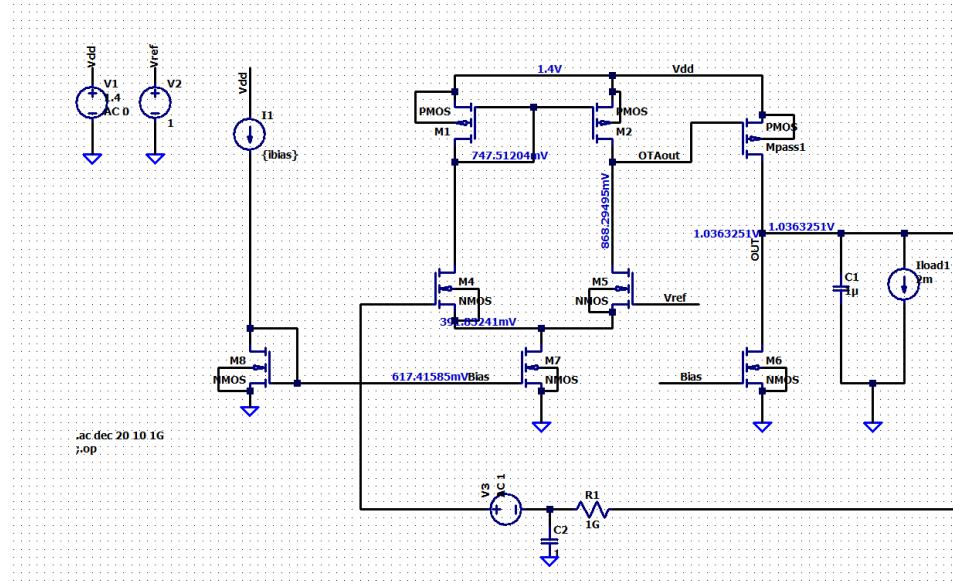


Figure 58: Schematic

Output Log File:-

--- BSIM4 MOSFETS ---					
Name:	m1	m2	mpass1	m3	m4
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-2.48e-05	-2.45e-05	-2.05e-03	2.48e-05	2.46e-05
Vgs:	-6.52e-01	-6.52e-01	-5.31e-01	6.11e-01	6.08e-01
Vds:	-6.52e-01	-5.31e-01	-3.98e-01	3.56e-01	4.77e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.89e-01	-4.90e-01	-4.87e-01	4.68e-01	4.68e-01
Vdsat:	-1.79e-01	-1.79e-01	-9.49e-02	1.53e-01	1.51e-01
Gm:	2.49e-04	2.47e-04	3.58e-02	2.46e-04	2.46e-04
Gds:	2.46e-06	2.65e-06	6.52e-04	3.03e-06	2.30e-06
Gmb:	5.27e-05	5.21e-05	7.39e-03	5.73e-05	5.73e-05
Cbd:	4.70e-16	4.82e-16	1.20e-13	1.87e-16	1.82e-16
Cbs:	8.87e-16	8.87e-16	2.14e-13	3.31e-16	3.31e-16
Name:	m5	m6	m7		
Model:	nmos	nmos	nmos		
Id:	5.08e-05	4.94e-05	5.00e-05		
Vgs:	6.17e-01	6.17e-01	6.17e-01		
Vds:	1.00e+00	3.92e-01	6.17e-01		
Vbs:	0.00e+00	0.00e+00	0.00e+00		
Vth:	4.69e-01	4.69e-01	4.69e-01		
Vdsat:	1.62e-01	1.61e-01	1.61e-01		
Gm:	5.08e-04	4.95e-04	5.01e-04		
Gds:	2.11e-06	3.27e-06	2.29e-06		
Gmb:	1.19e-04	1.16e-04	1.18e-04		
Cbd:	6.39e-16	7.20e-16	6.86e-16		
Cbs:	1.29e-15	1.29e-15	1.29e-15		

Figure 59: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.652	0.652	0.490	0.162	Saturation
Mpass	PMOS	0.398	0.531	0.487	0.044	Saturation
M4	NMOS	0.356	0.611	0.468	0.143	Saturation
M5	NMOS	0.477	0.608	0.468	0.140	Saturation
M6	NMOS	1.000	0.617	0.469	0.148	Saturation
M7	NMOS	0.392	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 13: Transistor Parameters and Operating Regions

Output on Python:-

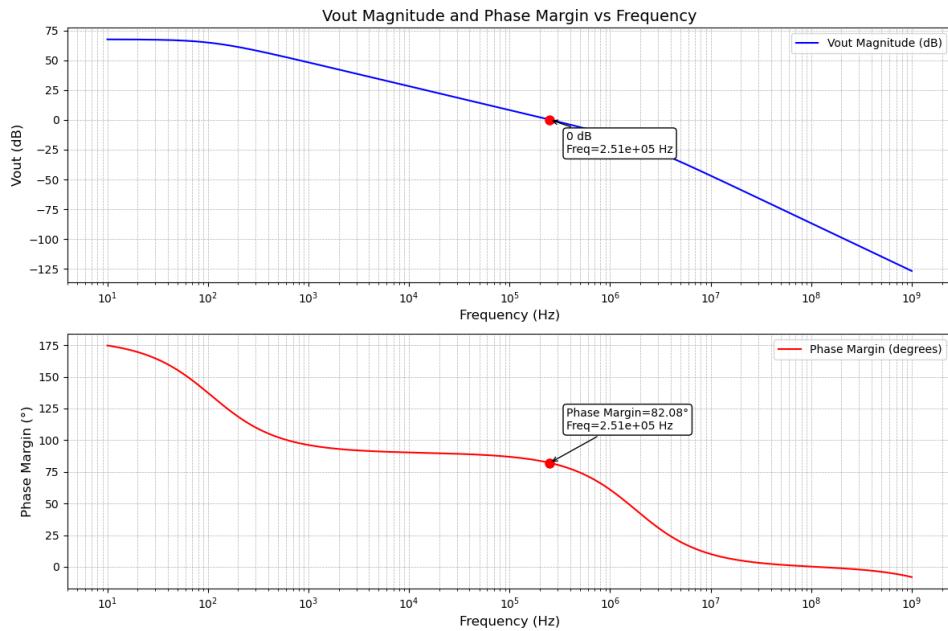


Figure 60: Vout and Phase Margin vs frequency

From above plot we can see Phase Margin = 82.08°

Case 2:- Open Loop PSRR calculation

Schematic

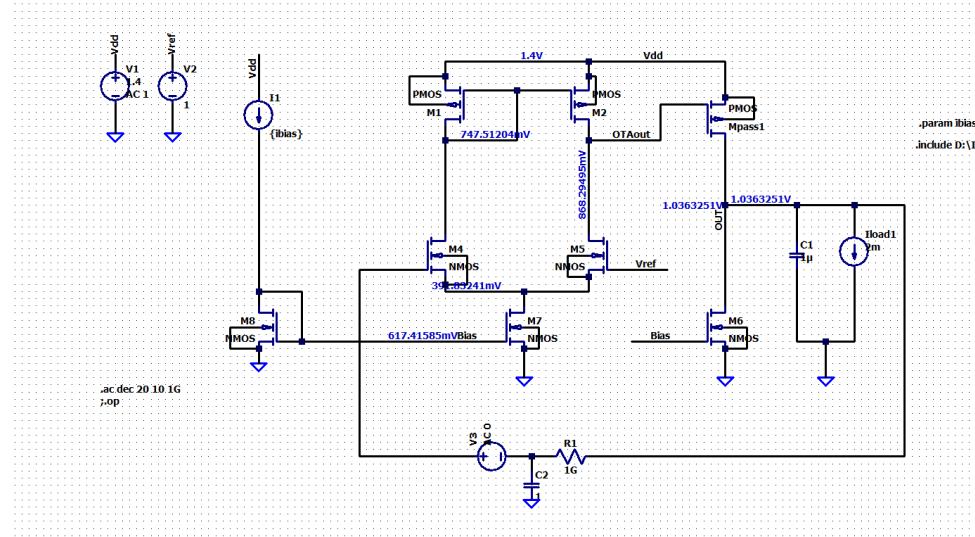


Figure 61: Schematic

Output on Python:-

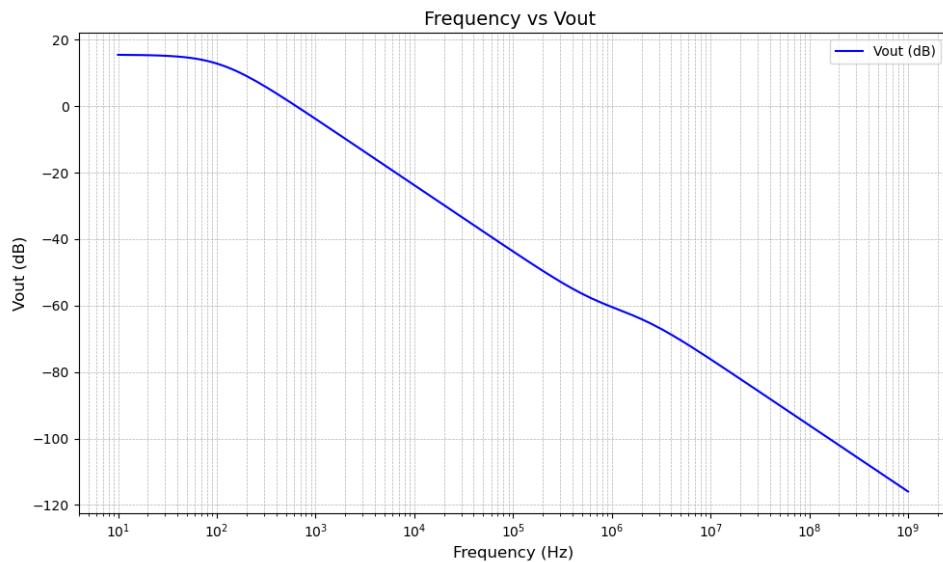


Figure 62: Vout vs frequency

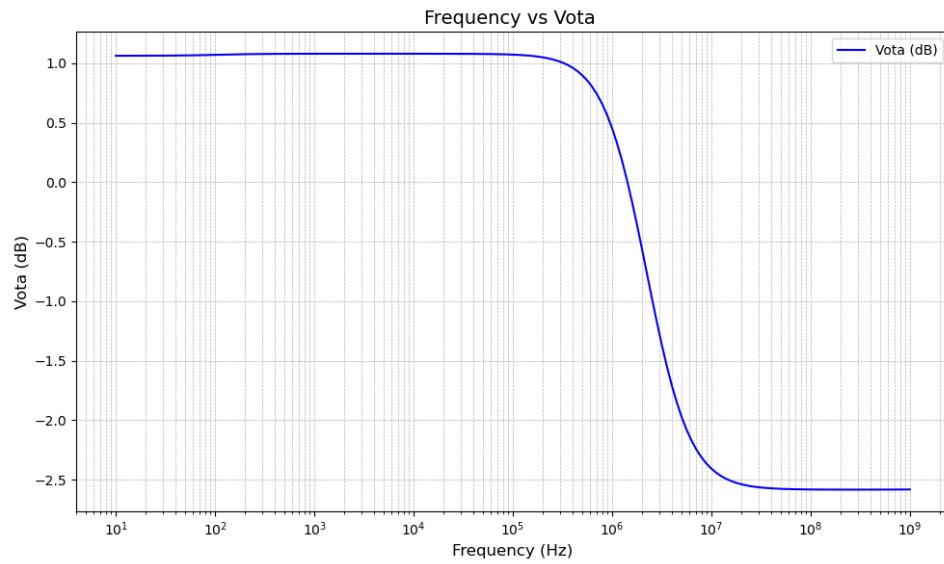


Figure 63: Vota vs frequency

Case 3:- Closed loop PSRR calculation

Schematic

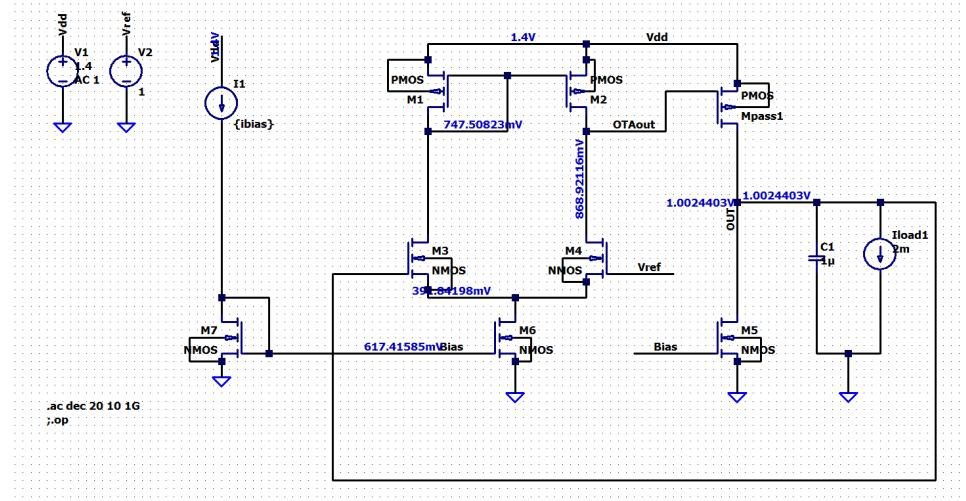


Figure 64: Schematic

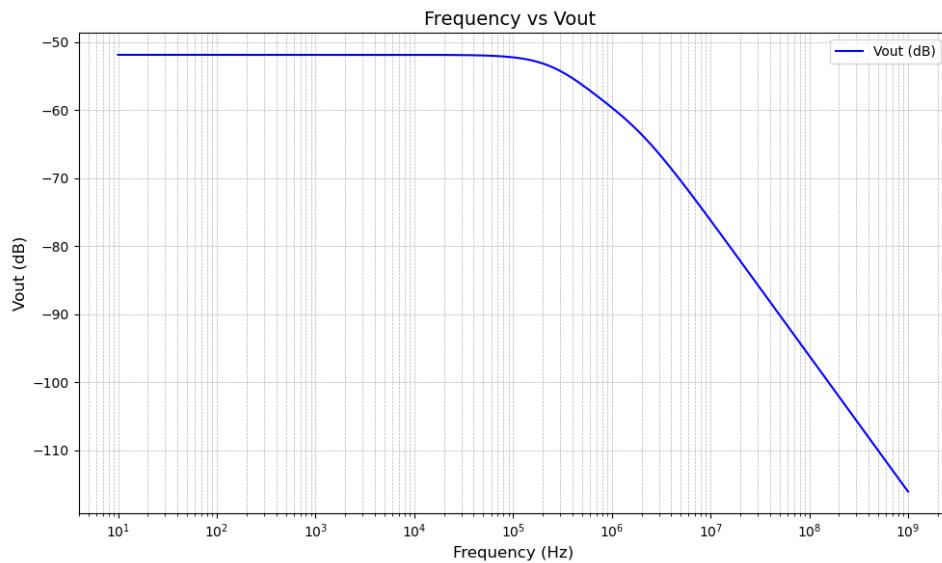
Output on Python:-

Figure 65: Vout vs frequency

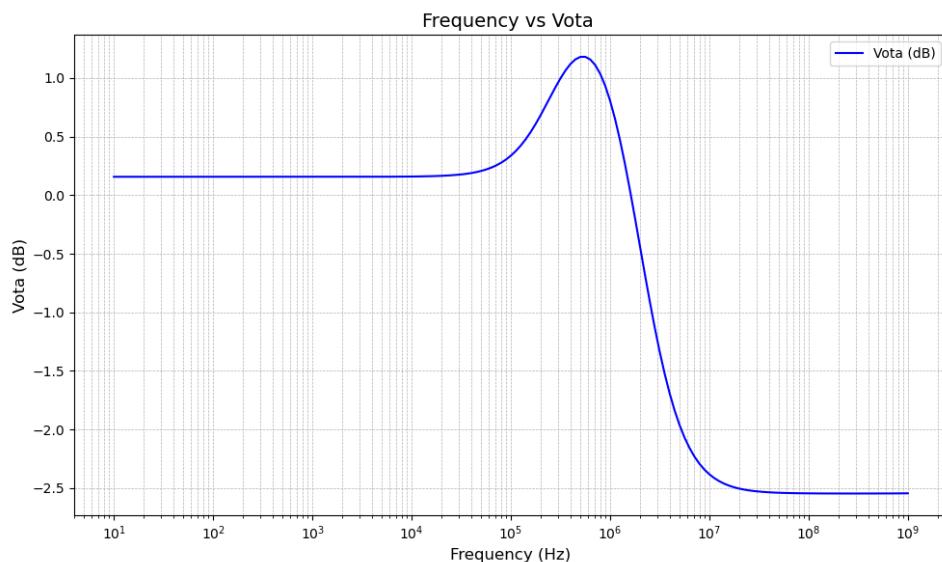


Figure 66: Vota vs frequency

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

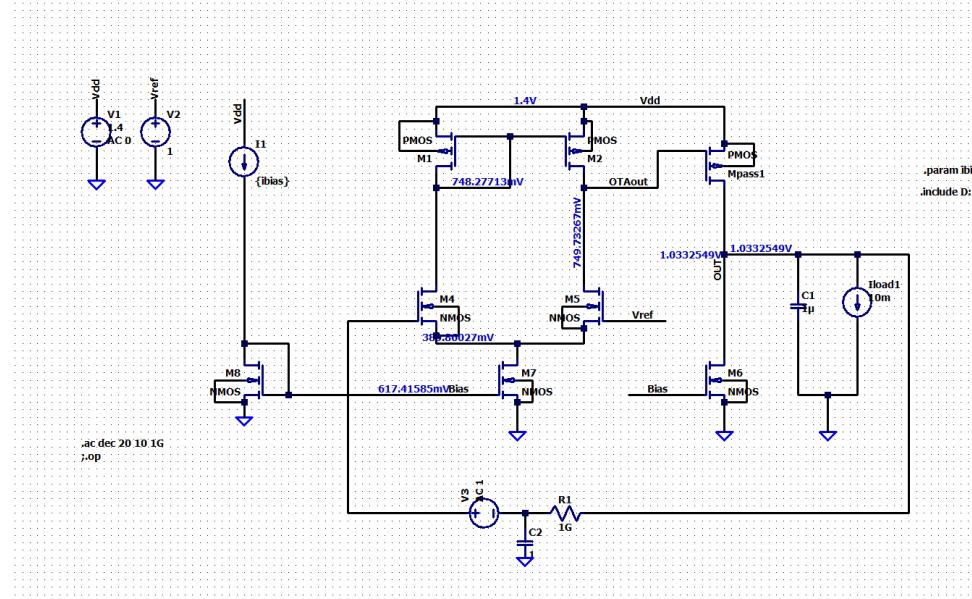


Figure 67: Schematic

Output Log File:-

--- BSIM4 MOSFETS ---					
Name:	m1	m2	mpass1	m3	m4
Model:	pmos	pmos	pmos	nmos	nmos
Id:	-2.47e-05	-2.46e-05	-1.01e-02	2.47e-05	2.47e-05
Vgs:	-6.52e-01	-6.52e-01	-6.49e-01	6.10e-01	6.10e-01
Vds:	-6.52e-01	-6.49e-01	-4.00e-01	3.58e-01	3.61e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.89e-01	-4.89e-01	-4.87e-01	4.68e-01	4.68e-01
Vdsat:	-1.78e-01	-1.78e-01	-1.77e-01	1.52e-01	1.52e-01
Gm:	2.48e-04	2.48e-04	9.91e-02	2.45e-04	2.46e-04
Gds:	2.45e-06	2.45e-06	2.46e-03	2.97e-06	2.96e-06
Gmb:	5.25e-05	5.25e-05	2.10e-02	5.71e-05	5.72e-05
Cbd:	4.70e-16	4.70e-16	1.19e-13	1.87e-16	1.87e-16
Cbs:	8.87e-16	8.87e-16	2.14e-13	3.31e-16	3.31e-16
Name:	m5	m6	m7		
Model:	nmos	nmos	nmos		
Id:	5.08e-05	4.94e-05	5.00e-05		
Vgs:	6.17e-01	6.17e-01	6.17e-01		
Vds:	1.00e+00	3.90e-01	6.17e-01		
Vbs:	0.00e+00	0.00e+00	0.00e+00		
Vth:	4.69e-01	4.69e-01	4.69e-01		
Vdsat:	1.62e-01	1.61e-01	1.61e-01		
Gm:	5.08e-04	4.95e-04	5.01e-04		
Gds:	2.11e-06	3.29e-06	2.29e-06		
Gmb:	1.19e-04	1.16e-04	1.18e-04		
Cbd:	6.39e-16	7.21e-16	6.86e-16		
Cbs:	1.29e-15	1.29e-15	1.29e-15		

Figure 68: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.649	0.652	0.489	0.163	Saturation
Mpass	PMOS	0.400	0.649	0.487	0.162	Saturation
M4	NMOS	0.358	0.610	0.468	0.142	Saturation
M5	NMOS	0.361	0.610	0.468	0.142	Saturation
M6	NMOS	1.000	0.617	0.469	0.148	Saturation
M7	NMOS	0.390	0.617	0.469	0.148	Saturation
M8	NMOS	0.617	0.617	0.469	0.148	Saturation

Table 14: Updated Transistor Parameters and Operating Regions

Output on Python:-

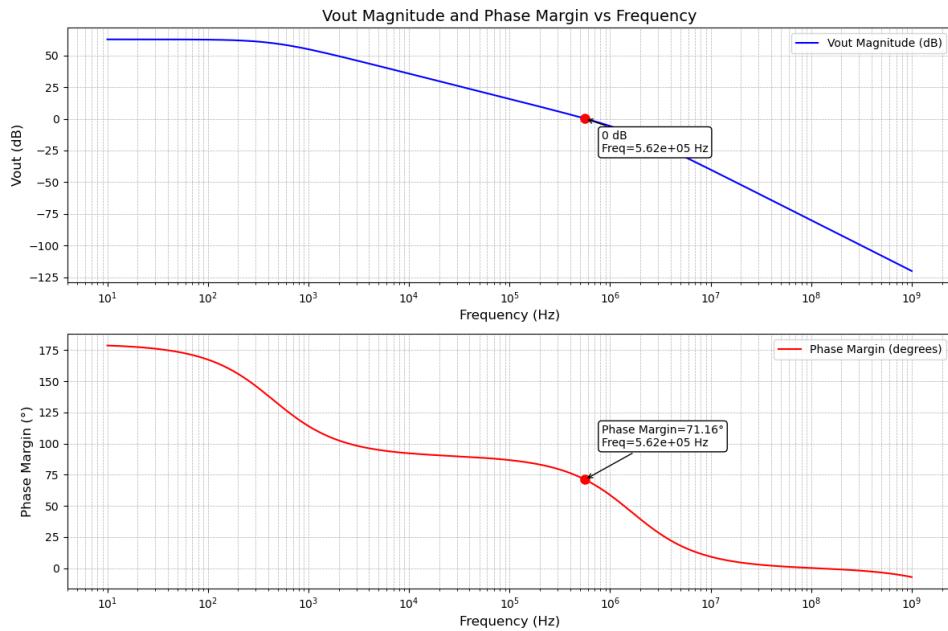


Figure 69: Vout and Phase Margin vs frequency

From above plot we can see Phase Margin = 71.16°

Case 2:- Open Loop PSRR calculation

Schematic

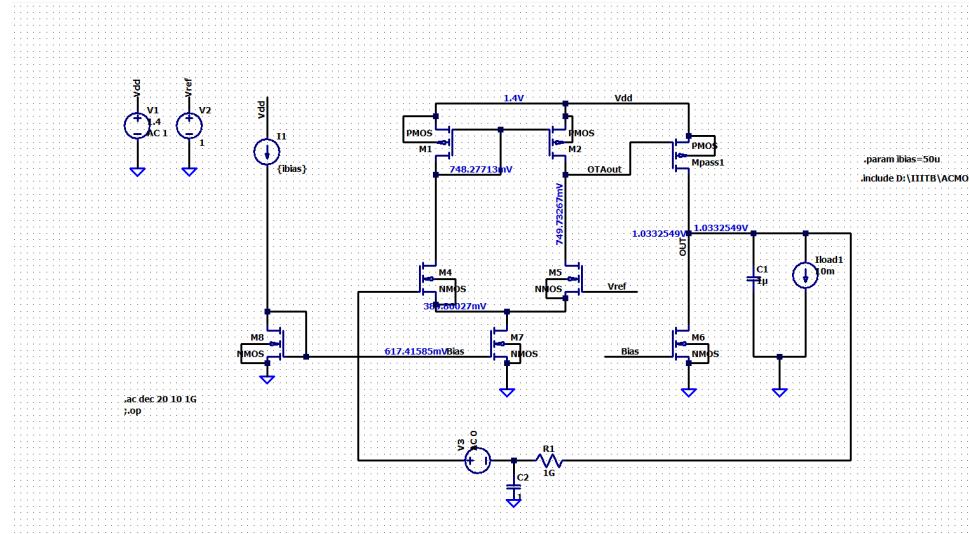


Figure 70: Schematic

Output on Python:-

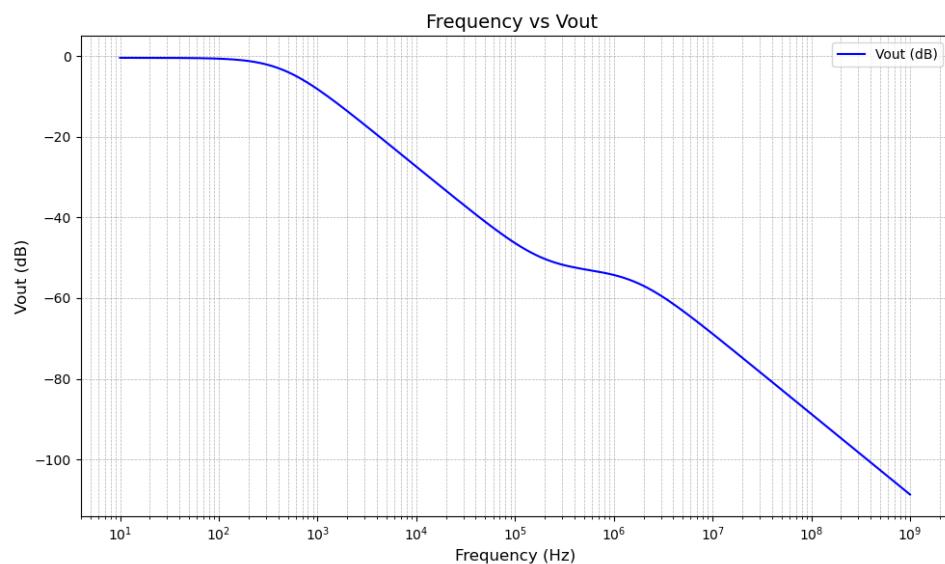


Figure 71: Vout vs frequency

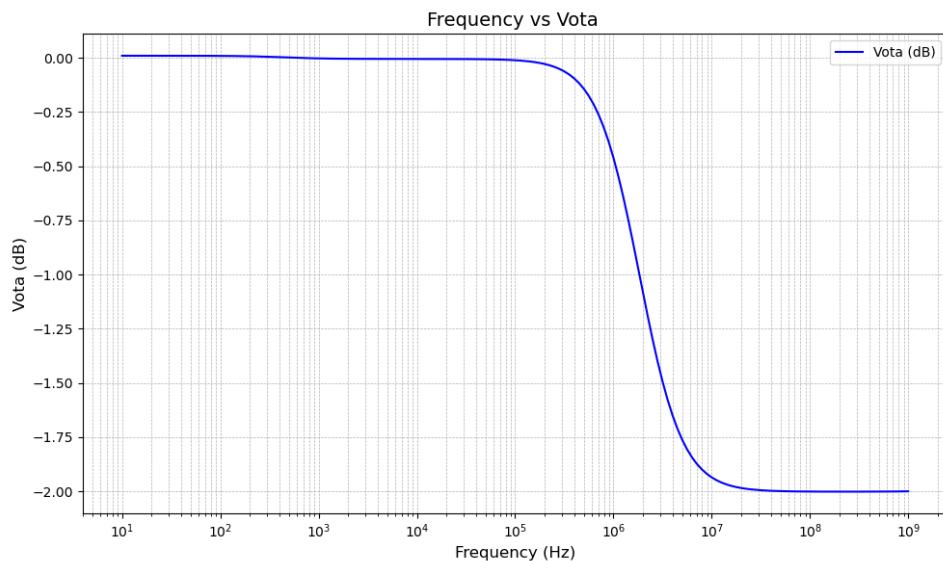


Figure 72: Vota vs frequency

Case 3:- Closed loop PSRR calculation

Schematic

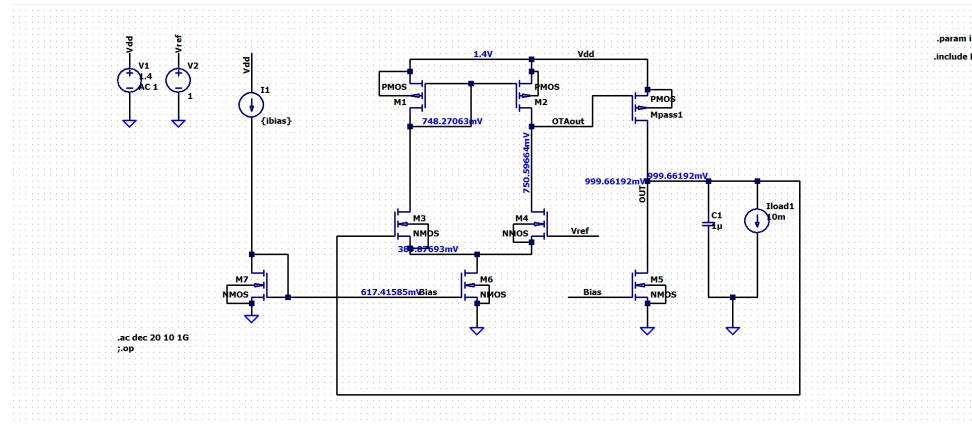


Figure 73: Schematic

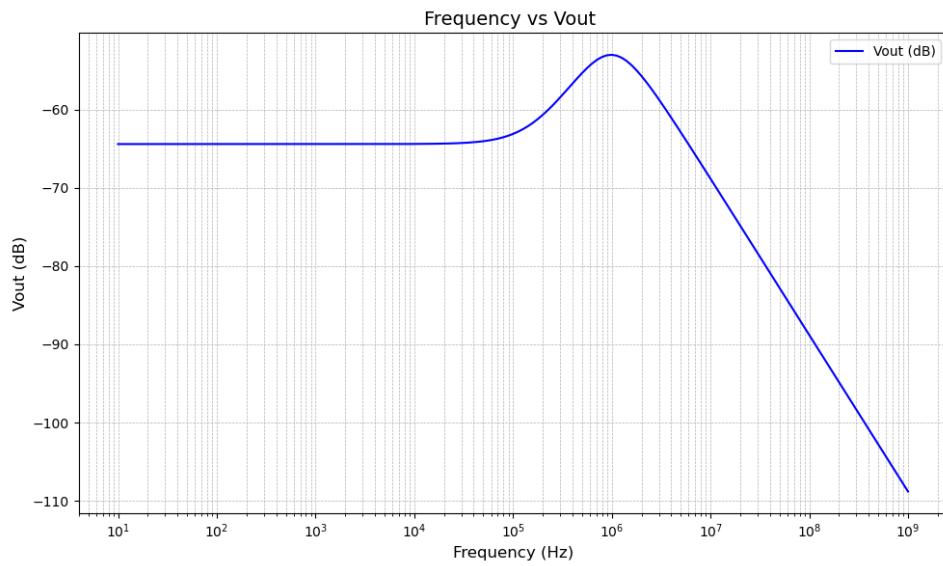
Output on Python:-

Figure 74: Vout vs frequency

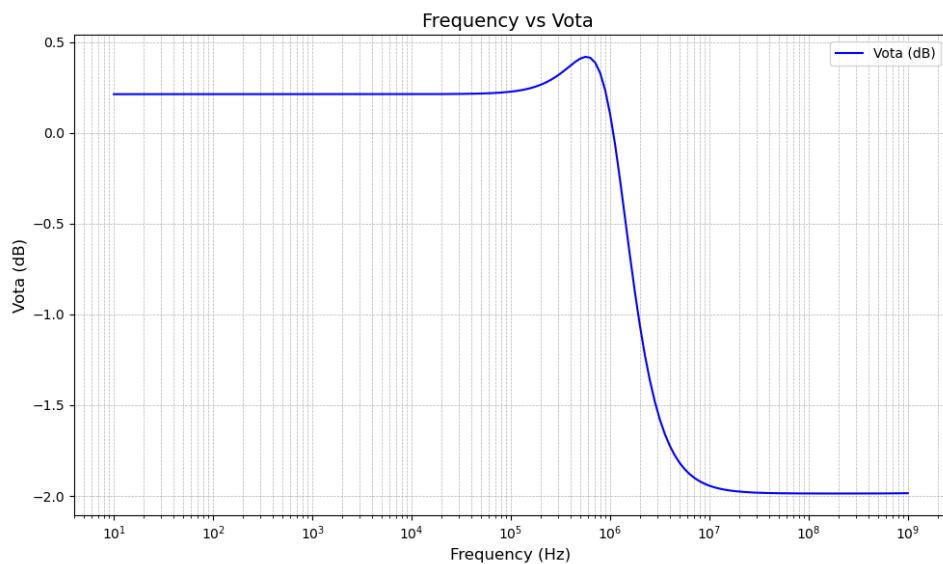


Figure 75: Vota vs frequency

Transient Analysis

Schematic

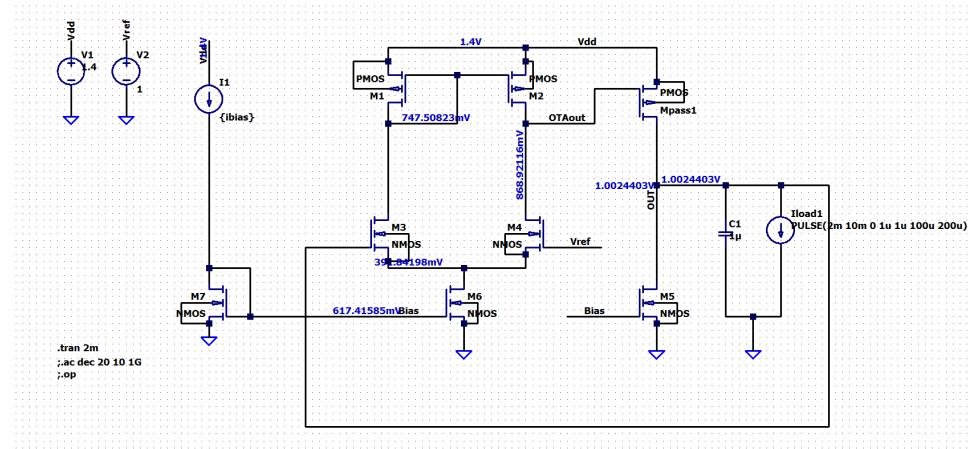


Figure 76: Schematic

Output on Python:-

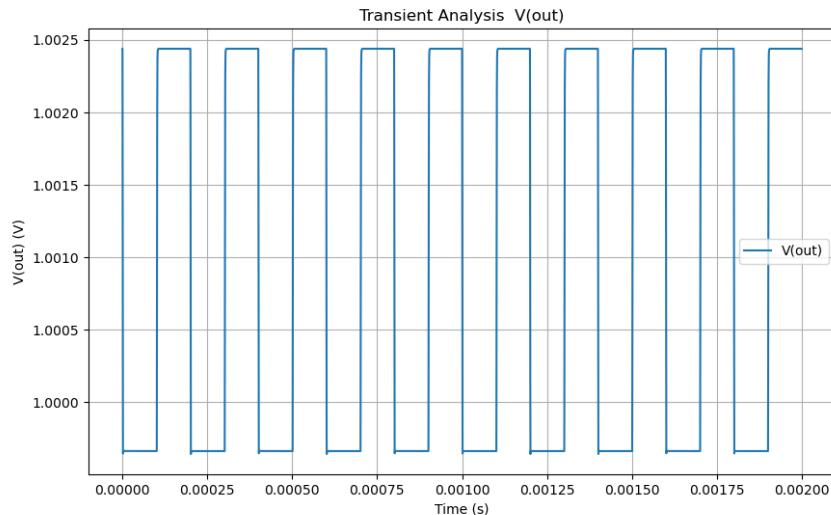


Figure 77: Vout vs time

Output on Python:-

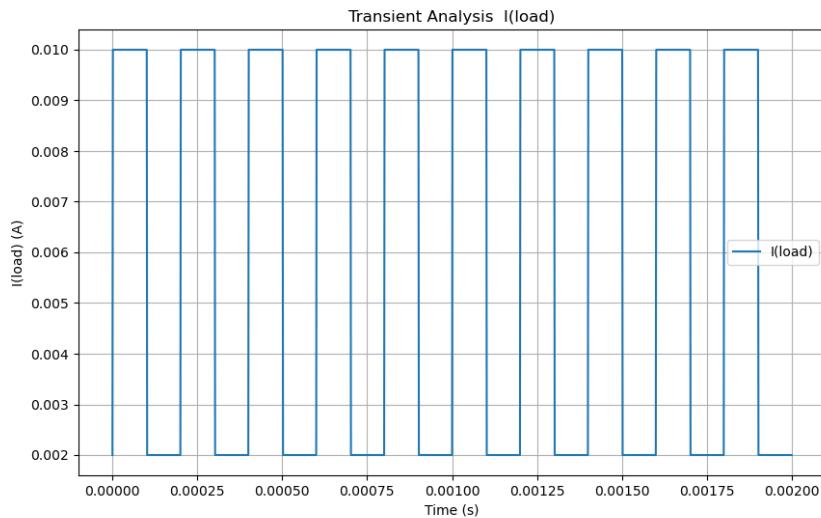


Figure 78: Iload vs time

Observations from Externally Compensated LDOs for gains 1000 and 2000 respectively:

Comparison of various metrics:

PARAMETER	GAIN =1000	GAIN=2000	UNITS	trend
Area	2.55E-11	2.58E-11	m2	
CLOSELOOP PSRR HIGH LOAD	-59.82	-64.48	db	INCREASED
CLOSE LOOP PSRR LOW LOAD	-49.8	-52		INCREASED
OPEN LOOP GAIN LOW LOAD	62.4	67.544		
POLE1 LOW LOAD	102.119	107.568hz		
POLE2 LOW LOAD	3230000	1700000		
wugb LOW LOAD	136600	257800		
PHASE MARGIN LOWLOAD	87.654	81.86		DECREASED
OPEN LOOP GAIN HIGH LOAD	58.49	62.356		
POLE1 HIGHLOAD	411.36	432.9	Hz	
POLE2 HIGHLOAD	2800000	1611000		
WUGBHIGLOAD	346000	550000		
PHASEMARGIN HIGHLOAD	83.3	71.5		DECREASED

Figure 79: Comparison of various metrics