Self Oscillating Voltage Doubler using 5 stage cascaded ring oscillators and flying capacitors for Energy Harvester

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***Abstract*—This paper explains the design of a Self-Oscillating Voltage Doubler circuit. This doubler circuit is designed using cascaded ring oscillators in a five-stage configuration with flying capacitors connected between the stages. The circuit, operating with a test input voltage of 1 V, achieves a peak efficiency of around 83% while supporting a load current of 0.22 mA. NMOS and PMOS FETs used in the design are based on the 45 nm technology node from the `gpdk45` analog library.**

***Index Terms*—Voltage Doubler, Self-Oscillating, Flying Capacitor, Switched Capacitor, Energy Harvester**

I. Introduction

This project focuses on designing a self oscillating voltage doubler [1] circuit. The main goal is to create a circuit that can take a small input voltage and increase it using a self-oscillating switched-capacitor voltage doubler. This circuit uses a five-stage ring oscillator and flying capacitors to boost the voltage. It is designed using the 45 nm technology node with the `gpdk45` analog library in Cadence Virtuoso and tested under different load and no-load conditions with an input test voltage of 1 V.

Boost DC-DC converters are widely used to harvest energy from DC sources due to their high conversion efficiency. However, they require a large off-chip inductor at low harvested power levels, which increases the overall system size. This makes them less suitable for compact or integrated applications.

Alternatively, switched-capacitor (SC) DC-DC converters can be fully integrated on-chip and are preferred for form-factor-constrained systems. However, at low power levels, the efficiency of SC converters is limited by the overheads of clock generation and level conversion required to drive the switches. As a result, efficient SC converter operation has typically been restricted to the microwatt (μW) range.

This paper presents a cascaded self-oscillating voltage doubler architecture that can be used in fully integrated switched-capacitor energy harvesters [2]. In each voltage doubler stage, the oscillator is completely internalized, significantly reducing the power overhead associated with clock generation and level shifting. This reduction in overhead enables the harvester to operate efficiently even with very weak power sources, as low as a few nanowatts (nW).

The design is suitable for small electronic devices that operate with minimal power, such as sensors or medical devices in wearables or other personal electronics. The inverter circuit used in the doubler follows a 2:1 sizing ratio, meaning the PMOS width is twice that of the NMOS. By parameterizing the widths of the NMOS and PMOS transistors and the capacitance of the flying capacitors, optimal values were determined. Using these values, the voltage doubler achieved an output voltage of up to 1.83 V from a 1 V input. The design reached a peak efficiency of 83% under no-load conditions and maintained 64% efficiency under a 0.22 mA load, making it a strong candidate for future low-power applications.

Section II describes the system overview and design outline, detailing the components used and the design specifications. Section III presents the analog circuit design of the ring oscillator and voltage doubler. Section IV discusses the simulation results. Section V provides the further steps and conclusion.

II. System Overview and Design Outline

The proposed voltage doubler consists of two main blocks: the ring oscillator and flying capacitors. Together, they form the complete self-oscillating voltage doubler circuit. Each component is described in detail below.

A. Ring Oscillator

A ring oscillator is an electronic circuit that produces a repeating signal, or oscillation, without the need for an external clock. It consists of an odd number of inverters (e.g., 3, 5, or 7) connected in a loop, where the output of the last inverter is fed back to the input of the first. With an initial condition, the signal continuously flips between high and low as it travels through the inverters, creating a periodic waveform.

In this project, a five-stage ring oscillator is used in the voltage doubler. Unlike a standard ring oscillator, the inverters here are connected in a cascaded manner, resulting in a total of 10 inverters. The signal delay through each inverter causes the output to change over time, generating oscillation. The

frequency of oscillation depends on the number of stages and the delay of each inverter—more stages typically result in a lower frequency.

B. Flying Capacitors

Flying capacitors are used to transfer electric charge from one part of the circuit to another. As the name suggests, these capacitors are not fixed to a single voltage level but instead "fly" between different nodes during operation. In this project, they are placed at the output of each inverter stage to gradually increase the output voltage.

These capacitors charge during one phase of the signal and transfer that charge to the next stage in the following phase. This step-by-step charge transfer boosts the voltage without requiring bulky inductors. Flying capacitors are ideal for low-power, compact designs and are easy to integrate on-chip. In this design, they play a key role in enabling the voltage doubler to work efficiently with an energy harvester.

C. Self-Oscillating Voltage Doubler

A voltage doubler is a circuit that increases the input voltage to nearly twice its value. It is especially useful in low-power systems where only a small input voltage is available. In this project, the voltage doubler is built using a five-stage self-oscillating ring oscillator and flying capacitors.

The ring oscillator generates a periodic signal that controls the timing of the circuit. The flying capacitors use this signal to move charge from one stage to the next, gradually increasing the voltage. This method avoids the need for inductors, making the design more compact and suitable for integration.

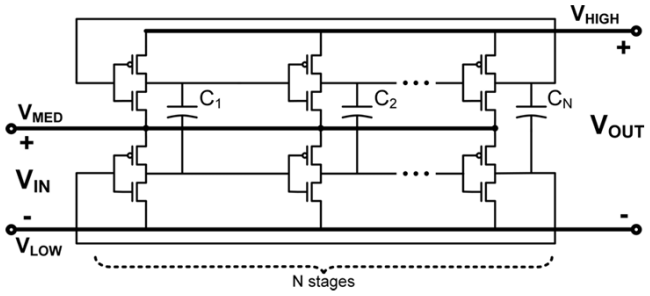

Fig. 1. Basic Structure of proposed Self Oscillating Voltage Doubler

The voltage doubler operates with a 1 V input and can increase the output to around 1.8 V, depending on the load. The detailed circuit design is discussed in Section III, and the simulation results are presented in Section IV.

III. Analog Circuit Design

A. Ring Oscillator

The analog design process began with the implementation of basic ring oscillator circuits, which play a crucial role in our system by eliminating the need for external clock sources. Ring oscillators enable self-sustained operation, which is essential for ultra-low-power energy harvesting applications.

We initially designed 3-stage and 5-stage CMOS ring oscillators using the `GPDK045` (45 nm) technology node. These were implemented with a standard inverter-based topology. Transient simulations were performed to observe the oscillatory behavior, including high and low voltage levels at the output node. To ensure proper startup, the output node was initialized to 0 V.

To improve circuit performance, we carried out parametric analysis by sweeping the transistor width-to-length (W/L) ratios. This helped us analyze how sizing impacts the oscillation frequency and voltage swing. Based on these results, we determined an optimum sizing that provided stable oscillation with minimal power consumption.

After verifying the behavior of standalone ring oscillators, we moved on to implement the self-oscillating voltage doubler. This circuit integrates two stacked ring oscillators connected through flying capacitors. The flying capacitors allow charge transfer between the stages, enabling step-wise voltage boosting.

B. Self-Oscillating Voltage Doubler

The self-oscillating voltage doubler was implemented using the `GPDK045` (45 nm) technology node, following the initial design and validation of standalone ring oscillators. This circuit forms the core of the energy harvester and enables autonomous voltage up-conversion without any external clocking mechanism.

To ensure stable and efficient operation, we performed parametric analysis on transistor sizing. A ratio of 2W:1W was maintained for PMOS to NMOS transistors in the ring oscillator stages, where W (width) was parametrized. Various widths were simulated to study their impact on output voltage swing, startup behavior, and power efficiency.

The value of flying capacitors—used for charge transfer between the stacked oscillators—was also parametrized. These capacitors play a crucial role in energy transfer and output voltage build-up. Simulations were conducted to observe how different capacitance values affected performance under varying load conditions.

The circuit was first tested under no-load conditions to validate startup and self-oscillation behavior. Once confirmed, the load current was gradually increased. The output voltage and efficiency were monitored, and the circuit exhibited optimum performance up to a load of approximately 50 µA with the initial sizing.

To further improve efficiency at higher load currents, we repeated the parametric analysis with increased transistor widths and flying capacitor values. This adjustment allowed the circuit to maintain stable operation and achieve optimum efficiency up to a maximum load current of 0.22 mA.

IV. Simulation and Results

After completing the design of the self-oscillating voltage doubler circuit, a detailed parametric analysis was conducted to optimize its performance under varying load conditions. The simulations were carried out using *Cadence Virtuoso*, focusing

on two key parameters: the capacitance of the flying capacitors and the width of the PMOS and NMOS transistors. These parameters were varied to support load currents ranging from 50 µA to 0.22 mA.

To ensure accurate transient behavior, the initial condition of the output node was set to 0 V, allowing the circuit to naturally reach its steady-state oscillation. Two configurations were tested: one with $C_{\text{fly}} = 100$ fF and transistor width $w = 600$ nm, and another with $C_{\text{fly}} = 10$ pF and $w = 2$ µm. The results showed that the circuit could achieve an output voltage of up to 1.83 V from a 1 V input, with efficiencies of up to 83% without load and 64% under a 0.22 mA load. These results demonstrate the circuit's suitability for low-power energy harvesting applications.

Below is the output waveform obtained for five stage ring oscillator.

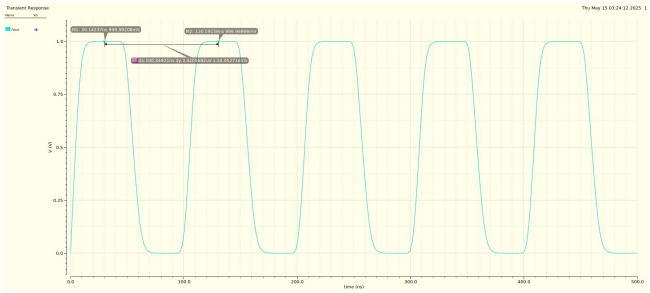

Fig. 2. Five Stage Ring Oscillator Output Waveform

Below is the table and respective voltage waveform for lower load current of up to 50 µA.

TABLE I
VOLTAGE DOUBLER ANALYSIS WITH CFLY = 100 FF AND W = 600 NM

Parameter	Without Load	With Load (50 µA)
Sizing PMOS:NMOS	2w:1w	2w:1w
C_{fly}	100 fF	100 fF
V_{in}	1 V	1 V
V_{out}	1.81 V	1.69 V
Efficiency	81%	69%

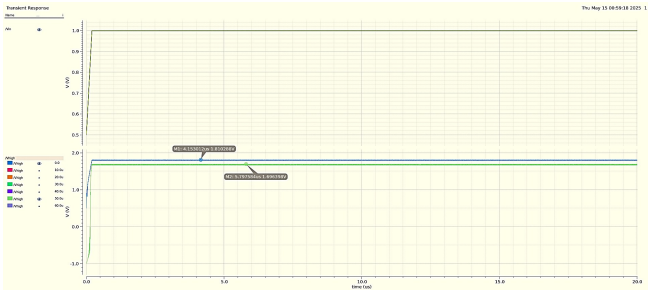

Fig. 3. Output waveform of the voltage doubler with load current = 50 µA, $C_{\text{fly}} = 100$ fF, PMOS:NMOS = 2w:1w, $w = 600$ nm

Below is the table and respective voltage waveform for higher load current of up to 0.22 mA.

TABLE II
VOLTAGE DOUBLER ANALYSIS WITH CFLY = 10 PF AND W = 2 µM

Parameter	Without Load	With Load (0.22 mA)
Sizing PMOS:NMOS	2w:1w	2w:1w
C_{fly}	10 pF	10 pF
V_{in}	1 V	1 V
V_{out}	1.83 V	1.64 V
Efficiency	83%	64%

Fig. 4. Output waveform of the voltage doubler with load current = 0.22 mA, $C_{\text{fly}} = 10$ pF, PMOS:NMOS = 2w:1w, $w = 2$ µm

V. FURTHER STEPS AND CONCLUSION

A. Further Steps

To further improve the performance of the voltage doubler, future work will focus on the following:

- Exploring newer technology nodes to reduce power consumption and improve efficiency.
- Using transistors with lower threshold voltages to enhance performance at lower input voltages.
- Integrating the voltage doubler with other components of the energy harvester to build a complete system.
- Optimizing the layout for area and power to achieve energy harvesting in the nanowatt range.

B. Conclusion

In this project, a self-oscillating voltage doubler circuit was successfully designed and simulated using *Cadence Virtuoso*. The design was optimized through parametric analysis by varying the transistor widths and flying capacitor values to support different load conditions. The circuit achieved an output voltage of up to 1.83 V from a 1 V input, with a peak efficiency of 83% under no-load and 64% under a 0.22 mA load. These results demonstrate the effectiveness of the proposed architecture for low-power energy harvesting applications.

REFERENCES

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