International Institute of Information Technology Bangalore

VLS 804-Analog Power ICs

A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter

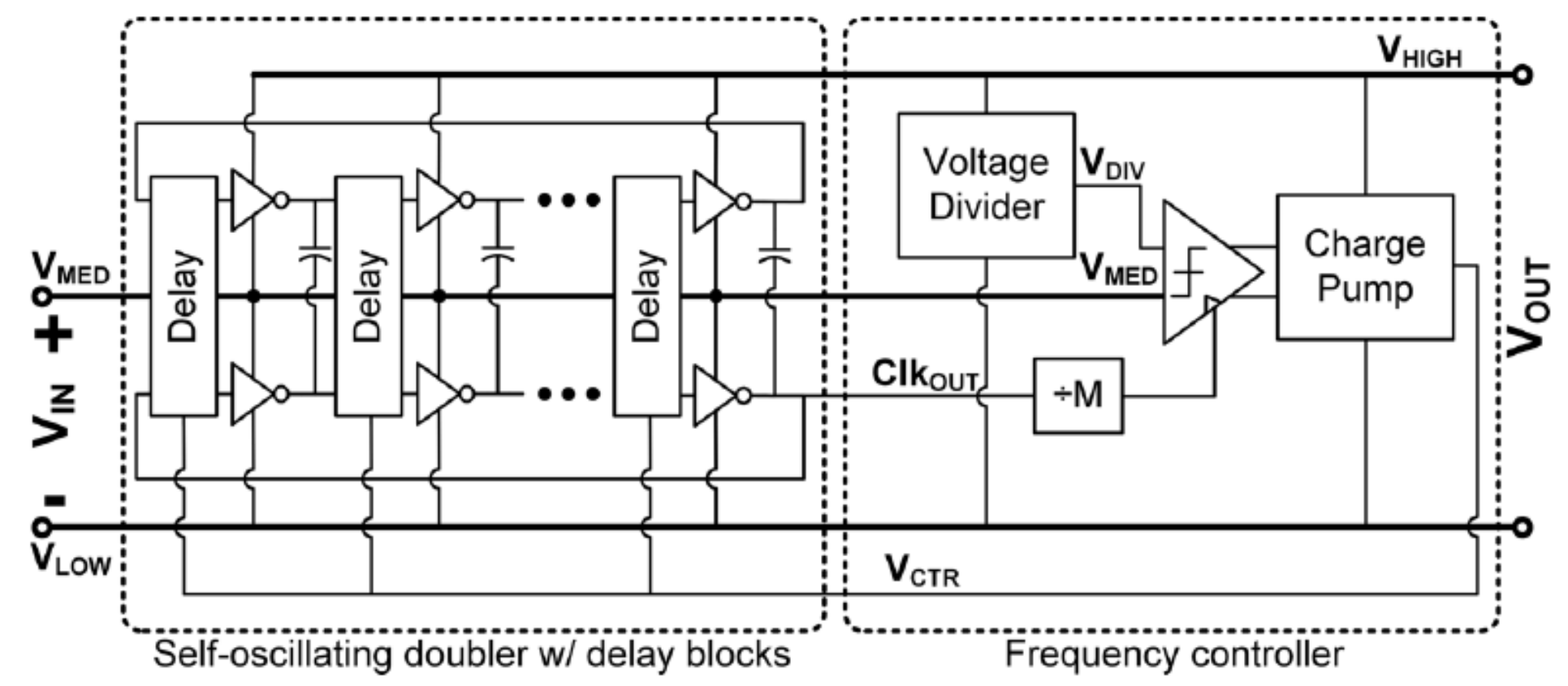
Submitted by:
Nikhil Bhusari - MT2024522
Talakokkula Karthik Satyanarayana - MT2024536

Instructor : Prof. Sakshi Arora

Introduction

- Design Problem: Design self oscillating voltage doubler circuit using cascaded ring oscillators and flying capacitors. The ring oscillator is a five stage circuit cascaded in nature.
- Relevance: The designed voltage doubler will be used as a basic block to further multiply the input voltage up to 16 times with different voltage rails and oxide thickness to thereby design the low power harvester circuit.
- Design Specifications:
- Input Test Voltage: 1V
- Operating Temperature from -40°C to 125°C
- Architecture: Self Oscillating Voltage Doubler
- Technology Node: 45nm

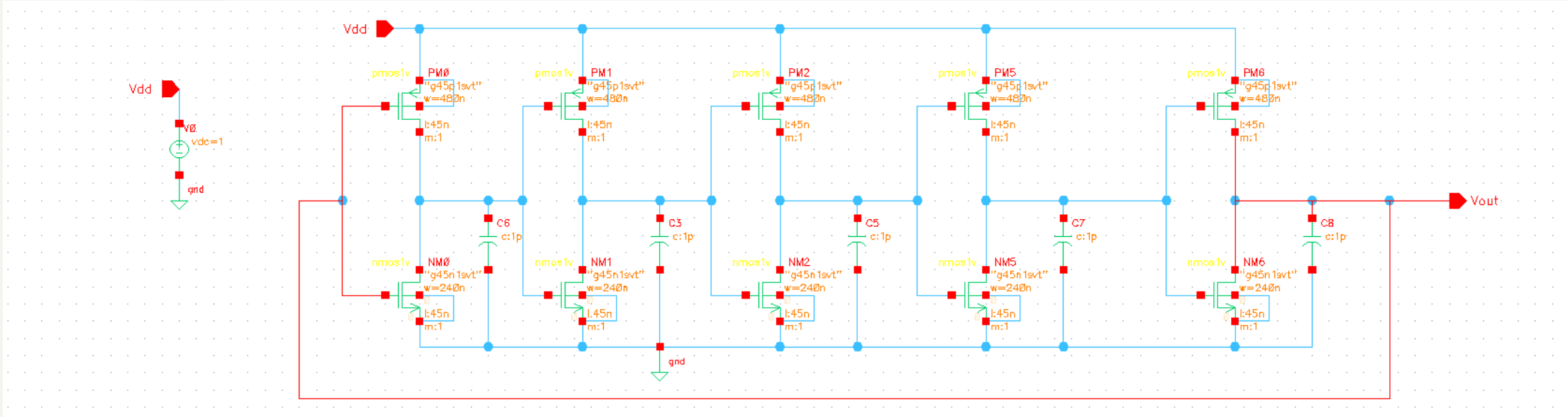
Design Outline – Block Diagram



Design Outline – Block Description

- Voltage Doubler: This circuit is a 5 stage cascaded self oscillating ring oscillator along with the flying capacitors which takes the input voltage at the lower level of inverters and doubles the voltage thereby the output voltage is taken at the higher inverter rails.
- Charge Pump: This circuit takes in the corresponding pull-up/pull-down signals, and adjusts VCON as needed to either speed or slow the oscillation
- Voltage Divider: This circuit uses the principle of voltage division and helps to divide the voltage into desired voltage with the help of series of resistors or capacitors.

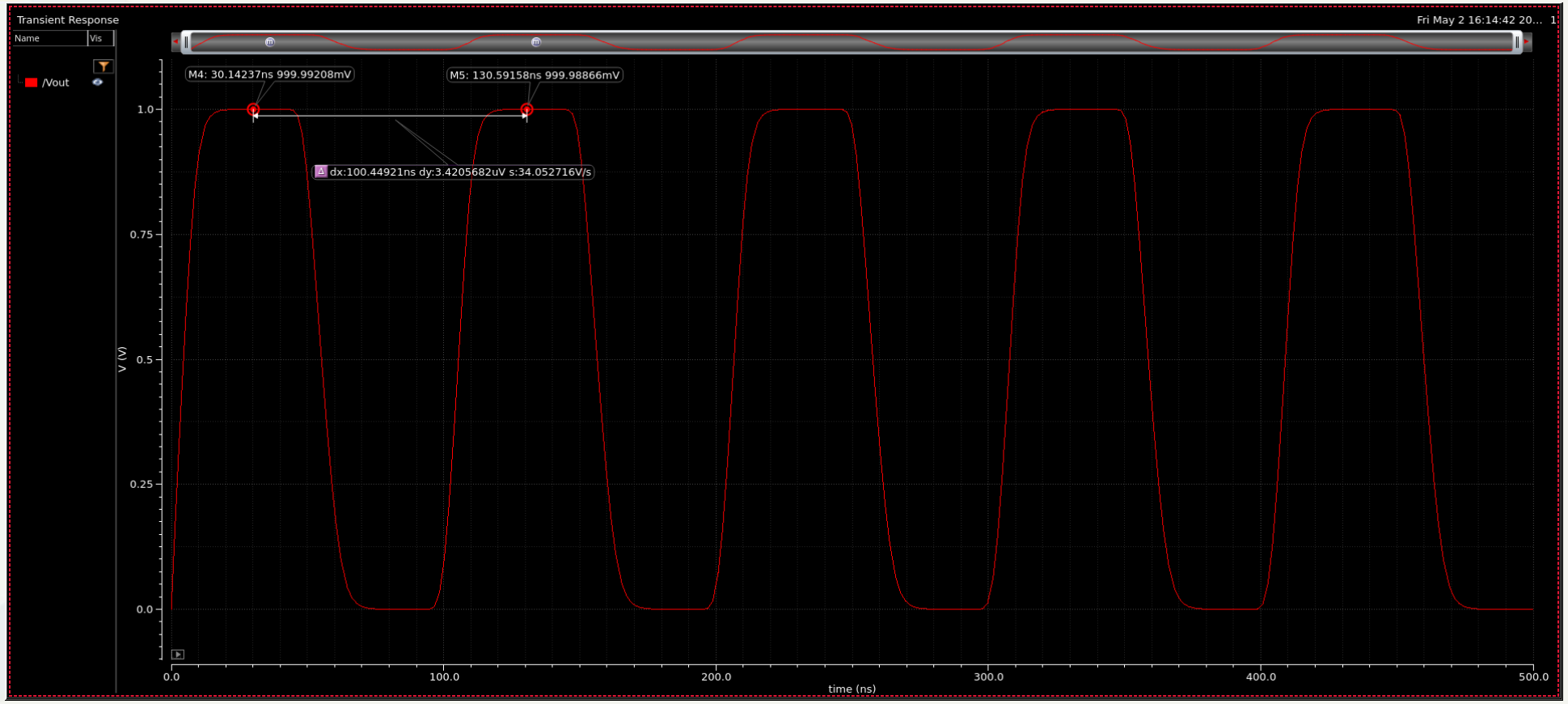
Core Design
Step I: Ring Oscillator – Schematic



5 Stage Ring Oscillator
Sizing of transistors: NMOS – 480nm PMOS – 240nm

Observation: As we increase the number of stages in the ring oscillator the frequency of oscillation at the output decreases (in this case we are able to observe the stable 1 and 0 values at the output node).

Core Design
Step I: Ring Oscillator – Output Waveform



Time Period – 30.14ns
Frequency of oscillation – 33.18MHz

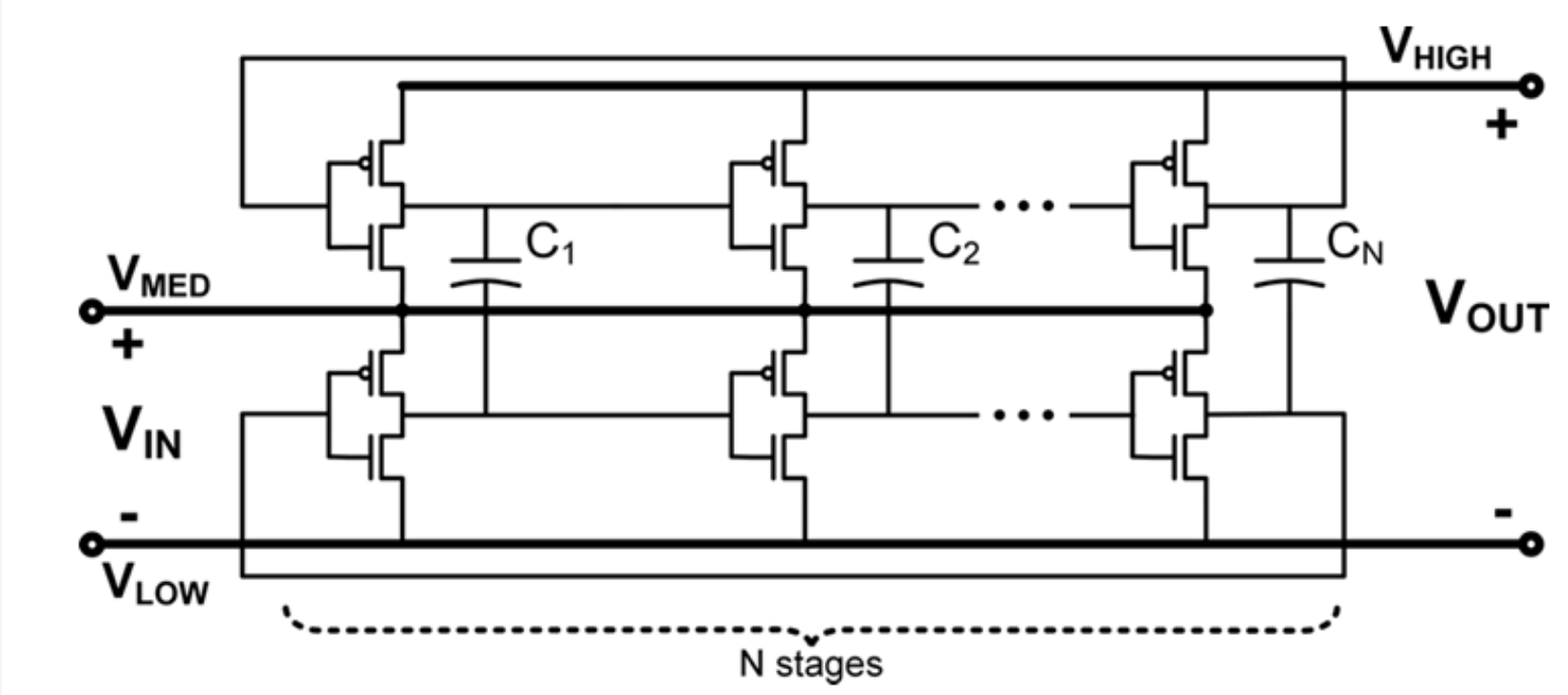
Core Design
Step II: Understanding Flying Capacitors

- Flying capacitors are capacitors that move charge from one part of the circuit to another.
- In this application, these flying capacitors are connected in between the cascading of inverters for each stage so that the logic high is stored in the capacitor and passed onto the next stage.
- To explain in a phased manner, in Phase 1, the capacitor gets charged from the input voltage whereas in Phase 2, it's reconnected and dumps its charge to the output or another stage.
- Also, these fly caps help to build charge pumps that boost voltage as well as allow the converter to work without inductors (which are bulky and hard to integrate on-chip).
- Overall in this selected research paper, the fly caps are part of the 5-stage switched-capacitor boosting network. Each stage uses these caps to pass energy to the next level and raise the voltage.

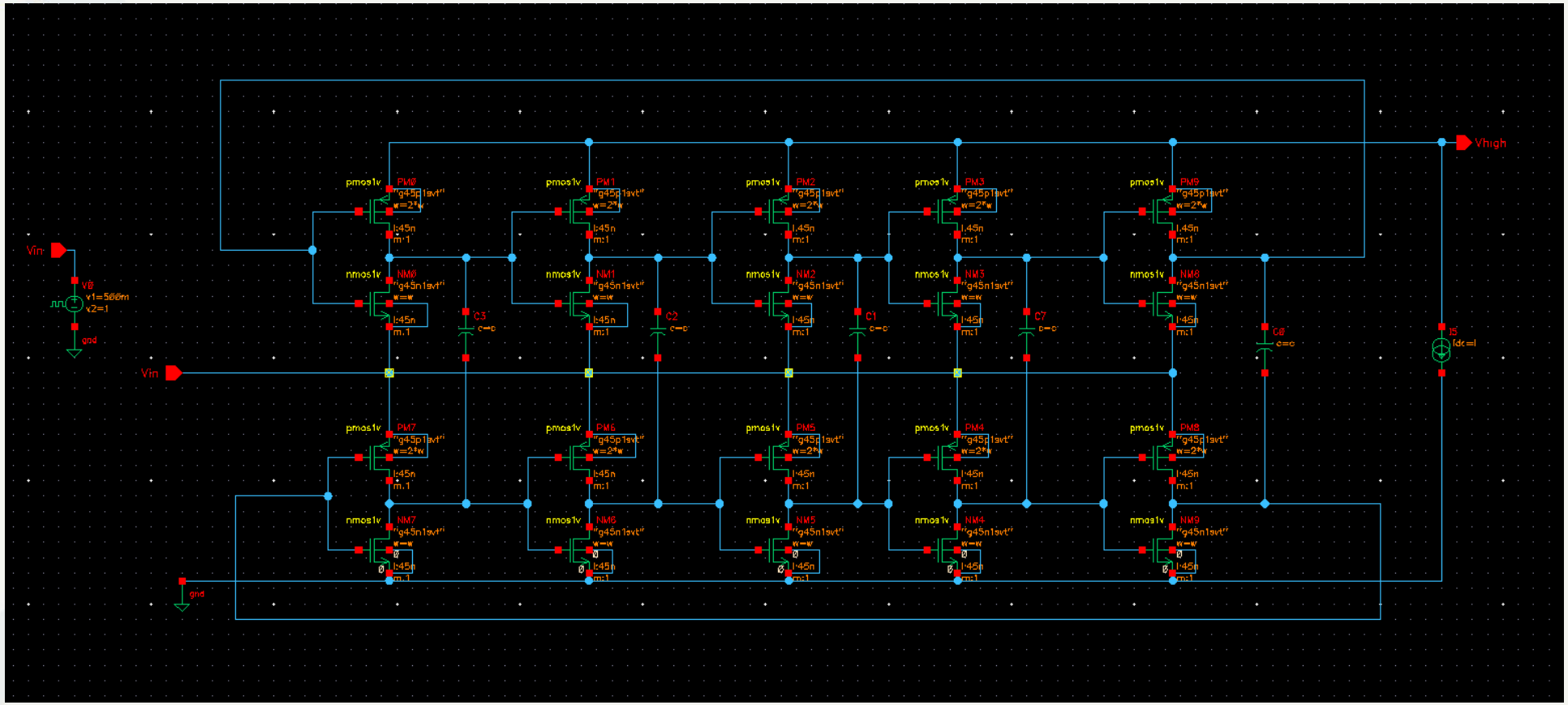
Core Design
Step III: Voltage Doubler – Circuit Diagram

- Number of Stages – 5
- Technology Node – 45nm
- Tool – Cadence Virtuoso
- Input Test Voltage – 1V

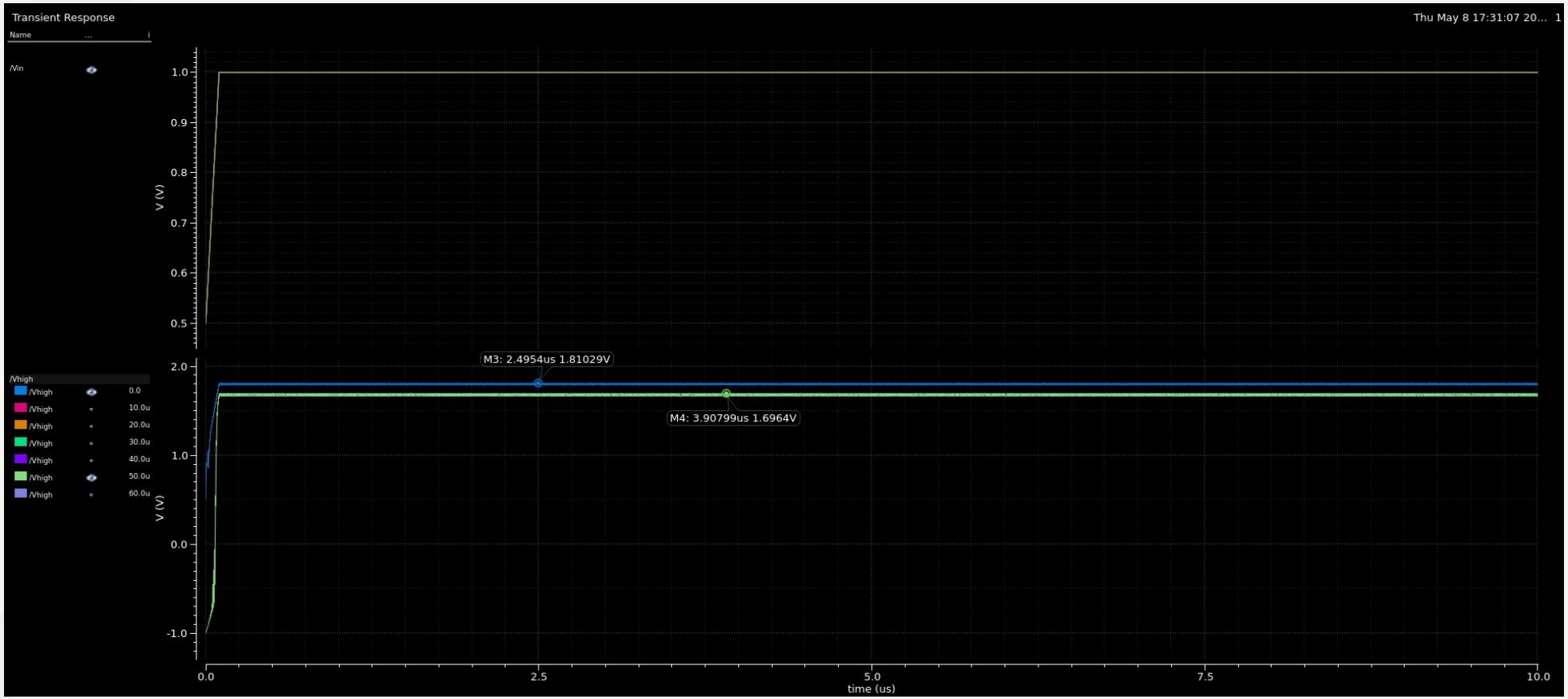
Note: For optimum width of NMOS and PMOS FETs and capacitance of fly caps we performed parametric analysis



Core Design
Step III: Voltage Doubler – Schematic



Core Design
Step III: Output Waveform – with I_{load} = 50 µA



C = 100fF and PMOS:NMOS = 2w:1w where w = 600nm

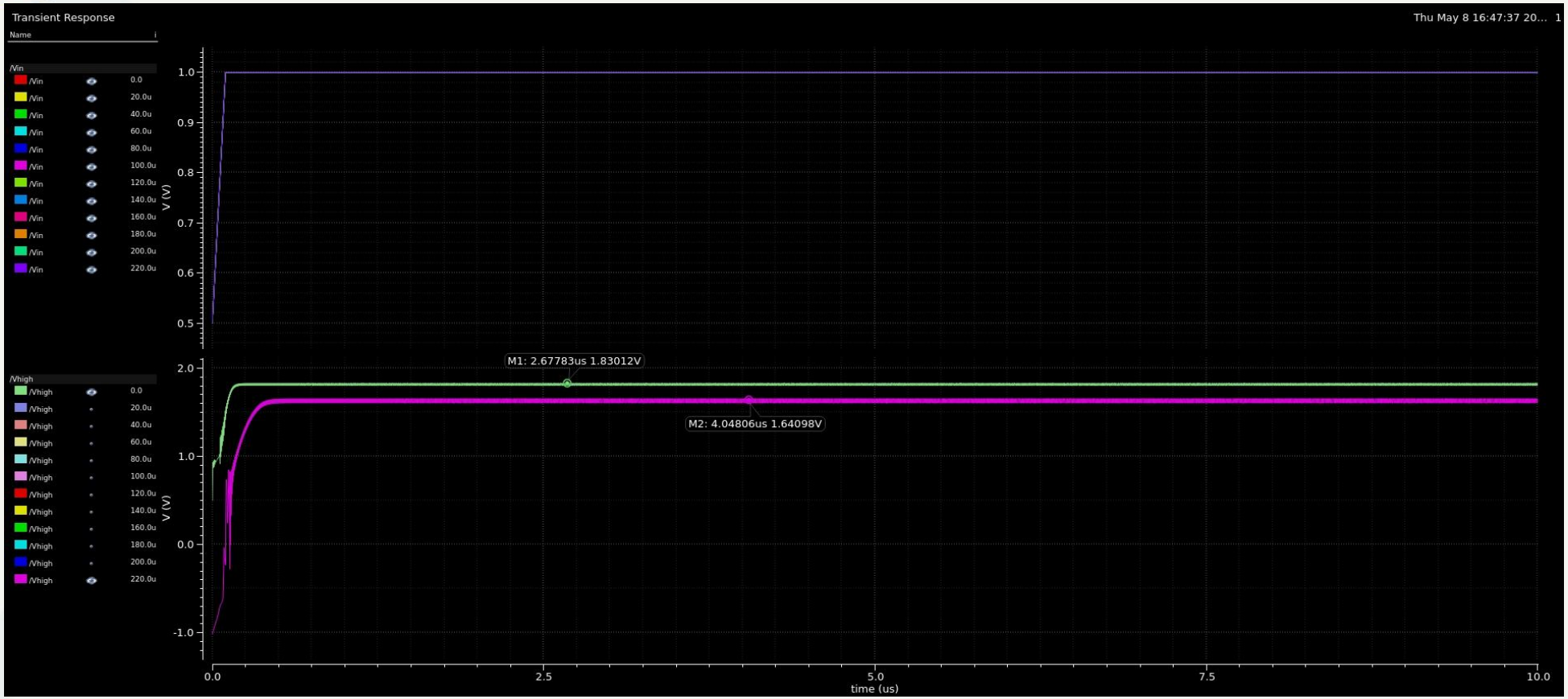
Core Design
Step III: Voltage Doubler – Analysis

Parameter	Without Load	With Load (50 µA)
Sizing PMOS:NMOS w = 600 nm	2w:1w	2w:1w
C_{fly}	100 fF	100 fF
V_{in}	1 V	1 V
V_{out}	1.81 V	1.69 V
Efficiency	81 %	69 %

To increase the efficiency of the proposed voltage doubler circuit for higher values of load current we have parameterized the width of transistor and capacitance of the fly cap.

The details of the same are in the next slide.

Core Design
Step IV: Output Waveform – with I_{load} = 0.22 mA



C = 10pF and PMOS:NMOS = 2w:1w where w = 2µm

Core Design
Step IV: Voltage Doubler – Analysis

Parameter	Without Load	With Load (0.22 mA)
Sizing PMOS:NMOS w = 2 µm	2w:1w	2w:1w
C_{fly}	10 pF	10 pF
V_{in}	1 V	1 V
V_{out}	1.83 V	1.64 V
Efficiency	83 %	64 %

Design Challenges and Trade-offs

Challenges:

- Initial challenge was to ensure the proper oscillation of the ring oscillator circuit.
- Also, to understand the working of the stacked ring oscillator and the effect of fly caps in order to obtain the expected voltage doubling.

Trade-offs:

- To achieve the optimized voltage doubling, the lower level of the input voltage signal should be above the threshold voltage of the transistors.
- In order to support for higher load currents of up to 0.22mA, the area has to be increased.
- The peak efficiency would be better in lower input voltages, as we keep on increasing the voltage level we saw slight decrease in the peak efficiency of the circuit.

Key Learnings: Intuition + Simulation

Intuition:

- Analysing the oscillatory behaviour of the ring oscillator and effect of number of stages
- The importance of using flying capacitors in the self oscillating voltage doubler circuit to move charge from one part of the circuit to another.

Simulation:

- Providing initial state to the output node in order to obtain and analyze transient simulation. After the simulation, we observed the expected oscillations for the ring oscillator at the output node.
- From the simulation, we learned that setting the lower level of the input pulse close to the transistor threshold voltage is crucial for achieving the expected oscillations and doubled output in ring oscillator circuits.

Performance Summary

Metric	Target	Achieved	Units
Output Voltage	2	1.83	V
Load Current	-	0.22	mA

Average Power delivered:
111.11µW (For maximum load = 50µA, Cfly = 100fF)
390.10µW (For maximum load = 0.22mA, Cfly = 10pF)

Next Steps

- The peak efficiency of the voltage doubler circuit can be improved.
- Newer technology node can result in better results for peak efficiency.
- Transistors of lower threshold voltage will help in better working of the circuit for lower input voltage levels.
- After achieving the desired efficiency of the voltage doubler, we can design the overall harvester and design the other components in a specific manner to achieve the power consumption in the order of nanowatts.

Conclusion: Designed self oscillating voltage doubler circuit with optimum sizing of transistors and capacitors through parametric analysis. Also, achieved the peak efficiency of around 70% with maximum load current of up to 0.22mA.

International Institute of Information Technology Bangalore

26/C, Electronics City, Hosur Road,

Bengaluru – 560 100, Karnataka, India

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