



Observations

1. Trend Consistency Across CPUs:

- Both graphs show a decreasing trend in miss rate as the cache size increases, which is expected. Larger caches can store more data, thus reducing the frequency of cache misses.

2. Miss Rate at Different Associativities:

- Associativity 2 (Solid Blue Line): Starts higher but shows significant reduction as cache size increases. This pattern is consistent in both CPUs.

- Associativity 4 (Dashed Orange Line): Generally starts with the highest miss rates at smaller cache sizes but rapidly converges with the other lines as cache size increases.

- Associativity 8 (Dotted Green Line): Generally shows the lowest miss rates across all cache sizes, emphasizing the efficiency of higher associativity in both CPU types.

3. Performance of Different CPUs:

- Both CPUs exhibit very similar patterns across different associativities, suggesting that the underlying architecture of the CPUs (at least in terms of cache performance) responds similarly to changes in cache size and associativity, with the O3 CPU being slightly better as compared to Simple CPU.

Graph Features

Both graphs depict:

- X-axis (Cache Size in kB): The cache sizes increase from left to right on the x-axis, ranging from a small value (possibly close to zero) to 1000 kB.

- Y-axis (Miss Rate): The miss rates are shown on the y-axis, starting from a high value near 0.9 down to lower values near 0.3 or less.

Graph Analysis

1. Trends:

- Both graphs show a decreasing trend in the miss rate as the cache size increases, which is expected as larger caches can hold more data and thereby reduce the number of cache misses.

- The graphs show that higher associativity generally results in a lower miss rate for any given cache size. This effect is due to the increased likelihood of finding data in the cache when there are more ways in a set-associative cache.

2. Comparative Analysis:

- Impact of CPU Model: The miss rate curves for the O3 CPU and the Simple CPU are similar, but the miss rates for the Simple CPU tend to be consistently lower across all associativities and cache sizes. However, when we increase the cache size significantly (say, to 1024 kB), the O3 CPU outperforms the Simple CPU. This suggests that the Simple CPU has a less complex access pattern and a more efficient baseline handling of cache accesses in this simulation setup, which is why it slightly outperforms O3 CPU for smaller cache sizes.

- Associativity Impact: For both CPU models, increasing the associativity from 2 to 8 tends to flatten the curve slightly, indicating diminishing returns on miss rate reduction as cache size increases. This effect is more pronounced in the O3 CPU graph, where the lines for different associativities are closer together, suggesting a more pronounced impact of associativity on miss rates in complex CPU models.

3. Interpretation and Implications:

- Cache Efficiency: Both CPUs show improved cache efficiency with larger cache sizes and higher associativities. However, the Simple CPU appears to extract more benefit from increasing cache size compared to the O3 CPU, up to a certain limit - due to its simple access pattern.

- Design Considerations: For scenarios where cache size and cost are constraints, these graphs suggest that increasing associativity might be a more cost-effective method of reducing miss rates than proportionally increasing cache size, especially for the O3 CPU.

- Optimization Strategies: The flatter curves at higher associativities indicate that after a certain point, further increases in cache size yield smaller improvements in miss rates. System designers might choose to optimize the cache configuration based on the specific needs and workload characteristics of the CPU type.

Conclusion

The graphs are a valuable tool for understanding how different cache configurations impact performance in various CPU architectures. They highlight how both cache size and associativity play crucial roles in optimizing cache performance, with distinct behaviors observed between simpler and more complex CPU models.

Observed Simulation Ticks:

simple cpu:

missrate = 0.763624, l2 cache = 64kb, assoc = 2, ticks = 60934126000
missrate = 0.885788, l2 cache = 32kb, assoc = 4, ticks = 61923108000
missrate = 0.764852, l2 cache = 64kb, assoc = 4, ticks = 60942022000
missrate = 0.768170, l2 cache = 64kb, assoc = 8, ticks = 60965467000
missrate = 0.521001, l2 cache = 256kb, assoc = 2, ticks = 58824192000
missrate = 0.523598, l2 cache = 256kb, assoc = 4, ticks = 58804134000
missrate = 0.251525, l2 cache = 1024kb, assoc = 2, ticks = 60996284000
missrate = 0.282557, l2 cache = 1024kb, assoc = 8, ticks = 56605603000

o3 cpu:

missrate = 0.766453, l2 cache = 64kb, assoc = 2, ticks = 13075161000
missrate = 0.887094, l2 cache = 32kb, assoc = 4, ticks = 13665636000
missrate = 0.767373, l2 cache = 64kb, assoc = 4, ticks = 13058308000
missrate = 0.770776, l2 cache = 64kb, assoc = 8, ticks = 13059688000
missrate = 0.523103, l2 cache = 256kb, assoc = 2, ticks = 12117522000
missrate = 0.525455, l2 cache = 256kb, assoc = 4, ticks = 12063130000
missrate = 0.251075, l2 cache = 1024kb, assoc = 2, ticks = 10785402000
missrate = 0.281598, l2 cache = 1024kb, assoc = 8, ticks = 10973545000

Simple CPU Data Table

L2 Cache Size	Associativity	Miss Rate	Ticks
64kB	2	0.763624	60,934,126,000
32kB	4	0.885788	61,923,108,000
64kB	4	0.764852	60,942,022,000
64kB	8	0.768170	60,965,467,000
256kB	2	0.521001	58,824,192,000
256kB	4	0.523598	58,804,134,000
1024kB	2	0.251525	60,996,284,000
1024kB	8	0.282557	56,605,603,000

O3 CPU Data Table

L2 Cache Size	Associativity	Miss Rate	Ticks
64kB	2	0.766453	13,075,161,000
32kB	4	0.887094	13,665,636,000
64kB	4	0.767373	13,058,308,000
64kB	8	0.770776	13,059,688,000
256kB	2	0.523103	12,117,522,000
256kB	4	0.525455	12,063,130,000
1024kB	2	0.251075	10,785,402,000
1024kB	8	0.281598	10,973,545,000