

## # Memory Hierarchy

- The memory unit is an essential component in any digital computer since it is needed for storing programs and data.
  - Not all the accumulated information is needed by the processor at the same time. Therefore, it is more economical to use low-cost storage devices to serve as backup for storing the information that is not currently used by the CPU.
  - The main memory unit the communicates directly with CPU is called main memory. Only programs and data currently needed by processor reside in main memory.
  - Devices that provide back up storage are called auxiliary storage memory.
- e.g Magnetic disk / hard disk (TB)  
 Magnetic Tape / Tape drives (PB/EB)
- AM are used for storing programs, large data files, and other back up information.

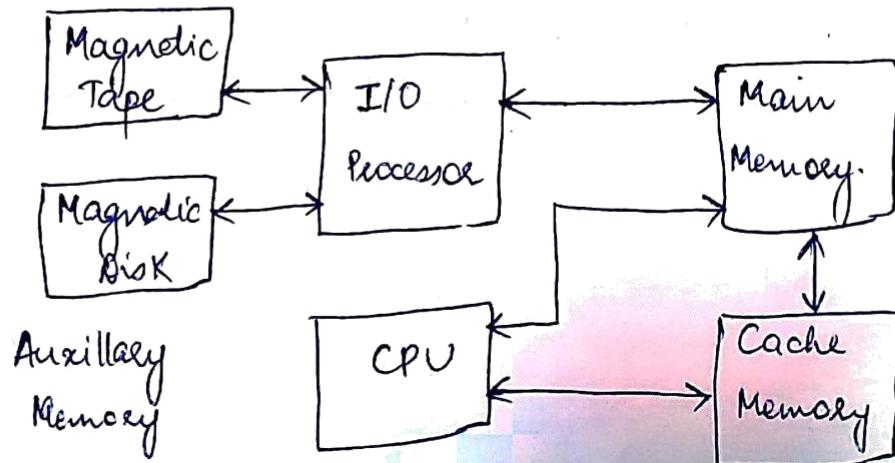


Fig:- Memory Hierarchy in computer

The total memory capacity of computer can be visualized as hierarchy of components

- Magnetic Tapes - used to store removable files.
- Magnetic Disk - used as backup storage.
- Main memory occupies a central position to communicate directly with CPU and auxiliary memory.

When programs in main memory are not needed by the CPU, they are transferred to auxiliary memory, to provide space for currently used program and data.

### Cache Memory-

A special very-high memory called a cache is used to increase the speed of processing by making current programs and data available at the CPU at a rapid rate.

The cache is used for storing segments of programs currently being executed in the CPU and temporary data frequently needed in the present calculations.

Note:- As the storage capacity of memory increases, the cost per bit for storing binary information decreases and the access time of the memory become longer. So the memory hierarchy is needed.

Auxillary Memory - large storage capacity, relatively inexpensive  
- low access speed compared to main memory

Cache Memory - small, relatively expensive.  
- very high access speed.

(24)  
(53)

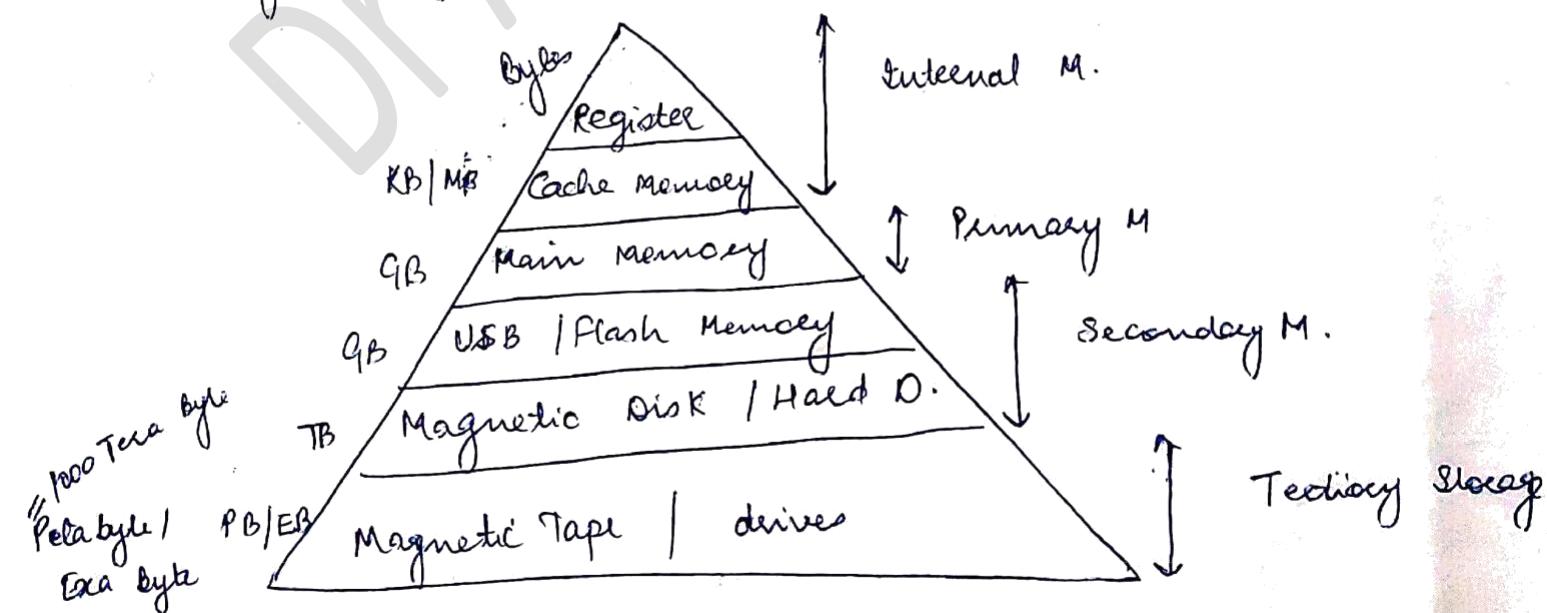
Therefore as the memory access speed increases, its cost increases.

## # Multiprogramming

Many operating system are designed to enable the CPU to process number of independent programs concurrently. This is known as multiprogramming.

## # Memory Management System

The part of computer system that supervise the flow of information b/w auxillary memory & main memory is known as memory management system.



$$1EB = 1000 \text{ PetaByte}$$

$$1PB = 1000 \text{ Tera Byte}$$

## # Main Memory (RAM)

- Central storage in computer system.
- Relatively large and fast memory.
- Used to store programs and data during computer operation.
- Integrated circuit RAM chips are available in two possible operating modes, static and dynamic.

→ Static RAM -

- \* Consist of internal flip-flop that store the binary information.
- \* Stored information remain valid as long as power is applied to the unit.

→ Dynamic RAM -

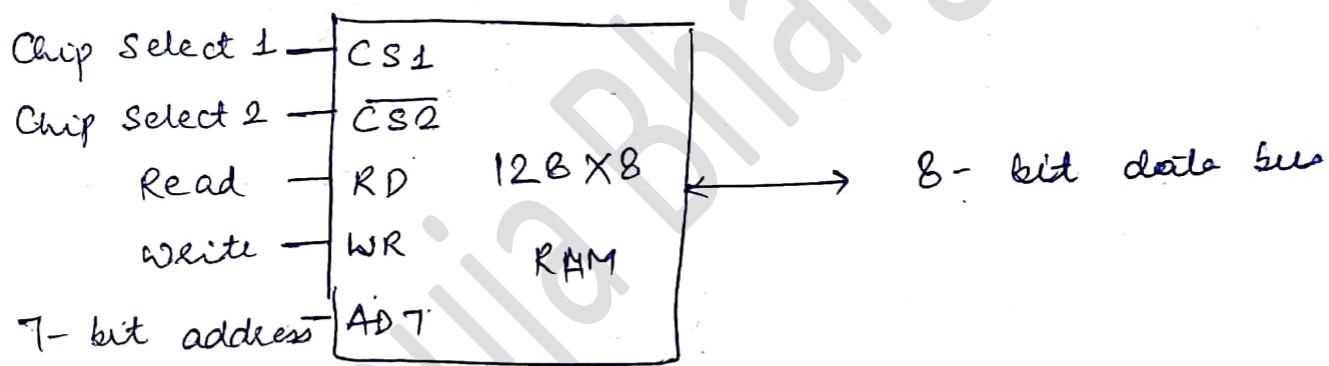
- \* Stores the binary information in the form of electric charges that are applied to capacitors.
- \* Offers reduced power consumption and larger storage capacity.
- \* Used in main memory.

## RAM & ROM Chips.

\* Read - data transfer b/w main memory & CPU.

\* Write - data transfer b/w CPU & main memory.

- RAM chip is better suited for communication with the CPU if it has one or more inputs that select the chip only when needed.
- RAM has bidirectional data bus that allows the data transfer either from memory to CPU i.e. read operation or CPU to memory i.e. write operation.
- Block diagram of RAM chip



- The capacity of the memory is 128 words of eight bits (one byte) per word.
- This requires 7-bit address and 8-bit bidirectional data bus.
- The read and write input specify the memory operation and the two chip select (CS) control input are used for enabling the chip only when selected by processor.

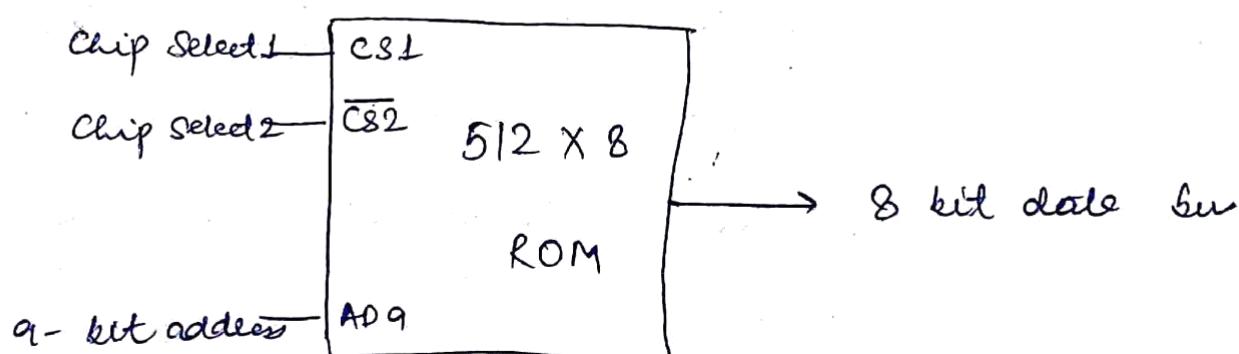
\* 2 Chip Select  $\rightarrow 2^2 = 4$  RAM can be selected

## • Functional Table of RAM

CS1	$\overline{CS2}$	RD	WR	function	State of Bus
0	0	x	x	Inhibit	High Impedance
0	1	x	x	Inhibit	"
1	0	0	0	Inhibit	"
1	0	0	1	Write	Input data to RAM
1	0	1	0	Read	Output data from RAM
1	1	x	x	Inhibit	High Impedance

\* Inhibit - Not performing any operation      \* High Impedance - Open Circuit  
 → When CS1 = 1,  $\overline{CS2} = 0$ ,  
 Memory can be placed in write or read mode.

- When WR is enabled, the memory stores a byte from data into location
- When RD is enabled, the content of selected bus is placed into the data bus.
- Block Diagram of ROM



→ Since ROM can only read, data bus can only be in output mode.

Note:- For the same-size chip, it is possible to have more bits of ROM than of RAM, because the internal binary cells of ROM occupy less space than RAM. For this reason, ROM specifies 512 bytes, while RAM has only 128 bytes.

→ 9 address lines specifies 512 bytes.

→  $\overline{CS1} = 1$  and  $\overline{CS2} = 0$  for operation

Otherwise data bus is in high impedance state.

### Memory Address Map.

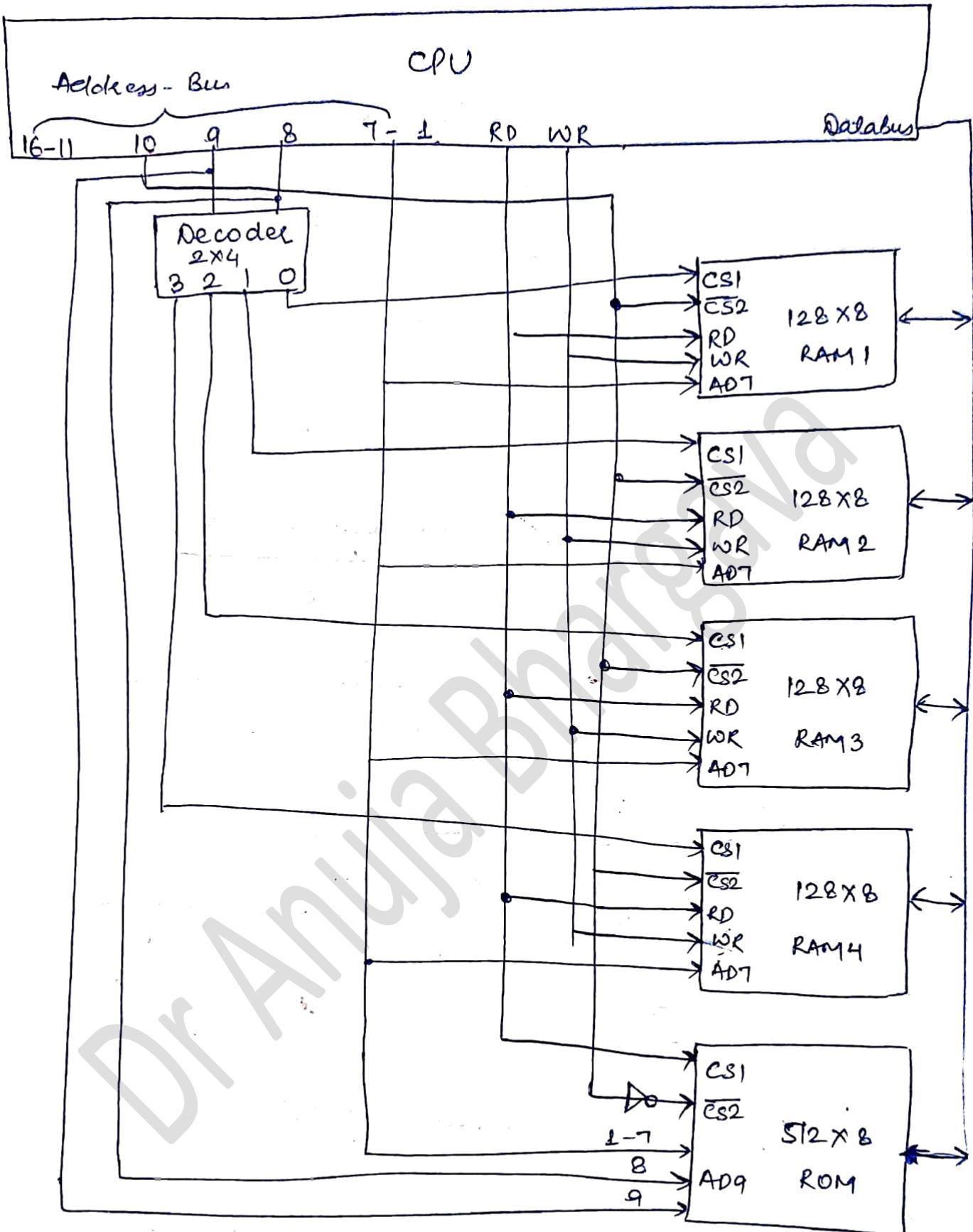
- The designer of the computer system must calculate the amount of memory required for particular application and assign it to either RAM or ROM.
- The Memory address map is a pictorial representation of assigned address space for each chip in the system.
- eg. 512 bytes RAM & 512 bytes ROM.

Component	Hexadecimal Address	Address Bus									
		10	9	8	7	6	5	4	3	2	1
RAM 1	0000-007F	0	0	0	x	x	x	x	x	x	x
RAM 2	0080-00FF	0	0	1	x	x	x	x	x	x	x
RAM 3	0100-017F	0	1	0	x	x	x	x	x	x	x
RAM 4	0180-01FF	0	1	1	x	x	x	x	x	x	x
ROM	0200 - 03FF	1	x	x	x	x	x	x	x	x	x

- The x's are assigned to low-order bus lines.
- When line 10 is 0, CPU selects RAM  
When line 10 is 1, it selects ROM.
- There are 16 lines in address bus, the table shows only 10 because in this example other 6 are not used.

### Memory Connection to CPU

Note:- The example shows gives an indication of interconnection complexity that can exist between Memory chips and CPU.



• 2x4 Decoder

Input		Output
0	0	RAM 1
0	1	RAM 2
0	0	RAM 3
1	1	RAM 4

- Q) a) How many  $128 \times 8$  RAM chips are needed to provide a memory capacity of  $2048$  bytes.
- b) How many lines of the address bus must be used to access  $2048$  bytes of memory. How many of the lines will be common to all chips.
- c) How many lines must be decoded for chip select? Specify size of decoders.

Soln:-

a) Number of chips =  $\frac{\text{Memory Capacity}}{\text{Size}}$

$$= \frac{2048}{128} = 16 \text{ chips}$$

b)  $2^x = 2048$

$\therefore 11$  lines needed to address  $2048$  bytes.

(AD1-AD7 + Decoder lines)

$$128 = 2^7$$

$\therefore 7$  lines are common to all chip.

c) for selecting 16 chips, decoder required is  
 $4 \times 16$  decoder

Q for 4096 bytes of RAM and 4096 bytes of ROM.<sup>41</sup>  
 List the memory address map and indicate decoder size.

Soln:-

$$\text{Number of chips} = \frac{4096}{128}$$

$$= 32 \text{ RAM chips}$$

$$= \frac{4096}{512}$$

$$= 8 \cdot \text{ROM chips.}$$

$$\text{Also, } 4096 = 2^{12}$$

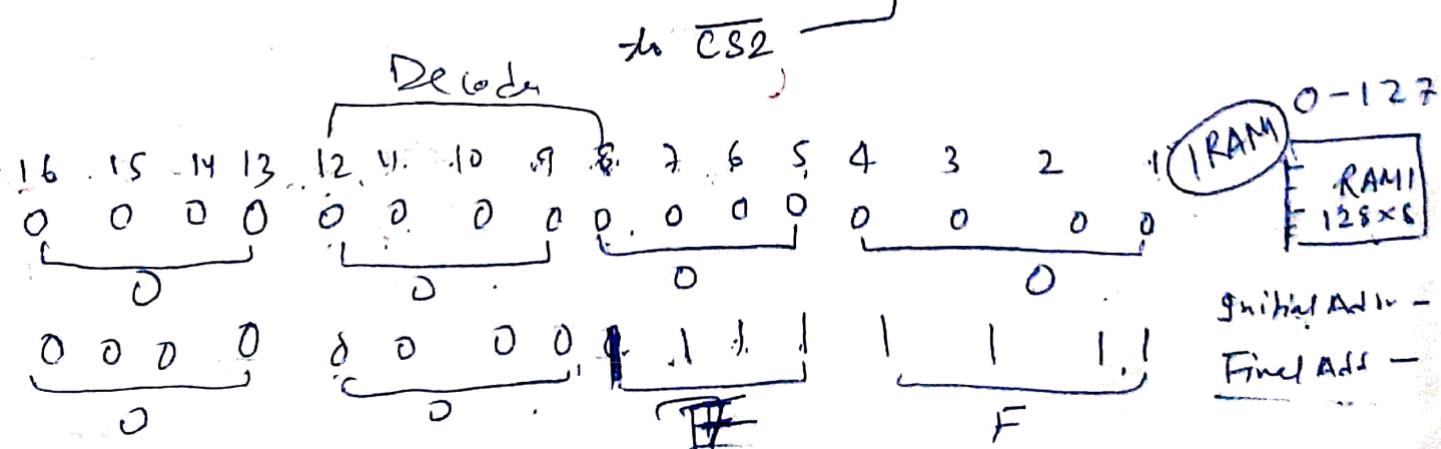
12 common address lines & 1 to select between RAM & ROM.

Component Address 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

RAM 0000-0FFF 0 0 0 0 ←  $\frac{8 \times 32}{\text{decoder}}$  → x x x x x x x

ROM 1000-1FFF 0 0 0 1 ←  $\frac{3 \times 8}{\text{decoder}}$  → x x x x x x x x

Decoder to CS2



Initial Addr -  
Final Addr -

0-127  
RAM  
RAM1  
128x8

A computer employs RAM chips of  $256 \times 8$  and ROM chips of  $1024 \times 8$ . The system needs 2K bytes of RAM, 4K bytes of ROM and four interface units each with four registers. A memory mapped I/O configuration used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for Interface registers.

- How many RAM & ROM chips are needed.
- Draw a memory address map for the system.
- Give the address range in hexadecimal for RAM, ROM & Interface.

Soln:- a) RAM chips =  $\frac{2048}{256} = 8$  chips

ROM chips =  $\frac{4096}{1024} = 4$  chips

b)  $2048 = 2^{11}$ ,  $256 = 2^8$

$4096 = 2^{12}$ ,  $1024 = 2^{10}$

Interface  $4 \times 4 = 16$  Registers =  $2^4$

c) Component Address 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

RAM 0000-0FFF 0 0 0 0 0 /  $\xrightarrow{\text{3x8}} \text{decoder}$  x x x x x x x x

ROM 4000-4FFF 0 1 0 0 /  $\xrightarrow{\text{2x4}} \text{decoder}$  x x x x x x x x

Interface 8000-800F 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 x x x x