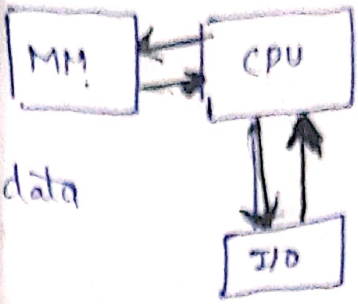
Mode of data transfer.

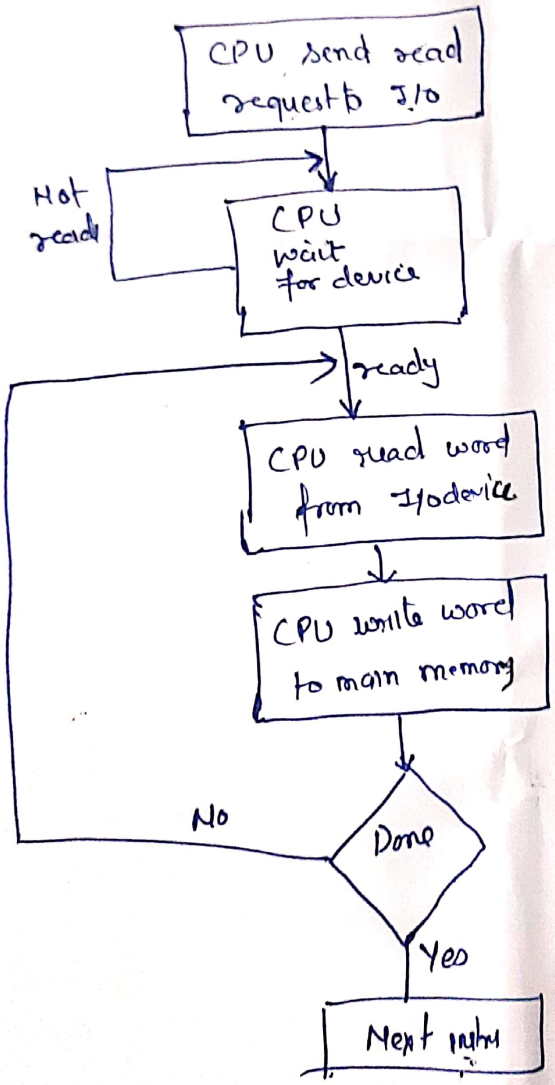
Data transfer between the Central Computer and I/O devices may be handeld in Vanity of modes.



There are three types of mode of data transfer.

1. Programmed I/O
2. Interrupt Initiated I/O
3. Direct memory Access.

1. Programmed I/O



Programmed I/O operation are result of I/O instruction written in computer program.

→ Each data transfer is initiated by an I/O instruction in the Program

→ Transferring data under program control requires constant monitoring of the I/O devices by the CPU.

→ In programmed I/O, CPU makes a request and then CPU stays in program loop (polling) until the I/O device indicates that it is ready for data transfer.

② Interrupt Initiated I/O

→ In II I/O instead of continous monitoring of CPU, interface will be informed to issue an Interrupt request signal when data are available from the device

→ meanwhile, CPU, proceeds to execute another program and interface keep monitoring the device

→ when device is ready for data transfer. it generate the Interrupt ~~signal~~ request

→ once Interrupt signal detected, the CPU stop ~~the~~ ~~for~~ its current task and process the I/O data transfer and the resume back to its orignal task it was performing.

Direct memory Access:-

To transfer larger block of data at high speed between external devices and main memory DMA approach is used efficiently.

→ DMA allows data transfer directly b/w I/O and main memory, with minimal intervention of CPU.

→ DMA grant ~~CPU~~ I/O interface authority to read/write to memory without CPU involvement.

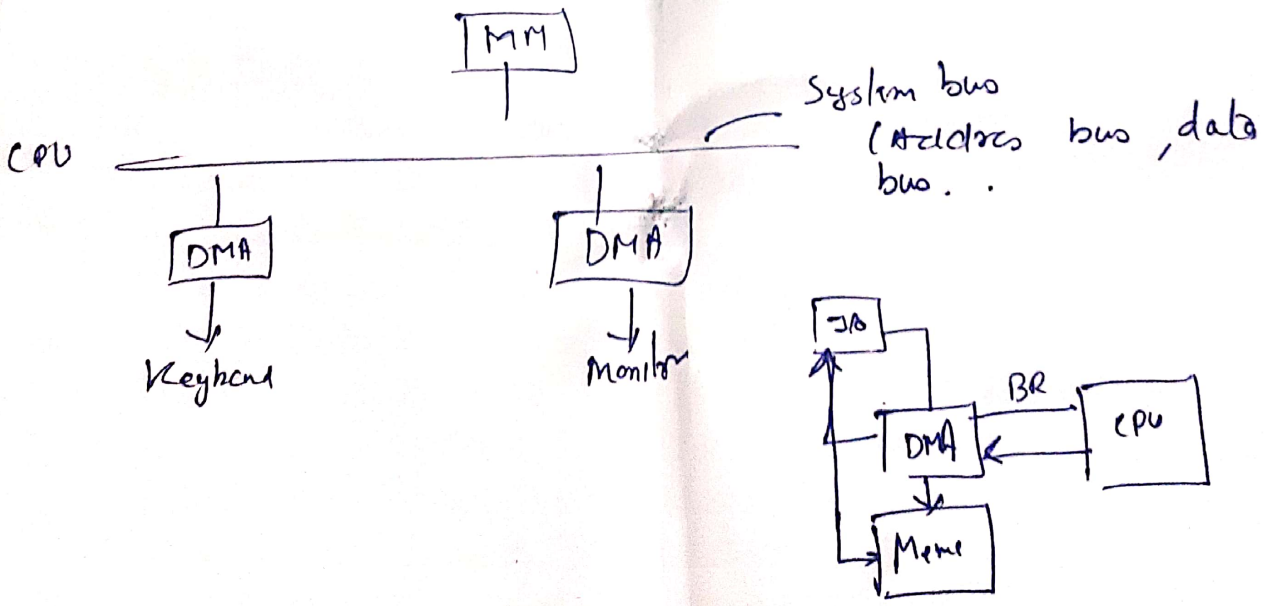
→ . DMA itself control data transfer b/w MM to I/O devices

→ . CPU only involved in begning and end of the data transfer. and interrupt only after entire block has been transferred.

→ CPU ask the DMA Controller to transfer data b/w a device and main memory and then CPU proceed to do other task.

→ DMA Controller issues a request to the right I/O device and manage data transfer b/w MM and device

→ when data transfer finishes DMA Controller interrupt the CPU



DMA ~~Control~~ working

1. I/O want to transfer data with MM
2. IO/Send DMA request to DMA Controller
3. DMAC sends BR (Bus req) to CPU for the bus
4. DMAC wait until CPU send BG signal to DMA
5. CPU provid the control of system Bus to DMAC, and place all of its data bus RD WR and AB in high impedance
6. CPU achn the BG signal and becom idel
7. DMAC take Controll of the buses to Conduct direct data transfer b/w MM & I/O devices.
8. After data transfer DMAC disable. BR and CPU disable BG; take Control of the buse and return the CPU normal function