

Input Output Interface

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- The purpose of interfacing are as follows -
 - (i) Peripherals are electromechanical and electromagnetic devices and are interacting with electronic devices (CPU).
 - (ii) Data transfer rate of ~~any~~ peripherals is usually slower than transfer rate of CPU.
 - (iii) Data codes and formats in peripherals differ from word format in CPU.
 - (iv) Operating modes of peripherals all differ from each other and each one must be controlled without disturbing other.
- To resolve these differences computer system includes interface unit between CPU and peripherals to supervise and synchronize all input and output transfers.
- Each peripheral has its own controller that operates a particular electromechanical device.
- To communicate with a particular device, the processor places a device address on the address lines.

- When the interface detects its own address, it activates path between bus lines and the device.
- At the -line address is made available in address lines, the processor provides function code (I/O command) in the control lines.

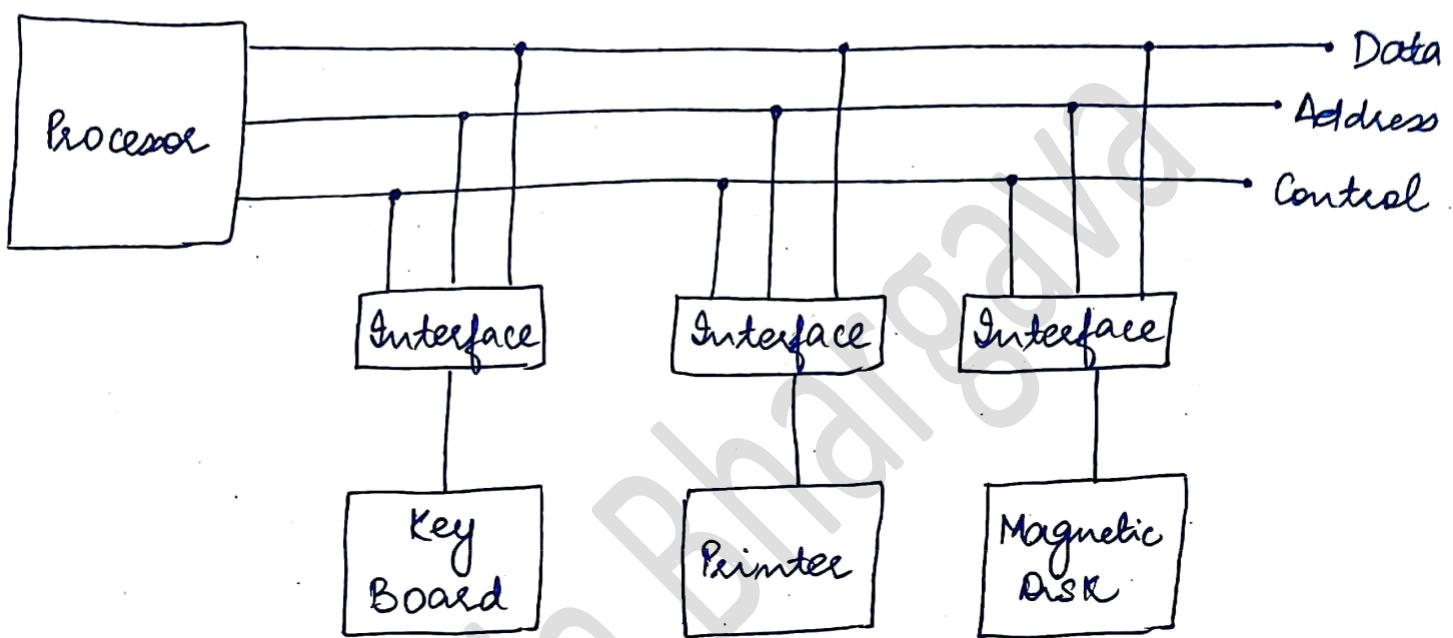


Fig :- Connection of I/O Bus to I/O devices.

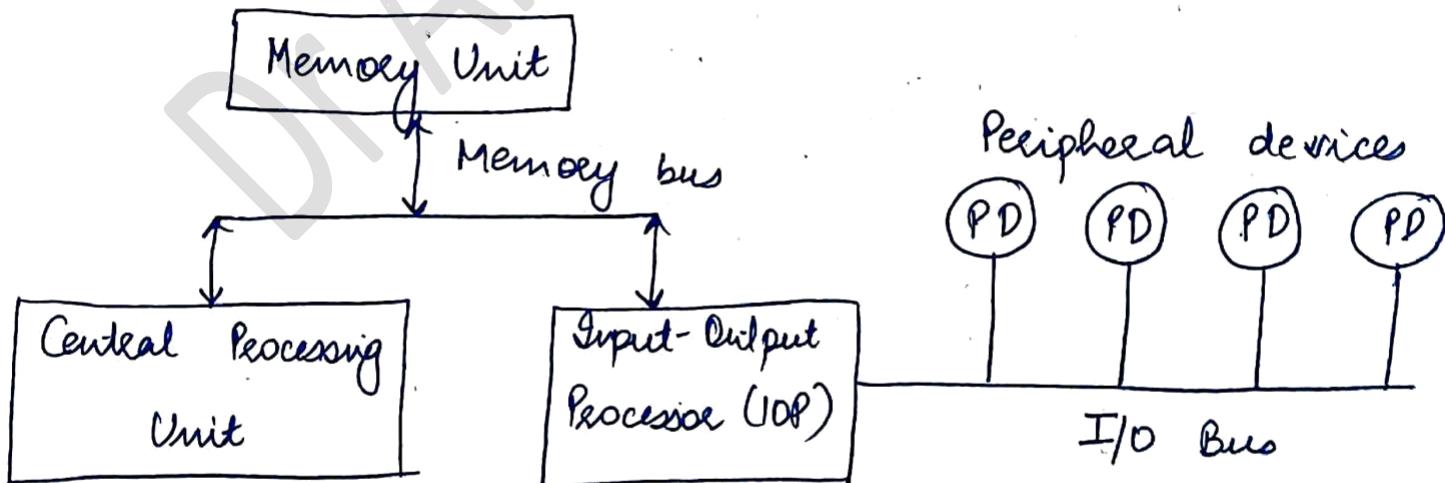
I/O versus Memory Bus

- In addition to communicating to I/O, processor must also communicate with memory unit.
- There are three ways that computer buses can be used to communicate with memory and I/O.
 - Use two separate bus, one for memory and one for I/O.

- Use one common bus for both memory and I/O but have separate control lines k/a Isolated I/O.
- Use one common bus for memory and I/O, with common control lines known as Memory Mapped I/O.

Input-Output Transfer (IOP)

- An IOP take care of input and output task.
- The CPU is assigned the task of initiating all operations, but I/O instructions are executed in IOP.
- When an I/O operation is required, the CPU informs the IOP where to find I/O program and then leaves the transfer details to the IOP.



Mode of Transfer

- Data transfer between the CPU and the I/O devices may be handled in variety of modes.
- Some modes use the CPU as an intermediate path and other transfer the data directly to and from the memory unit.
- Data transfer to and from peripherals be handled in three ways
 1. Programmed I/O
 2. Interrupt Initiated I/O
 3. Direct Memory Access (DMA)

1) Programmed I/O

- Programmed I/O operations are the result of I/O instructions. Each data item transfer is initiate by an instruction in the program.
- Usually the transfer is to and from a CPU register and peripheral. Other instructions are needed to transfer data between memory and CPU.
- Once a data transfer is initiated, the CPU is required to monitor the interface to see when a transfer can again be made.

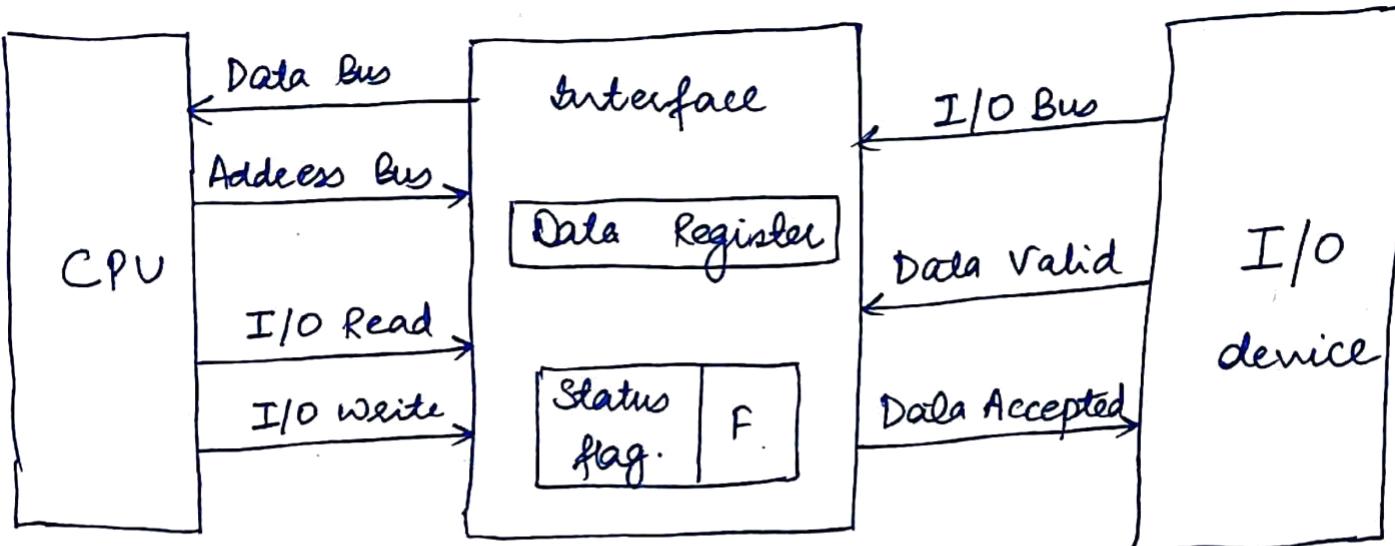


Fig: Data transfer from I/O device to CPU

2) Interrupt Initiated I/O

- In the programmed I/O CPU stays in program loop until the I/O indicates that it is ready for data transfer.
- This is time consuming process since it makes CPU busy needlessly.
- This can be avoided by using an interrupt facility.
- Major type of interrupt

1) External I- It comes from I/O devices or external source.

2) Internal I- It includes register overflow, stack overflow.

3) Software or Hardware I- External or Internal I. are hardware I. Software I. is initiated by executing a instruction

4) Priority I- If several devices request simultaneously, in this case system decide which device to service first.

Direct Memory Access (DMA)

- The transfer of data between a fast storage device such as magnetic disk and memory often limited to the speed of CPU.
- Removing the CPU and letting the peripheral device manage the memory bus directly improve speed of transfer
- Such transfer technique is called Direct Memory Access (DMA).

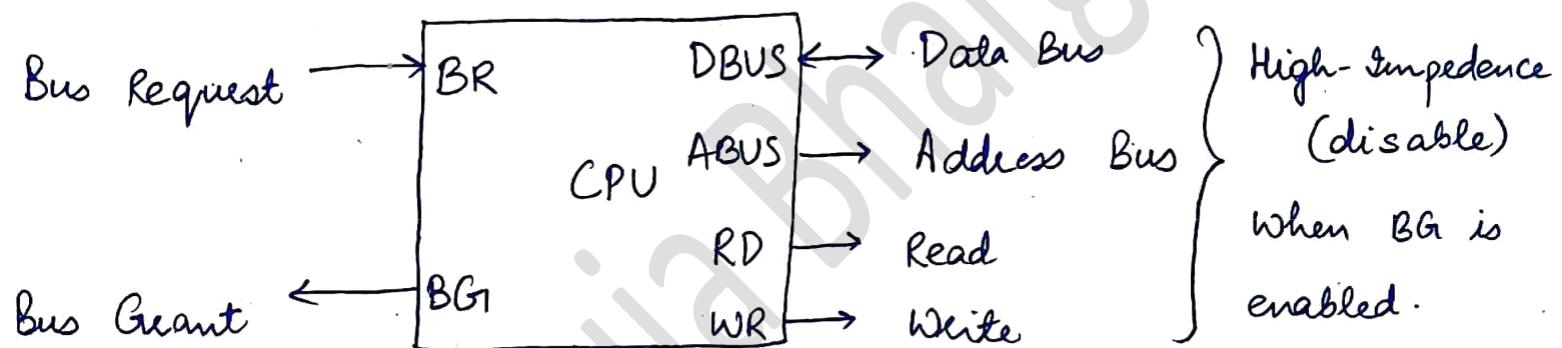


Fig : CPU bus signals for DMA transfer

- Data transfer ways :
 - Burst Transfer - Here, number of words are transferred in a block. Example: Magnetic Disk
 - Cycle Stealing : - Allow the DMA controller to transfer one data word at a time after it must return the control of buses to CPU.

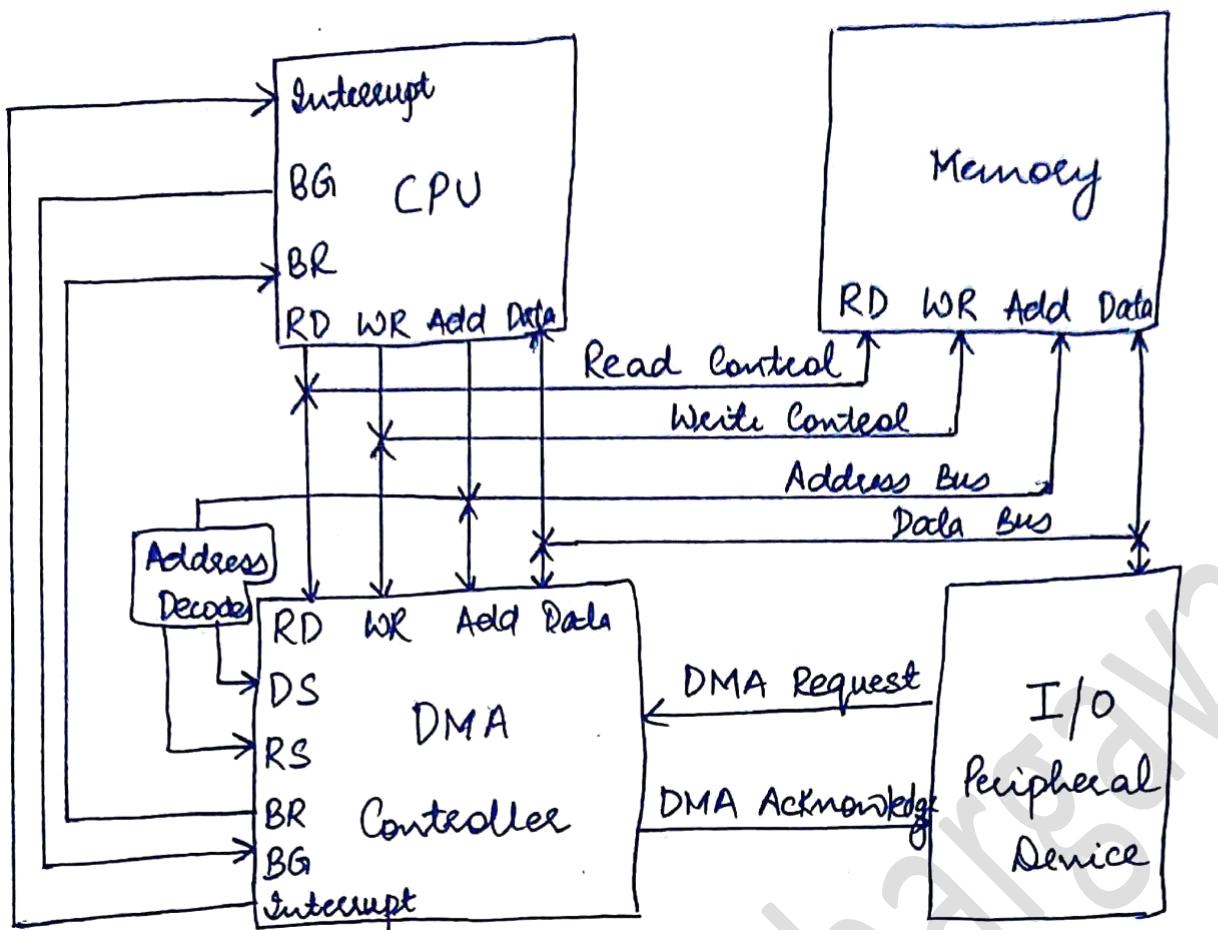


Fig: DMA transfer in computer

- DMA transfers the data between I/O to memory without using CPU.
- When I/O device is ready to send data, it sends DMA request. (i.e. ready to transfer the data) Then DMA controller sends BR (Bus request to CPU). CPU stands RD, WR, Address and Data in high impedance state i.e. open circuit. Now, CPU sends BG (Bus Grant) to DMA controller. Now, bus is hand over to the DMA controller. Now, it is the responsibility of DMA controller to transfer the data between I/O & memory.

then DMA send acknowledgement to the I/O device.

i.e $BG_1 = 1$, Buses with DMA

$BG_1 = 0$, Buses with CPU

Bus Arbitration

- The device that is allowed to initiate data transfer on the bus at any given time is called bus ~~master~~ ^{Master}.
- Bus arbitration is the process by which the next device becomes bus master and will do the data transfer.

Bus

1. Data bus - Bidirectional bus and transfers data.
2. Address bus - Unidirectional bus and sends the address.
3. Control bus - R/W, BR, BG etc.

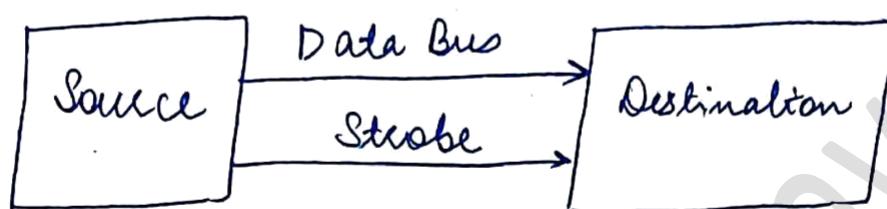
Synchronous or Asynchronous Data Transfer

- If the registers in the interface share a common block with the CPU registers, the transfer is synchronous.
- Asynchronous data transfer can be accomplished by strobe & handshaking.

Strobe Control

- It employs single control line.
- It can be activated either by source or destination unit.

(i) Source Initiated Data Transfer



If strobe is activated, data bus has valid signal.

(ii) Destination Initiated data transfer

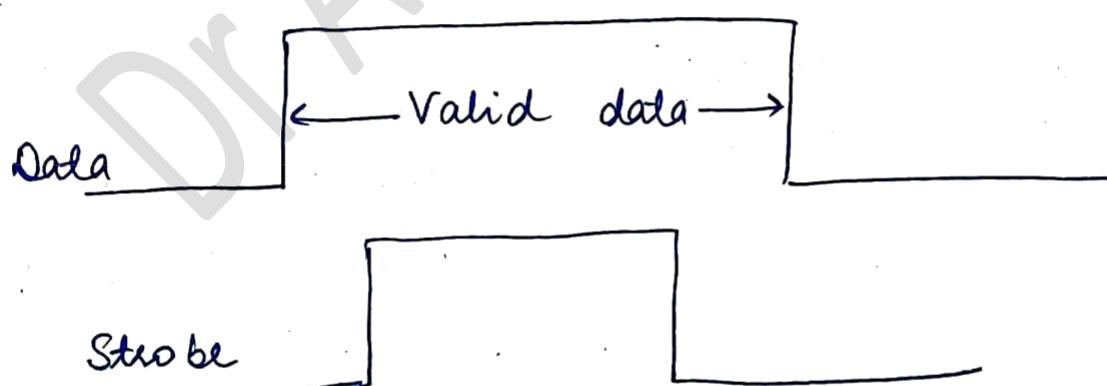
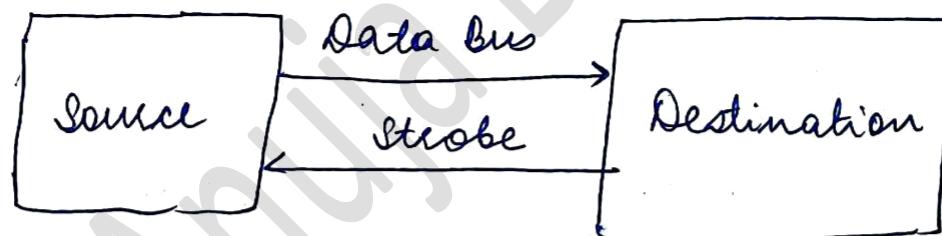
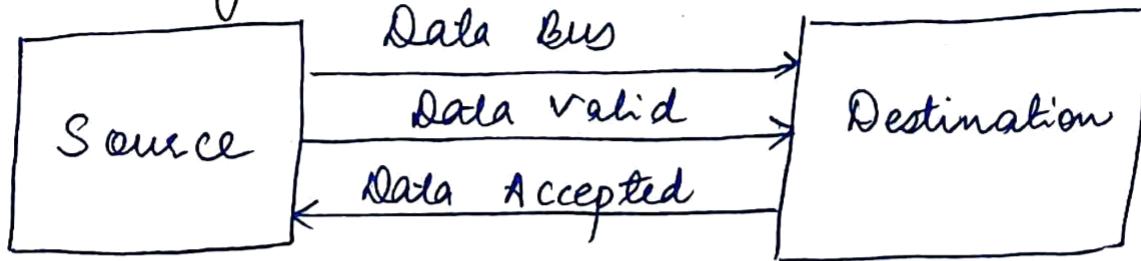
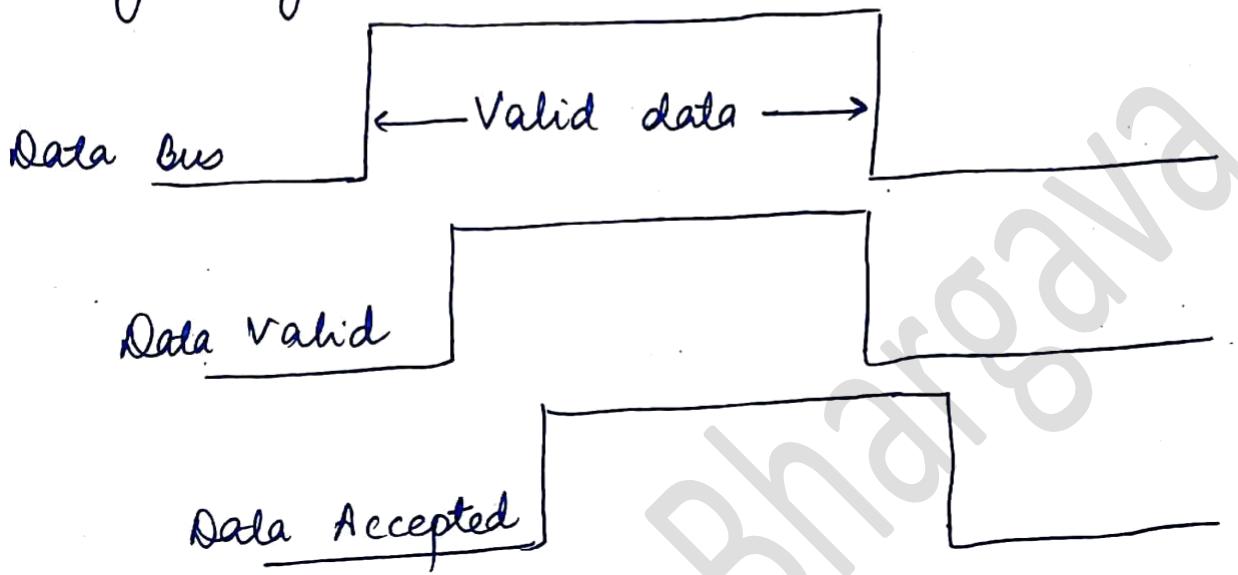


Fig: Timing diagram

Hand shaking



Timing Diagram



Sequence of Events

