CS

University Roll No.....

End Term Examination, Odd Semester, 2018-19

B.Tech, CS/CCV/DA, II[nd] Year, III Semester

Subject Code: BCSC 0005 **Subject Name: Computer Organization**

Max Marks: 50 **Duration: 3 hours**

Section-A **(7 X 5 = 35 marks)**

Note: Attempt ALL questions

I. Consider a register A holding 8-bit binary 10101101. Determine the value of B operand and logic/shift microoperation to be performed in order to change the value in A to:

a. 11101111 b. 01100110 c. 00001001 d. 10000001
e. 01011011

II. Draw the block diagram of 64-word stack and explain how push and pop operations are implemented in it using various micro operations.
The content of the top of a memory stack is 1120. The content of the stack pointer SP is 5040. A two-word call subroutine instruction is located in memory at address 2441 followed by address field of 6720 at location 2442. What are the content of PC, SP and top of stack:
a. Before the call instruction is fetched from the memory.
b. After the call instruction is executed.

III. What is the purpose of control memory? Draw the block diagram of micro-program sequencer for a control memory and also explain it.

IV. Define the following:

a. Micro-operation b. Micro-instruction c. Micro-routine
d. Control word e. Micro program counter

V. What is bus arbitration? Explain various mechanisms for bus arbitration in detail. Also specify advantage and disadvantage of each of them.

VI. Explain various cache mapping techniques. A computer system has a 4K word cache organized in block associative manner with 4 blocks per set, 64 words per block. The main memory contains 65536 blocks. How many bits are there in each of the TAG, SET and WORD fields?

VII. Differentiate between:

a. DMA and Input/Output processor

b. Isolated input/output and Memory mapped input/output

Section- B

Note: Attempt ALL questions **(3 X 2= 6 marks)**

(I)A. Why are the read and write control lines in a DMA controller bidirectional? Under what conditions they are used as inputs and under what conditions they are used as output?

B. What are the various write policies used to write data in cache? Explain them with advantage and disadvantage of each.

C. Consider a digital computer has a memory unit of 64K X 16 and cache memory of 1K word. The cache uses direct mapping with 4 block size of four words.

a. How many bits are there in the TAG, BLOCK and WORD fields?

b. How many blocks can cache accommodate.

Note: Attempt ALL questions **(3 X 3= 9 marks)**

(II) A. Consider a 32- bit microprocessor that has an on-chip 16 KB four way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped?

B. a. How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

c. How many lines must be decoded for chip select? Specify the size of decoder.

C. Consider the following page address trace generated by a two-level memory scheme using page system. The memory has capacity of four pages:

6 4 5 1 4 3 2 1 2 1 4 6 7 4

Assuming the memory has pages 1, 2, 3 and 4 initially. Show the number of page faults using following replacement policies:

a. FIFO b. LRU