\* Write Back and Write through Write Back write through 1. Date is updated only in cm 1. Data is updated both in cM and MA 2. Simple method to implement 2. Complex method to implement 3. When a cache block is not required then selected ache block is written back to 3. When Cache block is not required, there is no need to written back to main memory MM to UPDATE the main miney. 4. commonly used method 4. unpopular method i. Unreliable Method 5. Reliable Method No Date Redundancy 6. Data Redundancy No wastage of time as data updates occurs only in cm 7. Wastage of time as each data updates both in cache and main memory - Cache Performance: (h) Hit + Miss = Total No. of CRU Reference Miss Ratio = No. of Miss = Total No. of Miss

(1-h) Hit+Miss Total No. of (A) Reference Cache Access Time - Time required to access word from

(Cache Hit Time) Miss Penalty (Cashe Misstane Penalty) - The time required to feth the required block from MM. Aug. Access Time of CPU = Hit Ratio x Cache Access Time + (1-Hit Ratio) x Miss Had X Miss Amal = hx T, + (1-h) 7m

The access time of a cache memory is looms and that of MM looms. It is estimated that 80% of the memory requests are fer read and the remaining 20% for write. The hit ratio for read accesses only is 0.9. A write through procedure is used

a what is the average acess time of the system considering only memory read cycle.

b) what is the average access time of the cyslen for both read and write cycle-

c) what is the hit ratio taking into consideration the writy cycles

501": Aug Access hime of Gyskm ((Au) = Hit Rahio x Cache Access hime + (1-Hit rahio) x Miss Penalty

= hx Tc + (1-h) x Th

a) Total read access him = 0.9×100 + (1-0.9) × (100+1000)
= 90+0.1×1100 = 90+110=200 ms

Total write access hime = 1 x max (100, 1000)
= 1000 hs lm mm

b) Avg. access time for both read & write
= 80% are Read request + 20% are write
= 0.8 x 200 + 0.2 x 1000
= 3160 + 200 = 3600015

c) Hit Ratio = 0.8x 0.9 + 0.2x 0 = 0.72