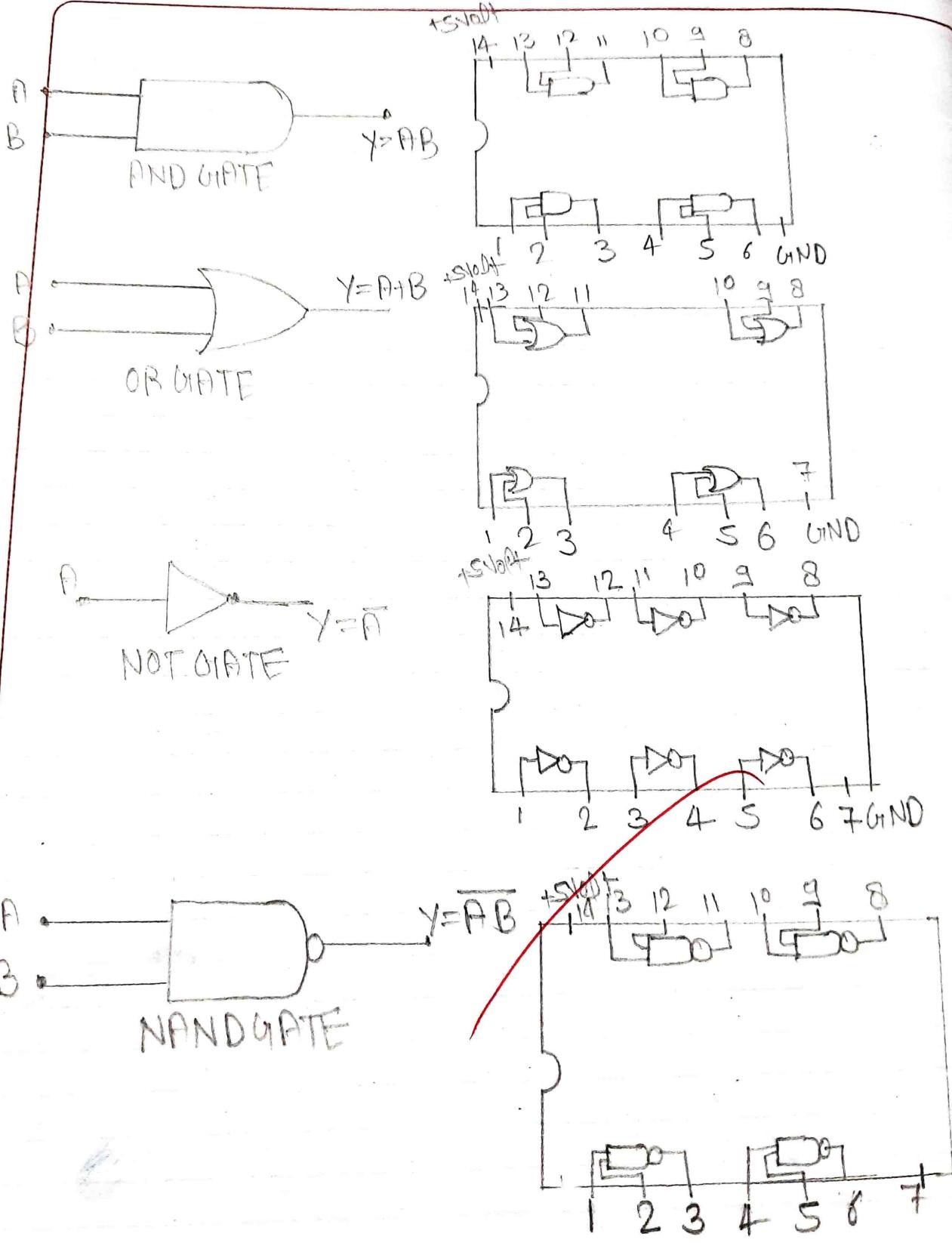


I N D E X

Name : Kanishk Patel Class & Section : BTech (SE) (D2)
 Subject : Computer Organization LAB Roll No. 26

S.No.	Name of the Experiment	Page No.	Date of Experiment	Date of Submission	Teacher's Sign/Remarks
1	Bread board implementation of different AND OR NAND NOT NOR and XOR	1-4	01-9-22	Rn 8-9-22	
2	To realize all logic gates using NAND and NOR	5-7	8-9-22	fir 15-9-22	
3	Implementation of Half adder and full adder using logic gates	8-11	15-9-22	fir 22-9-22	
4	To implement half subtractor and full subtractor	12-14	22-9-22	Rn 29-9-22	
5	Bread board implementation of flip flop (SR, JK, DT)	15-17	29-9-22	Rn 3-10-22	
6	Design 2x1 and 4x1 multiplexer using logic gate	18-19	3-11-22	fir	
7	Bread board implementation of binary adders	20-22	10-11-22	Rn 17-11-22	



Objective - Bread board implementation of different AND, OR, NOT, NAND, NOR and XOR.

Apparatus required - Bread board wires Logic Trimmers and ICs.

Theory -

1. AND gate (IC-7408) -

The AND gate is a logic circuit that has two or more inputs and one output. If any of the input is 0 or low then the output will be 0 and if both the input goes low or high the output will be corresponding low or high.

2. OR Gate (IC-7432) -

The OR gate has been two or more inputs but only one output. If any input signal is high or the output is one and if both the input is 0 then output will be 0. The OR gate can have as many inputs as desired.

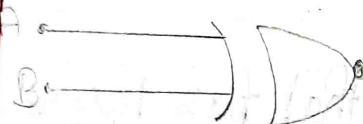
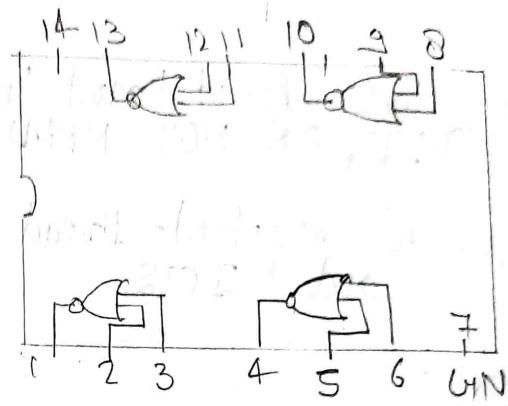
3. NOT Gate (IC-7404) -

The NOT gate is the simplest form of digital logic circuit. The other name of this gate is inverter gate. The output state is always opposite to the input state. If input is 0 then the output is 1 and vice versa.

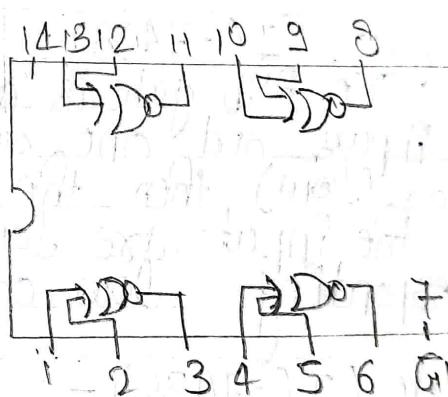
Teacher's Signature : _____



$$Y = \overline{A} + B$$



$$Y = A \oplus B$$



4. NAND Gate (IC 7400) - The NAND Gate is an improved logic element used for implementing decision making logic functions. The NAND Gate is in fact a NOT-AND gate.
5. NOR Gate (IC - 7402) - The NOR gate is an improved logic element used for implementing decision making logic functions. The nor gate is in fact a NOT OR gate.
6. XOR Gate (IC - 7486) -
The XOR gate works as logical "either/or". The output is high if either input is high and output is low when either both inputs are high or both are low.

Observation Table -

AND gate truth table

Input		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

Teacher's Signature : _____



OR gate truth table -

Input		Output
A	B	$y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate truth table -

Input		Output
A	B	Output
0		1
1		0

NAND gate truth table -

Input		AB	Output
A	B	$y = \bar{AB}$	
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

Teacher's Signature :

Name of Experiment..... Date.....
 Experiment No..... Experiment Result.....

Page No 11

NOR gate truth table -

Input		$A+B$	Output $Y = \bar{A} + \bar{B}$
A	B	0	1
0	1	1	0
1	0	1	0
1	1	1	0

XOR gate truth table

Input		$A \oplus B$	Output $Y = A \oplus B$
A	B	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Result - All the truth tables of all the basic gates are verified.

Precautions -

1. All connections should be tight.
2. All instruments should be of proper range.

RsL

Teacher's Signature :

1. Implementation using NAND gate (Part 1 of 3)

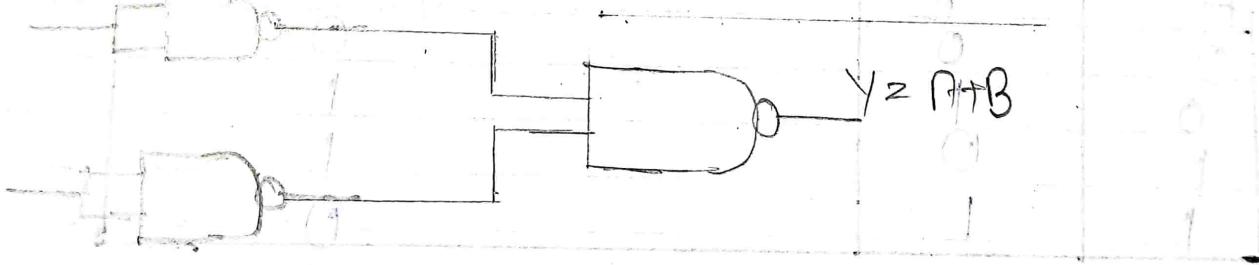
(a) NOT gate



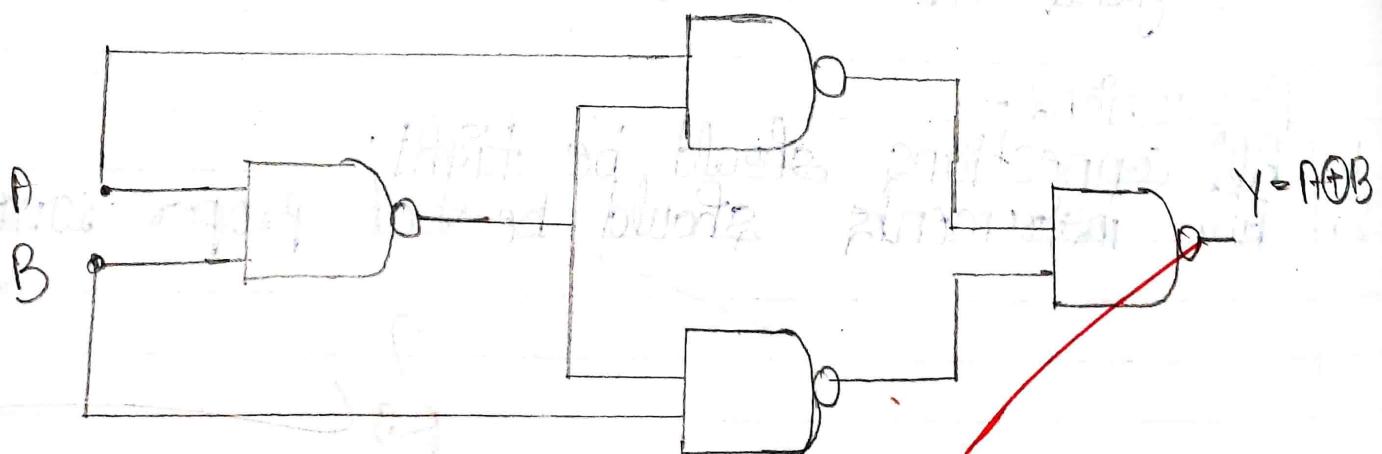
(b) AND gate



(c) OR gate (Part 2)



(d) XOR gate (Part 3 of 3) - follow next step





Name of Experiment.....

Date.....

Experiment No..... 2

Experiment Result.....

Page No. 5

Experiment - 2

Object- To realize all logic gates using NAND and NOR gates.

Apparatus required- IC 7400, IC 7400, Digital Trainer kit, Bread board.

Observation Table-

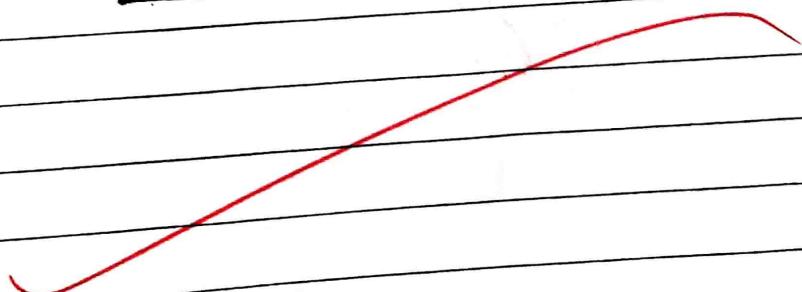
I. Implementation using NAND gate-

a) NOT gate-

A	Y=A'
0	1
1	0

(b) AND gate

A	B	X=A.B
0	0	0
0	1	0
1	0	0
1	1	1



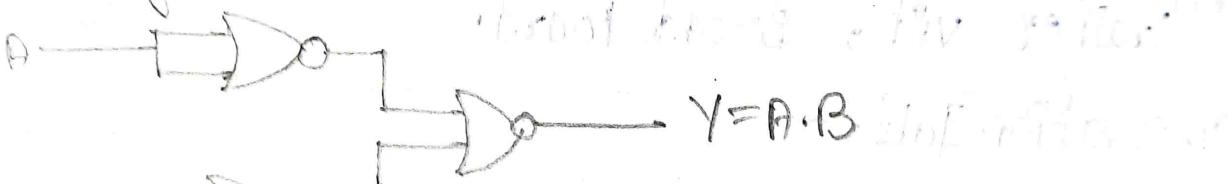
Teacher's Signature :

2. Implementations using NOR gate

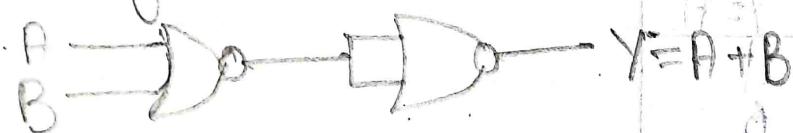
(a) NOT gate



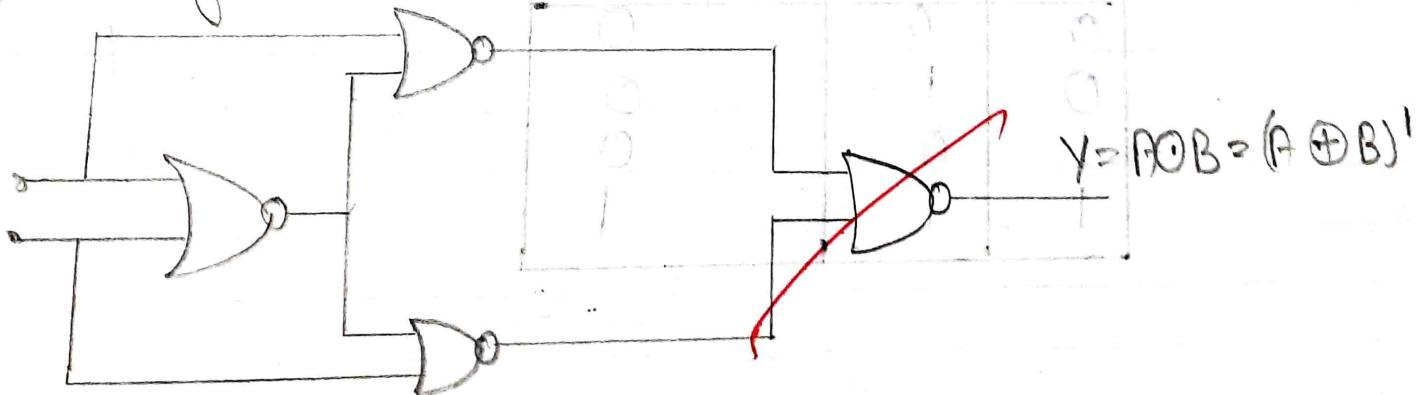
(b) AND gate



(c) OR gate



(d) XNOR gate





Name of Experiment.....

Date.....

Experiment No.....

Experiment Result.....

Page No **6**

c) OR gate -

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

d) XOR gate -

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

2. Implementation using NOR gate -

a) NOT gate -

A	$Y = \bar{A}$
0	1
1	0

b) AND gate -

A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

Teacher's Signature :



Name of Experiment.....

Date.....

Experiment No.....

Page No. 7

Experiment Result.....

(c) OR gate

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(d) XNOR gate -

A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Precautions -

1. Connections must be tight on the bread board
2. Identify the pins IC correctly
3. Take care while removing and inserting the IC on bread board.

Result - Realized all basic logic gates using
NAND or NOR gates.

✓ ✓

Teacher's Signature :

Experiment no-3

Objective - Implementation of Half adder and Full adder using logic gates.

Apparatus required -

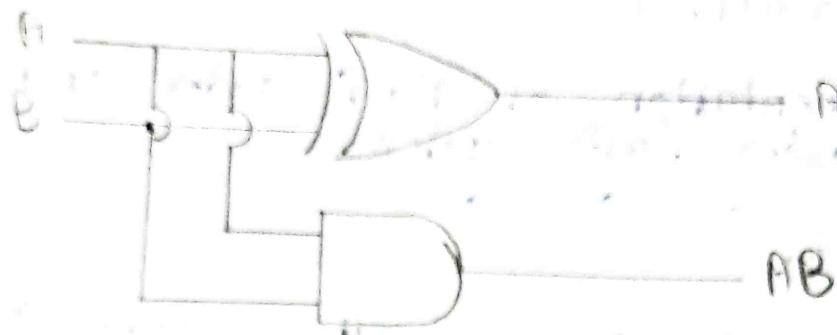
S.NO	Apparatus	Specification	QTY
(i)	IC-7408	AND GATE	1
(ii)	IC-7432	OR GATE	1
(iii)	IC-7486	XOR GATE	1
(iv)	Bread board	-	1
(v)	Jumper wires	-	Adsp
(vi)	LED	-	1
(vii)	Power Supply	+5V	1

Theory -

(i) **Half Adder** - The most basic digital arithmetic circuit is the addition of two binary digits. A combinational circuit that performs the arithmetic addition of two bits is called a Half Adder. The input variables of a half adder are called the augend and addend bits. The output variables are the sum and carry.

Teacher's Signature :

Circuit diagram of Half Adder-



Circuit Diagram of Full Adder-

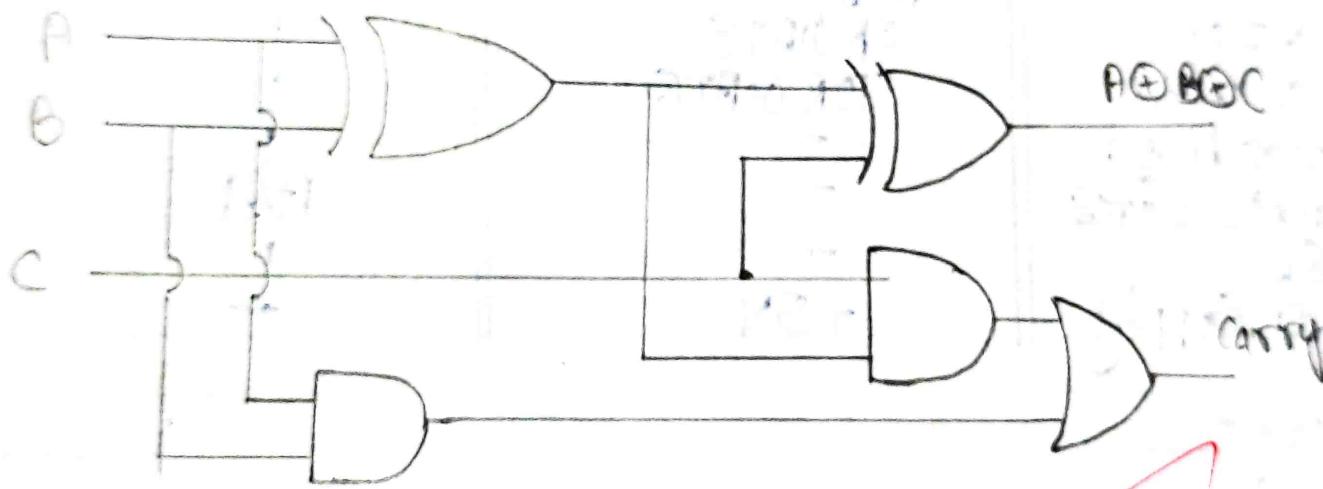
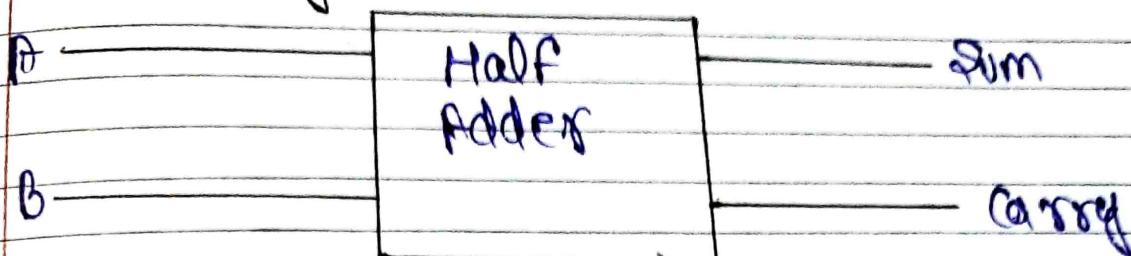


Diagram of Full Adder
Half adder can be used to add two bits and the sum will be given by the formula $S = A \oplus B$ and the carry will be given by the formula $C = A \cdot B$. Now if we want to add more than two bits then we have to use full adder. In full adder we have three inputs A, B, and C. Input A and B are given to the first OR gate and its output is given to the second OR gate along with the third input C. The output of the second OR gate is the sum and the output of the first OR gate is given to the third AND gate along with the input C. The output of the third AND gate is the carry.

Block diagram -



Truth Table -

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Equation -

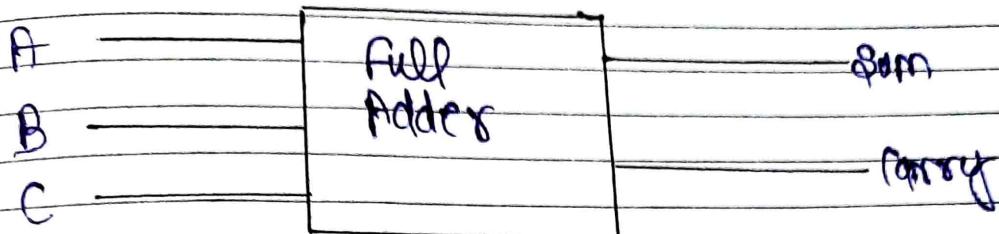
$$\text{Sum} = \overline{A}B + A\overline{B} = A \oplus B$$

$$\text{Carry} = AB$$

2. Full Adder - A full adder is a combinational circuit that forms the arithmetic sum of the three input bits. It consists of three inputs and two outputs. So that two half adder is required to implement a full adder.

Teacher's Signature :

Block diagram -



Truth Table -

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equation -

$$\begin{aligned}
 \text{Sum} &= \cancel{ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC} \\
 &= \cancel{A(CBC + BC)} + \cancel{A(\bar{B}\bar{C} + BC)} \\
 &= \cancel{\bar{A}(B \oplus C)} + A(CBC + BC) \\
 &= A \oplus B + C
 \end{aligned}$$

$$\begin{aligned}
 \text{Carry} &= \cancel{ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC} \\
 &= \cancel{C(\bar{A}B + AB)} + \cancel{ABC(\bar{C} + C)} \\
 &= \cancel{C(A \oplus B)} + AB
 \end{aligned}$$

Teacher's Signature : _____

Name of Experiment.....

Date.....

Experiment No.....

Experiment Result.....

Page No. (1)

Result - Both Half adder and full adder are implemented using different logic gates.

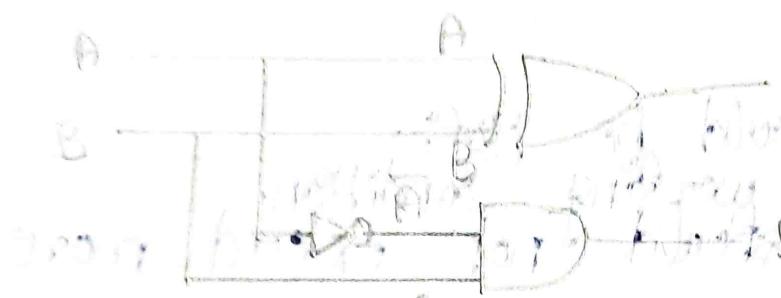
Precaution -

- (i) All connection should be tight.
- (ii) IC should be in working condition.
- (iii) Power supply should not exceed more than 5V

for safety

for

Teacher's Signature :



Half Subtractor

Difference
 $A \oplus B$

Borrow
 $\bar{A}B$

Objective - To implement half subtractor and full subtractor

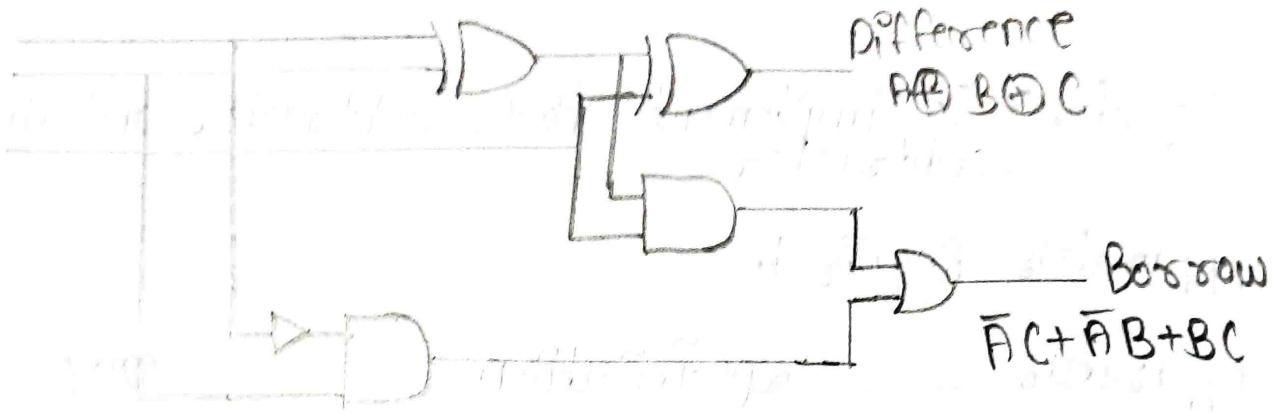
Apparatus Required:

Apparatus	Specification	QTY
(i) AND Gate	IC 7408/74117	1
(ii) X-OR Gate	IC 7486	1
(iii) NOT Gate	IC 7404	1
(iv) OR Gate	IC 7432	1
(v) Powerfull supply +5V		1
(vi) Bread Board		1
(vii) LED		1
(viii) Connecting wires	ADEQUATE as required	

Theory -

Half Subtractor - The half subtractor constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The output are difference and borrow. The difference can be applied using X-OR Gate and borrow output can be implemented using an AND Gate and an inverter.

Teacher's Signature :



Full Subtractor

Subtracting
difference



Name of Experiment.....

Date.....

Experiment No.....

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Experiment Result.....

Truth Table

A	B	Borrow	Difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Full Subtractor - The full subtractor is a combination of XOR, AND, OR, NOT gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor. The first half subtractor will be C and AB. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term of first is the inverted difference output.

✓

Teacher's Signature :

Truth Table.

A	B	C	Borrow	Difference
0	0	0	0	0
0	0	-	1	1
0	1	0	1	1
0	1	-	1	0
1	0	0	0	1
1	0	-	0	0
1	1	0	0	0
1	1	-	1	1

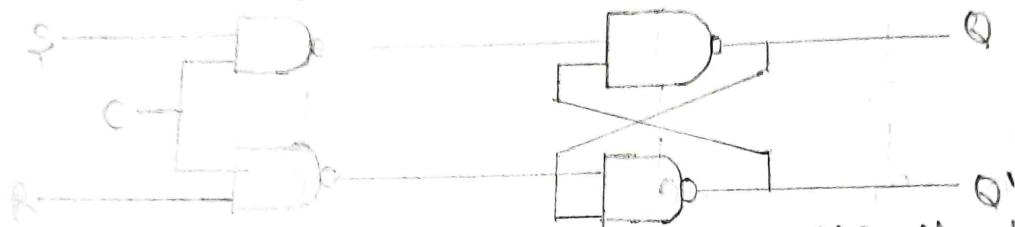
Result - The half subtractor and full subtractor circuits are implemented and verified

Precaution:-

- (i) Switch off the power supply while making connections.
- (ii) All the connections should be made properly before your circuit checked either by faculty or by lab assistance before you switch on the power supply.

Ru

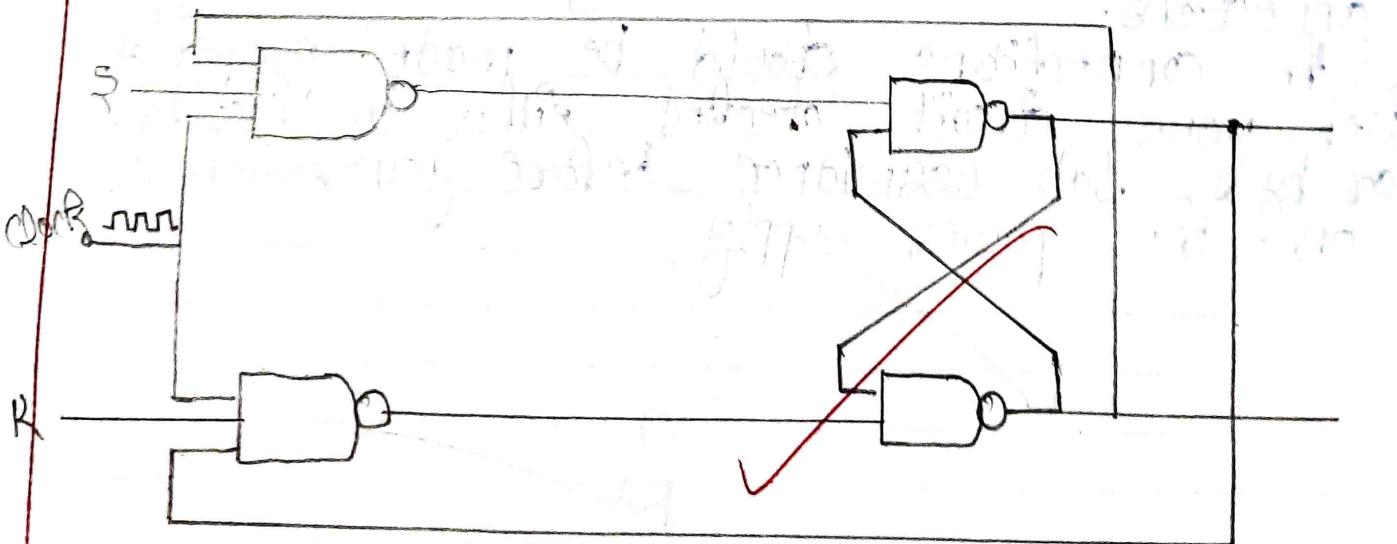
Teacher's Signature :



(Logic diagram of SR - flip flop)

Truth table

C	S	R	Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$, Reset state
1	1	0	$Q = 1$, Set state
			Indeterminate



(JK flip flop)

Experiment - 5

Objective - Bread board implementation of Flip flop (SR, JK, D)

Apparatus required - NAND gate, power supply, Bread board, LED, wires.

Theory - Flip flop are basic fundamental building block of digital system. Flip flop is binary storage device that can store only 1 bit of data. It has property to remain same in one state until it is directed by input signal to switch over the state.

There are 4 types of flip flops

SR (Set Reset)

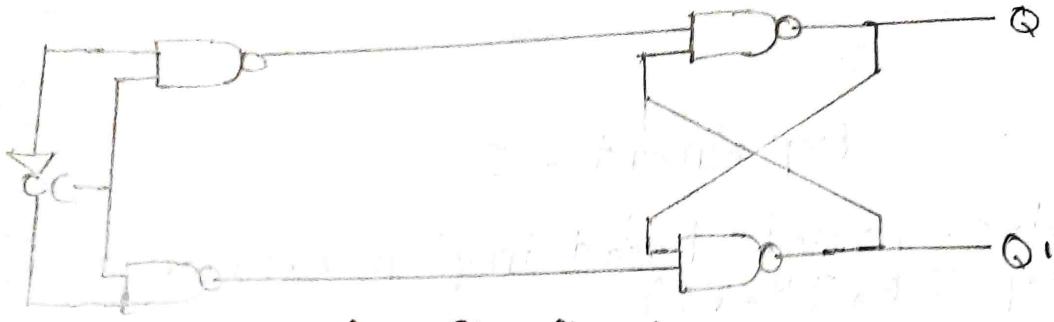
D (Data or Delay)

JK (Toggle)

JT

~~SR flip flop - SR flip flop consists of two cross coupled NAND gate. A clocked SR flip flop has an additional clock input so that S and R input are active only when clock is high when clock goes low state of flip flops can not change.~~

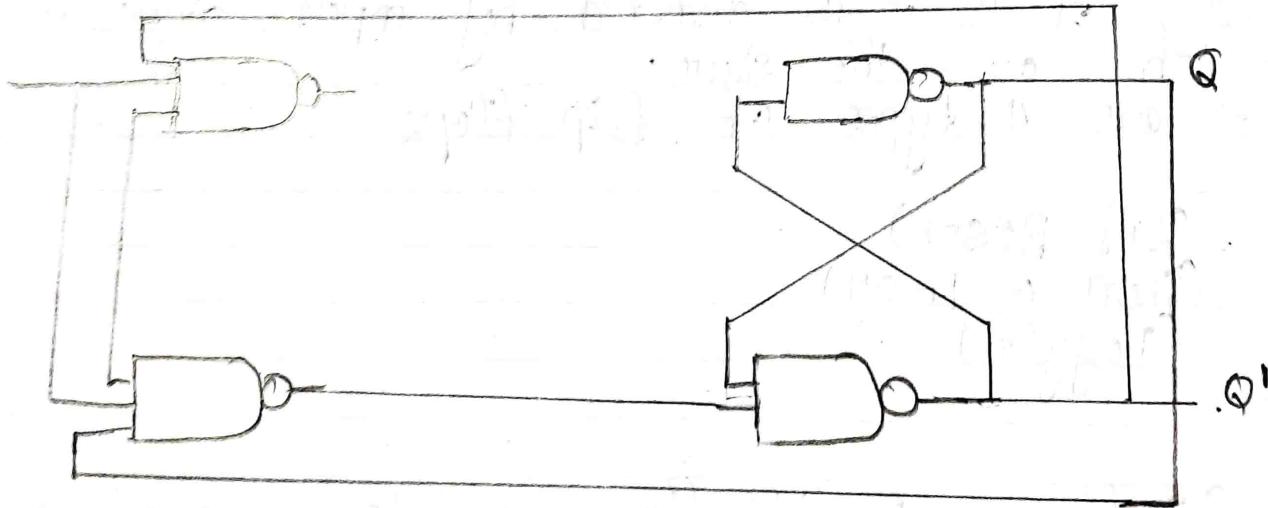
Teacher's Signature : _____



(D-Flip Flop)

Truth Table -

C	D	Q
0	X	X (No Change)
1	0	$Q = 0$, R set
1	1	$Q = 1$, Set



Truth Table -

T	Q _n	Q _{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



JK flip-flop - JK flip flop is similar to SR flip flop has two basic problem then to overcome these problem , JK flip flop was develop.

In JK flip flop two input NAND gate are required with three input NAND gate . Third input of each gate is connected to the output of Q and \bar{Q} .

Truth table for JK flip flops -

J	K	Clock	Q
0	0	↓↑	Q (nonchange)
0	1	↓	0
1	0	↓	1
1	1	↓	Q (Toggle)

D flip flop - D flip flop is most important flip flop from other clocked types . It ensure that same time both input never equals to 1 . If it is designed using gate . SR flip flop with an inverter connected between input allowing for a signal input . D is referred as Data , when data input set 1 flip flop would be set , when 0 set to 0 flip flop would change .

Teacher's Signature :



Name of Experiment.....

Date.....

Experiment No.....

Experiment Result.....

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T flip flop - T stands for toggle. T flip flop has only one input constructed by connecting input of JK flip flop.

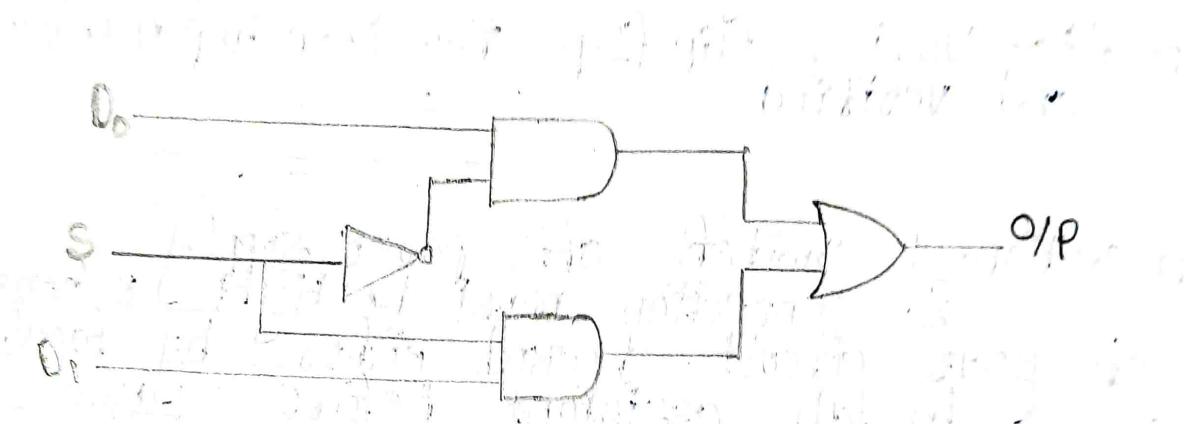
Result - Various flip flop has been implemented and verified

- Precaution -
1. Switch off power supply
 2. Connection must be tight & neat
 3. Get your circuit checked either by faculty or by lab assistant before you switch on the power supply.

Rn

Teacher's Signature :

Two to one Mux is a logic circuit which takes two data inputs and one select input and produces one output.



Logic Circuit of Two to One Line Mux

Truth table

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



Name of Experiment.....

Date.....

Experiment No. 6

Experiment Result.....

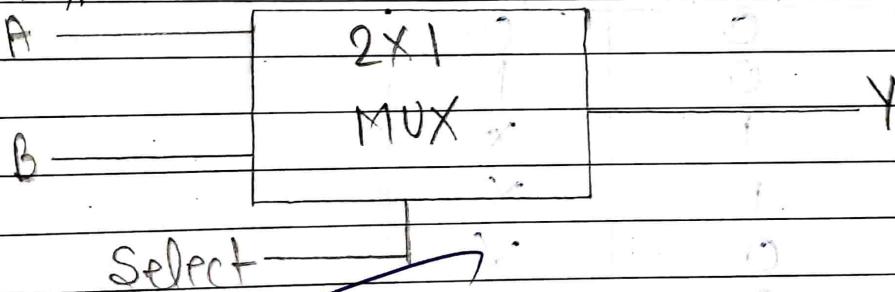
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Objective - Design 2×1 and 4×1 multiplexers using logic gates.

Theory -

• Multiplexer - A multiplexer is a network that has many inputs and one output and the value of the output will be the value of one of inputs which will be decided by some select lines. The simplest type of multiplexer is the two line to one line data multiplexer.

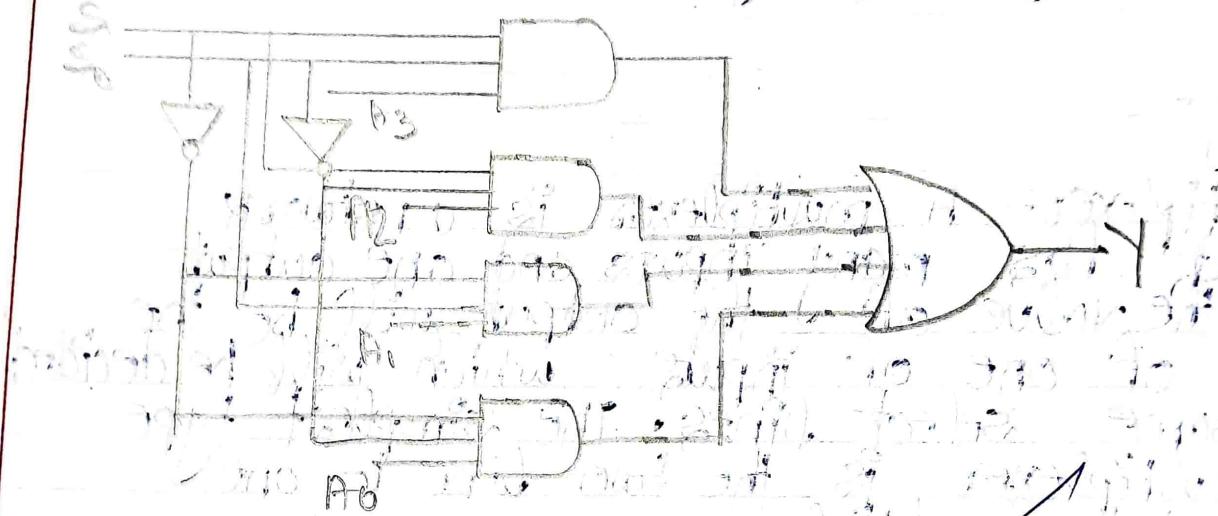
2×1 MUX -



Expression : $F(A, B, C) = \bar{A}C + \bar{B}C + A\bar{B}C$

Teacher's Signature :

4 to 1 Multiplexer Circuit diagram



Truth Table -

S ₀	S ₁	Y
0	0	0
0	1	1
1	0	1
1	1	0

Name of Experiment.....

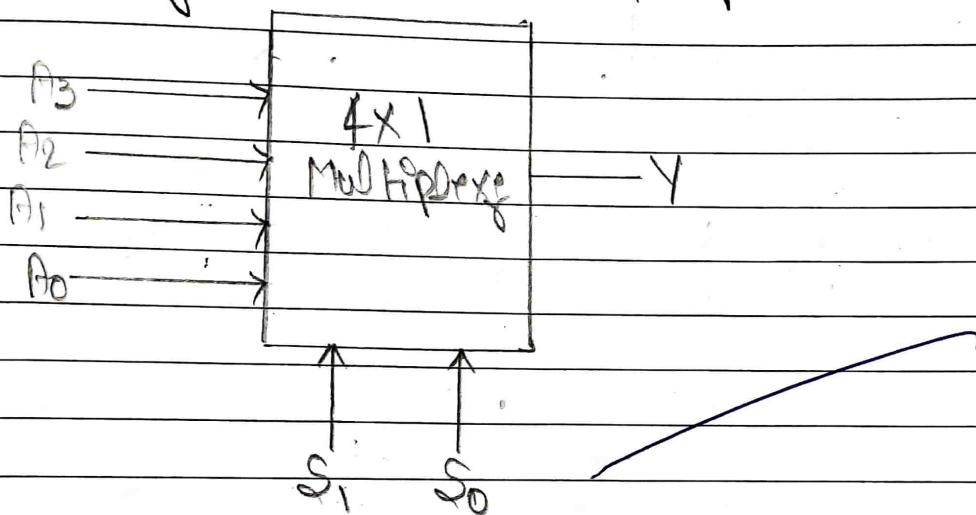
Date.....

Experiment No.....

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4x1 Multiplexer - A 4 to 1 MUX contains four input lines and these are D₀, D₁, D₂ and D₃. Two selected lines S₀ and S₁ and one output Y-line.

Block diagram of 4 to 1 Multiplexer -



Expression -

$$Y = S_1 \bar{S}_0 A_0 + \bar{S}_1 S_0 A_1 + S_1 \bar{S}_0 A_2 + S_1 S_0 A_3$$

Result - 2 to 1 and 4 to 1 multiplexers implemented successfully.

Rizwan

Teacher's Signature :



Name of Experiment.....

Experiment No.....

Date..... 10-11-22

Experiment Result.....

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Experiment No - 7

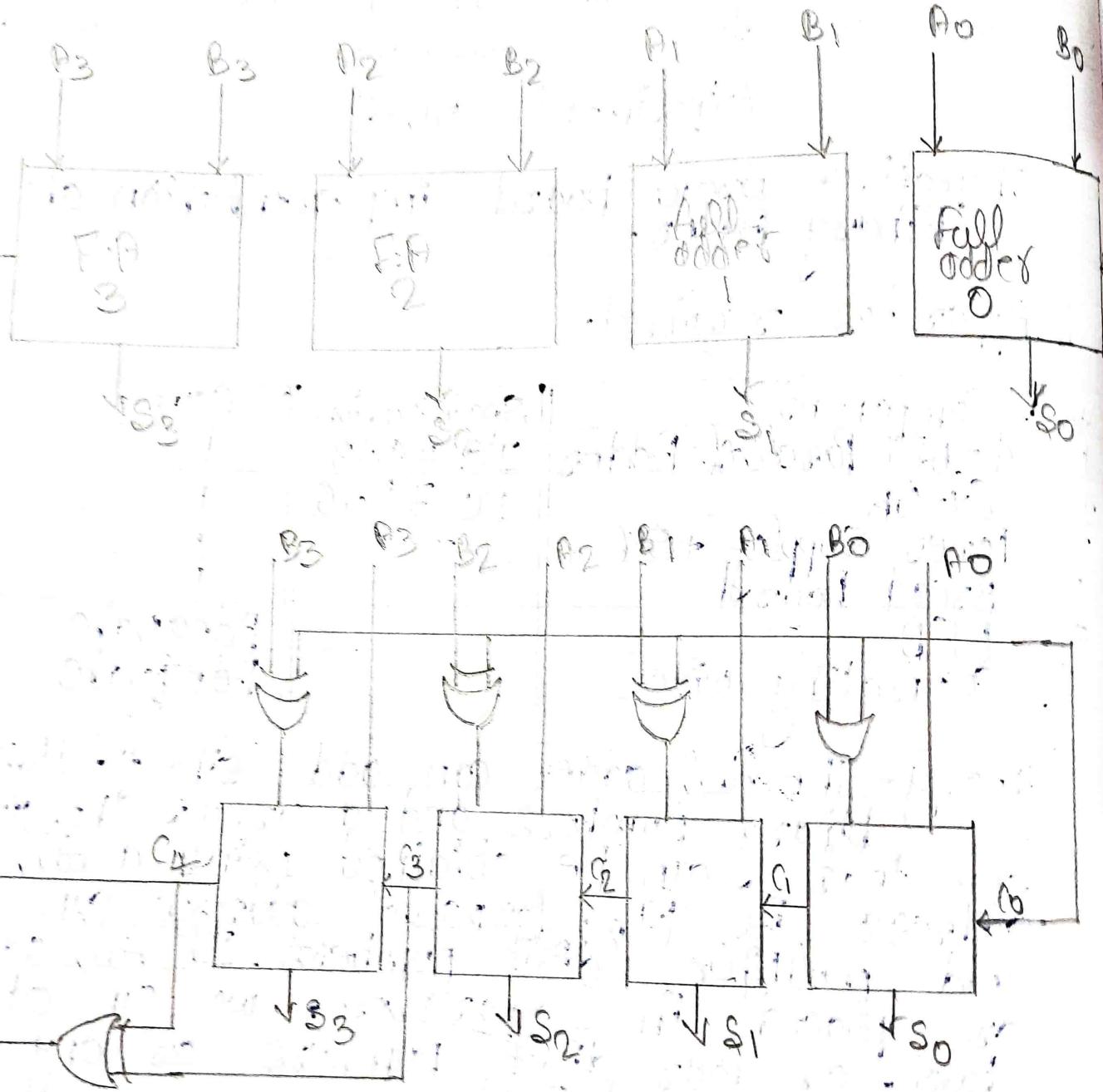
Objective- Bread board implementation of
Binary Adder.

Apparatus required.

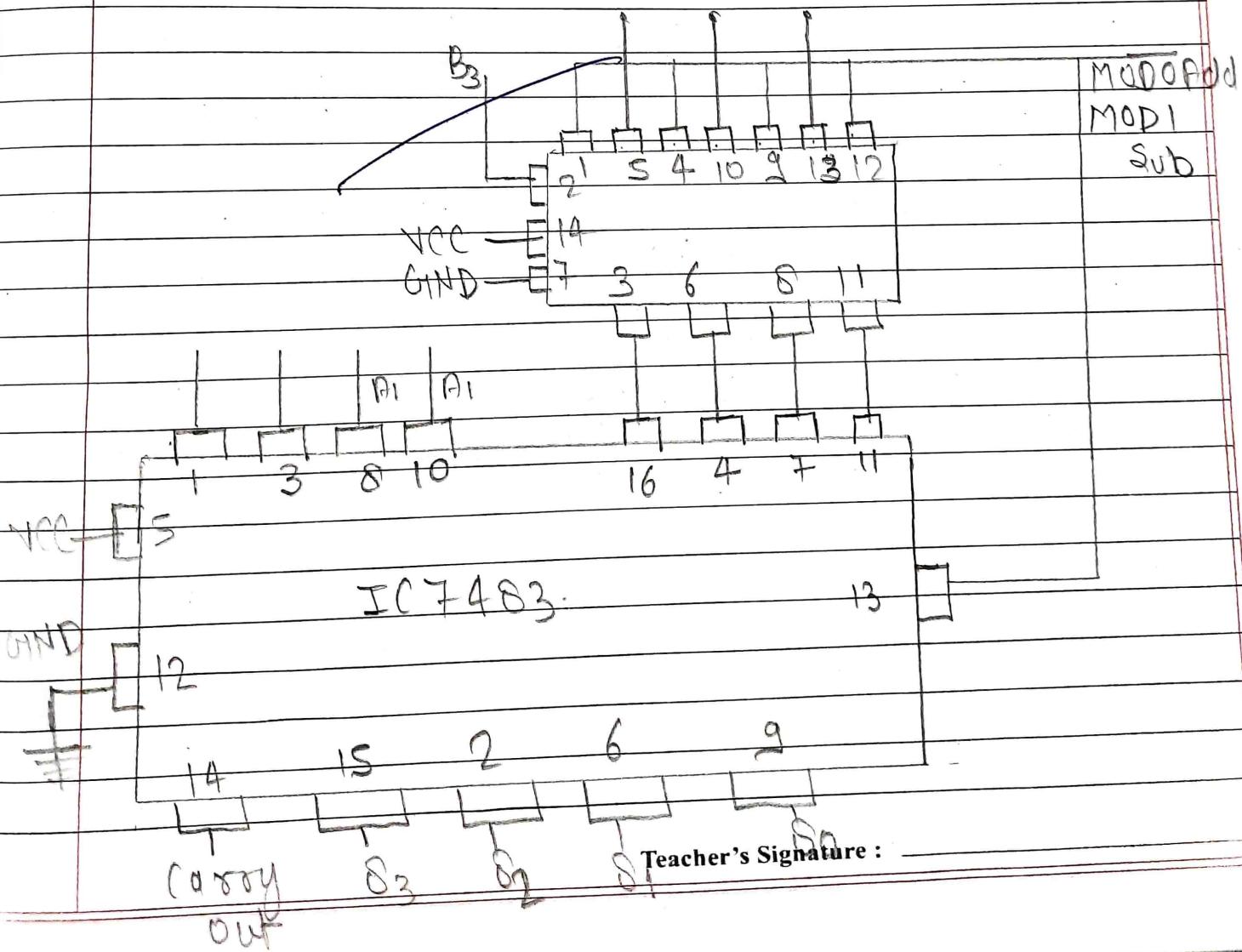
S.NO.	Component	Specification	Q'TY
1	4-BIT Parallel Adder	IC 7483	1
2	EX-OR	IC 7486	1
3	Power Supply +5V	-	1
4	Bread board	-	1
5	LED		Adequate
6	Connecting wire		Adequate

Theory- The full adder can add single-digit binary numbers and a carry. The largest sum that can be obtained using a full adder is 11_2 . Parallel adders can add multiple digit numbers. If full adders are placed in parallel, we can add two- or four digit numbers or any other size desired.

Teacher's Signature :



Subtraction is performed adding 2's complement of augend and addend by simply taking its complement of augend and taking input carry i.e. Common circuit can be used to perform addition as well as subtraction one input of each Ex-OR gate and input carry to a common terminal known as mode input. This mode input decides whether circuit will perform addition or subtraction. If Mode = 0, it performs addition if Mode = 1 it performs subtraction.



Teacher's Signature :



Name of Experiment.....

Date.....

Experiment No.....

Experiment Result.....

Page No.

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Procedure-

- 1 Connections are given as per circuit diagram
- 2 Logical inputs are given as per circuit diagram
- 3 Observe the output & verify the truth table

Result - Adder/Subtractor function of IC 7483 has been performed & verified.

Precaution -

1. Switch off the power supply while making connections.
2. All the connections should be made properly as per the circuit diagram.
3. Get your circuit checked either by your faculty or by lab assistant before you switch on the power supply.

RN

Teacher's Signature :

Pin diagram -

Output 5

Output 1

Output 0

Output

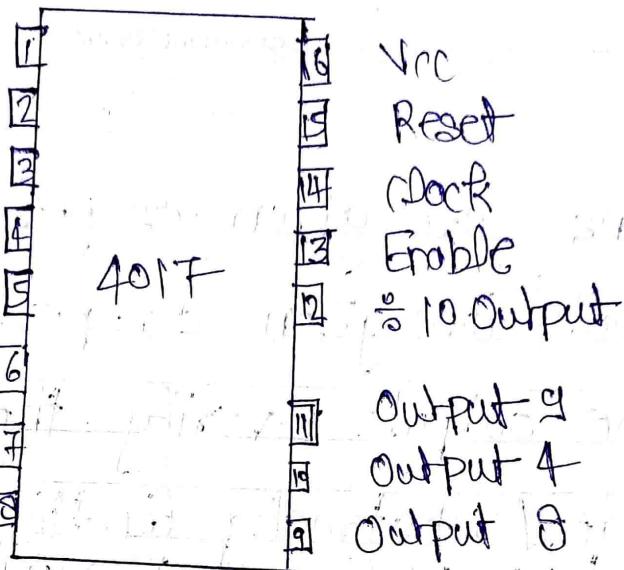
Output

Output 8

Output

Output 3

01



Truth Table -



Name of Experiment.....

Experiment No.....

Date 17-11-22

Experiment Result.....

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Experiment no - 8

Objective - Design of counter (Mod - 10)

Apparatus Required -

S.No	Component	Specification	QTY
1	Counter	IC 4017	1
2	Power supply +5V	-	1
3	Bread board	-	1
4	LED	-	1
5	Connecting wire	ADEQUATE	ADEQUATE

Theory - A BCD counter counts in binary coded decimal from 0000 to 1001 and back to 0000. Because after a count of 9, a BCD counter does not have a regular pattern as in a straight binary count.

Synchronous BCD counters can be cascaded to form a counter for decimal numbers of any length.

Result - The operation of BCD counter has been verified

Precautions - 1. Switch off the power supply while making connections.

Teacher's Signature :



Name of Experiment.....

Experiment No..... 9

Date..... 1-12-22

Experiment Result.....

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Experiment NO - 9

Object - To study of 7 segment decoder.

Apparatus required - Bread board, IC-7447, LED connecting wires.

Theory - IC 7447 is a BCD to decimal decoder which takes BCD as input and convert

It provides seven output pair which delivers data

Truth table for 7 segment

Decimal digit	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Teacher's Signature :



Name of Experiment..... Date.....

Experiment No.....

Experiment Result.....

Page No

Precaution -

1. Connection should be proper and accurate
2. See the LED's output and note it.
3. Check power supply before applying.
4. Verify the truth table

Result - The operation of 7 segment decoder has been verified.

Teacher's Signature :