Printed Pages: **University Roll No: .....**

End Term Examination, Odd Semester 2021-22

B.Tech. CSE/AIML/CSF/CCV/DA/IIoT, II Year, III Semester

BCSC1005: Computer Organization

Time: 3 Hour **Maximum Marks: 50**

Section- A

Note: Attempt ANY FIVE Questions. 5 x 4 = 20 marks

Q1. The 8 bit registers AR, BR, CR, DR initially have the following values.
AR = 11110010 BR = 11111111 CR = 10111001 DR = 11101010

Determine the final 8-bit values in each register after the execution of the following sequence of micro-operations.
AR=AR+BR
CR=CR+1, BR=BR+1
AR=AR-CR

Q2. What do you mean by General register organization? Draw the block diagram of bus organization of GRO having 7 CPU registers.

Q3. Perform the arithmetic operations (+42)+(-13) and (-42)+(-13) in binary using signed-2's complement representation for negative numbers.

Q4. What is hardwired and microprogrammed control unit? Write the control signals for executing the complete instruction XOR R1,R2.

Q5 What do you mean by write-through and write-back? A four-way set associative cache memory uses block of eight words. The cache can accommodate a total of 2048 words from memory. The memory size is 256Kx32. Formulate all the pertinent information for required to construct the cache memory. What is the size of cache memory including valid bit?

Q6. Explain the following:

a. System Bus
b. Memory mapped I/O
c. Isolated I/O
d. Interrupt

Section- B

Note: Attempt ALL Questions. 5 x 3 = 15 marks

Q1. What is instruction cycle? Draw the flowchart for instruction cycle.

Q2. What do you mean by high-impedance state of buses? A computer uses RAM chips of 1024x1 capacity. How many chips are needed to provide a memory capacity of 1024 bytes? How many address lines are required to access 2048 bytes of memory?

Q3. Why I/O Interface is needed? Explain the various I/O commands.

Q4. What is bus arbitration? Differentiate strobe control and handshaking by using suitable figure.

Q5. What is the use of branch instruction? Write the sequence of control steps for executing an unconditional branch instruction.

Section- C

Note: Attempt ANY THREE Questions. 3 x 5 = 15 marks

Q1. What do you mean by pipeline processing? In a certain scientific computation, it is necessary to perform the arithmetic operation Ai*Bi*Ci+Di+Ei with a stream of numbers. Specify a pipeline

configuration to carry out this task. List the content of all the registers in the pipeline for i=1 to 4.

Q2. What do you mean by locality of reference? A computer employs RAM chips of 256x8 and ROM chips of 1024x8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units each with four registers. A memory-mapped I/O configuration used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

a. How many RAM and ROM chips are needed.
b. Give the address range in hexadecimal for RAM, ROM and interface.

Q3. Differentiate programmed I/O and interrupt initiated I/O. Explain in detail the Direct Memory Access (DMA) transfer in a computer system by giving appropriate figure.

Q4. What do you mean by virtual memory? How it is useful for executing any program. A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1K words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is FIFO and LRU.