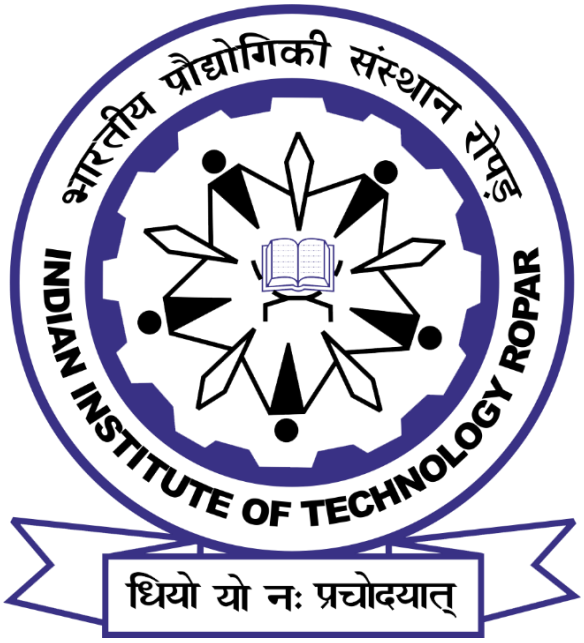
ANALOG CIRCUITS

EE301



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Entry Number: 2022EEB1165

Course Project

AIM:

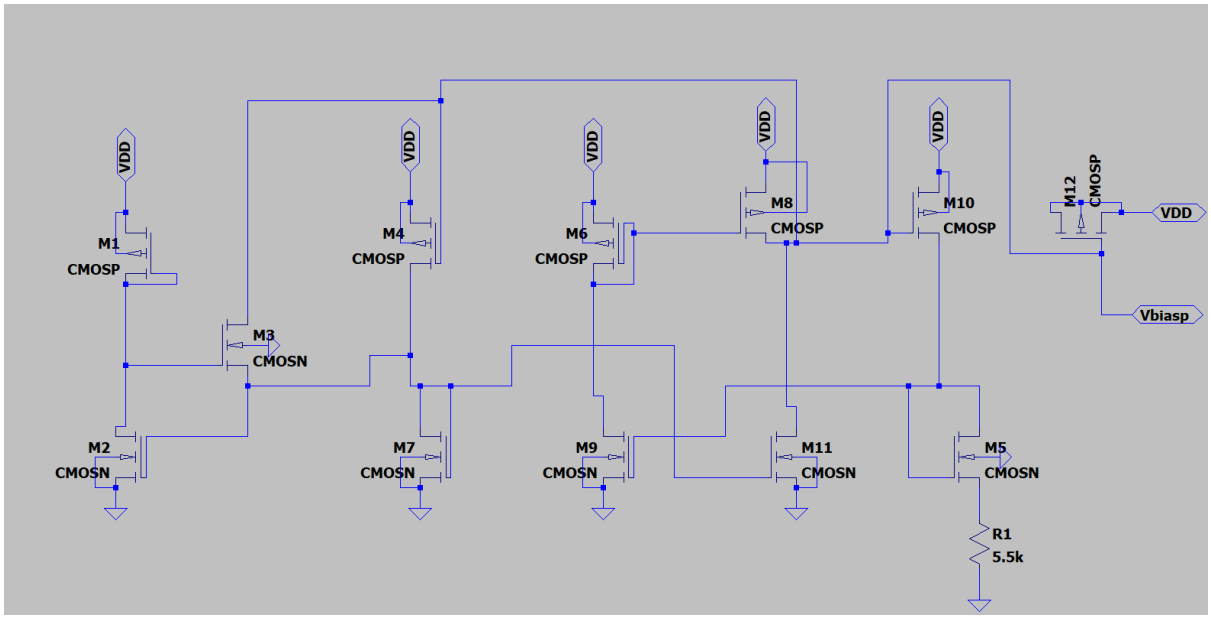
Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice or Cadence and Magic/Cadence tools in 180nm (supply 1.8V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22nm (supply 0.8V) technology node to see the effect of lowering the technology node.

LTSpice Simulations:

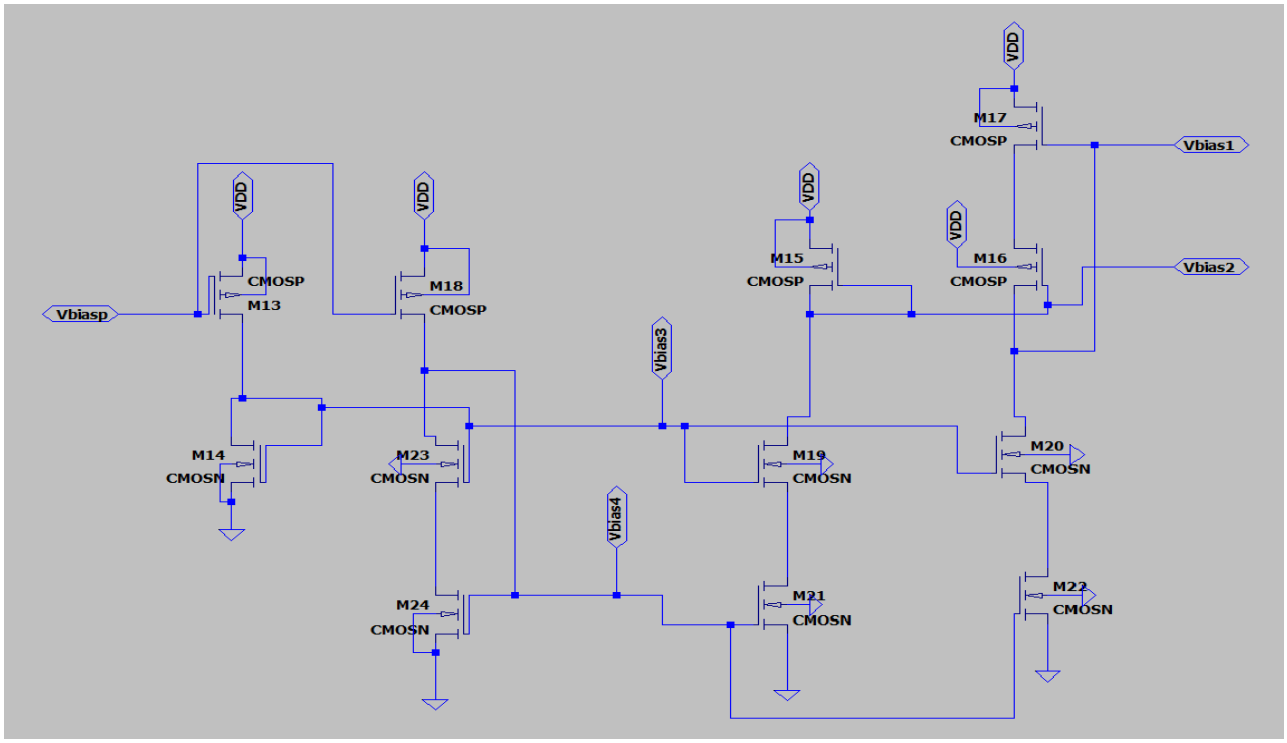
Simulated LTSpice schematics for beta multiplier circuit, cascode current mirror and cascode amplifier for both 180nm and 22nm technology files.

- *180nm Technology Simulations*

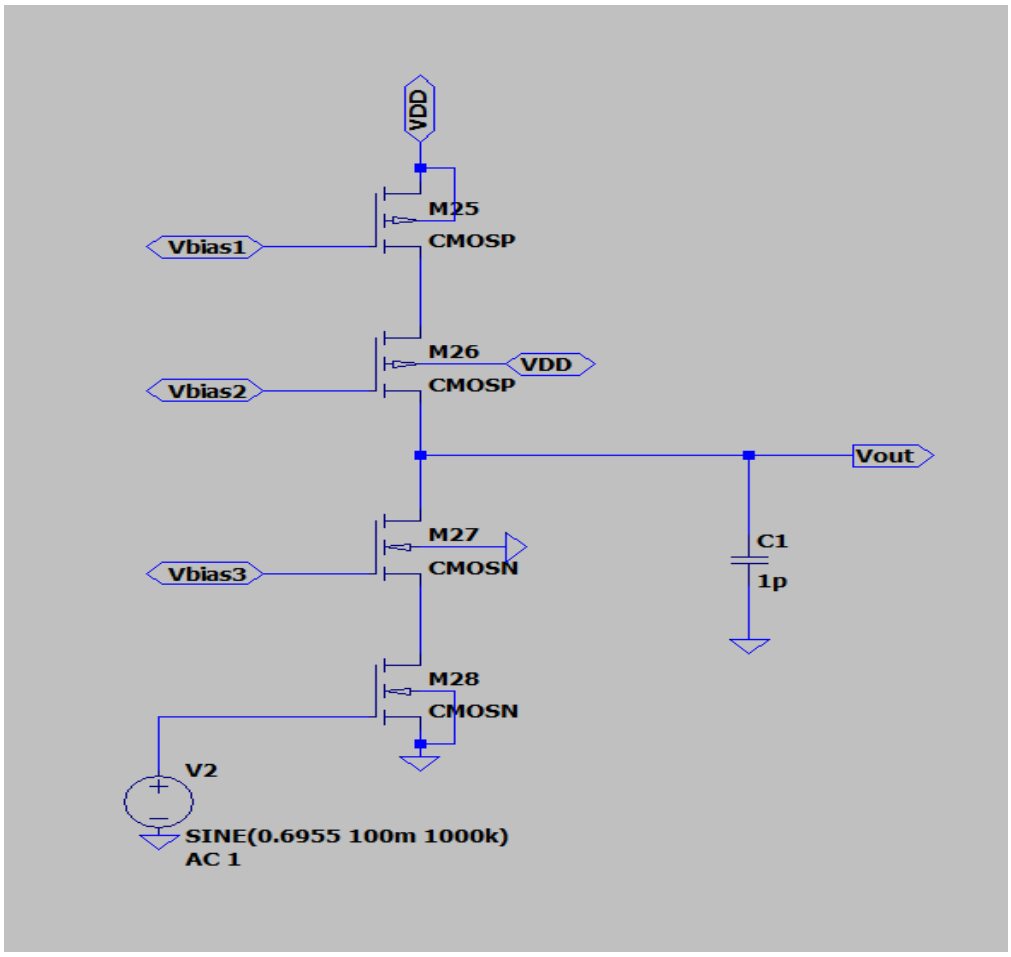
The below LTSpice schematics and respective simulations are set to perform according to the given (W/L) ratios and assigned target specifications for all 3 circuits.



Beta Multiplier Circuit

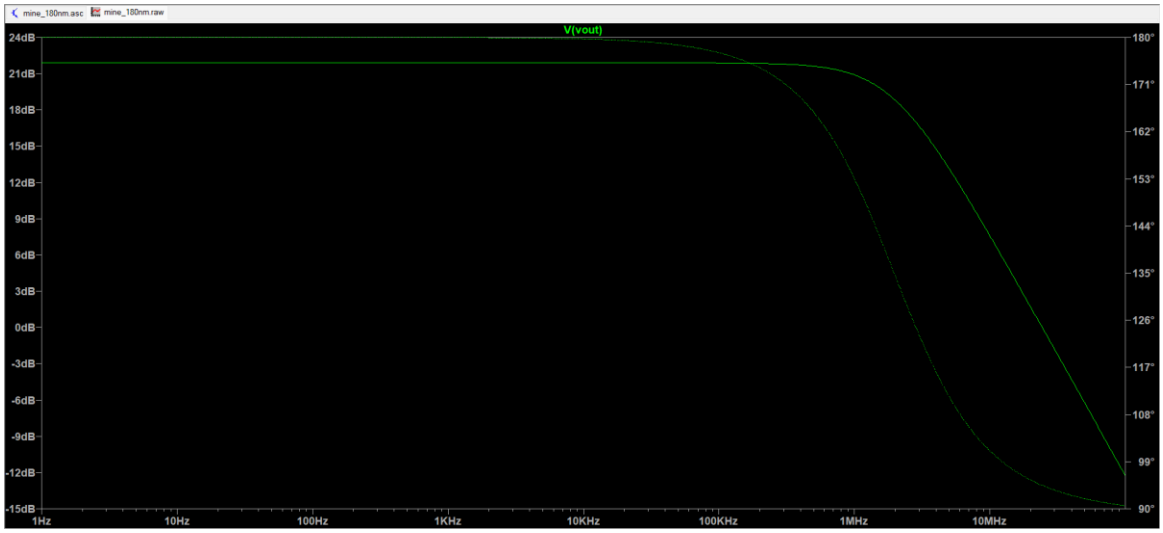


Cascode Current Mirror

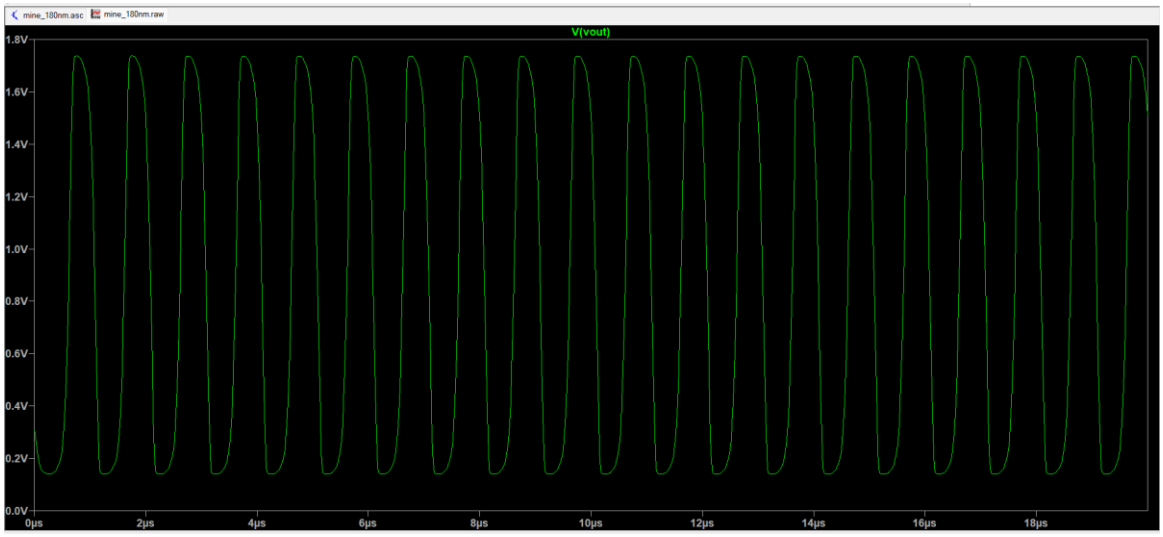


Cascode Amplifier Circuit

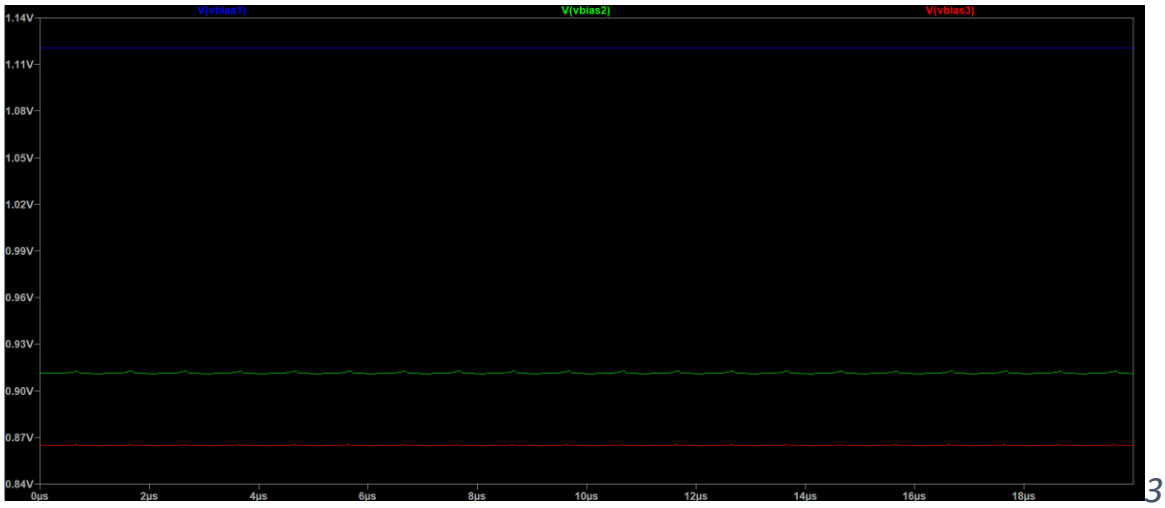
Output Simulations-



1Vout Frequency Plot



2Vout transient



Vbias1, Vbias2, Vbias3 values

Calculations for designing the cascode amplifier for target specifications (180nm tech)

Pago:

180nm Technology-

As per given data, $A_v = 20$ V/V and $C_L = 1pF$ (Capacitive load)

$V_{DD} = 1.8V$

Frequency of pole (let) = 2.4 MHz

$$R_{out} = \frac{1}{2\pi f C_L} = \frac{1}{2\times 3.14\times 2.4\times 10^6 \times 10^{-12}} = 0.663148\times 10^6$$

$$\Rightarrow \boxed{R_{out} = 66314.8\ \Omega}$$

And, $$g_m = \frac{A_v}{R_{out}} = \frac{20}{66314.8} = 0.0003015\ S$$

Since, $g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{th})$

As per given values $\rightarrow$ $\mu_n C_{ox} = 2(175.4) = 350.8\ \mu A/V^2$

$\mu_p C_{ox} = 2(35.6) = 71.2\ \mu A/V^2$

For finding V_{ov}; we are considering all MOSFETs at the edge of saturation (i.e, $V_{DS} = V_{GS} - V_{th}$)

$(V_{ov} = V_{DS})$

By taking 0.2 V drop across each MOSFET

For NMOS - M_4 → $V_D = 0.2\,V$, $V_S = 0$

$\Rightarrow V_{DS} = 0.2\,V$

$\Rightarrow 0.2 = V_G - V_{th}$ $\{V_{th} = 0.51V\}$

$\Rightarrow \boxed{V_G \leq 0.71\,V}$

For NMOS - M_3 → $V_D = 0.4\,V$, $V_S = 0.2\,V$

$\Rightarrow 0.2 = V_{bias3} - 0.2 - 0.51$

$\Rightarrow \boxed{(V_{bias})_3 \leq 0.91V}$

$\Rightarrow g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n V_{ov}$

$\Rightarrow \left(\frac{W}{L}\right)_n = \frac{(0.000315)}{(350.8)(0.2)} = 4.2973$

$\boxed{\left(\frac{W}{L}\right)_{NMOS} = 4.2973}$

$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} (V_{ov})^2 \left(\frac{W}{L}\right) (1 + \lambda V_{DS})$

$= \frac{1}{2} (350.8)(10^{-6})(0.2)^2 (4.2973)(1 + (0.09)(0.2))$

$\boxed{I_D = 30.622\,\mu A}$

$\rightarrow I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p V_{ov}^2 (1 + \lambda V_{DS})$

$\left(\frac{W}{L}\right)_p = \frac{30.622 \times 10^{-6}}{(0.5)(71.2 \times 10^{-6})(0.2)^2 (1 + (0.09)(0.2))}$

$\boxed{\left(\frac{W}{L}\right)_p = 21.1864}$

For PMOS - M_2

$V_{SD} \geq V_{SG} - V_{th,p}$ $\quad V_S = 1.6V \mid V_D = 1.4V$

$0.2 \geq 1.6 - V_{bias2} - 0.5$

$\Rightarrow \boxed{V_{bias2} \geq 0.89\,V}$

For PMOS - M_1

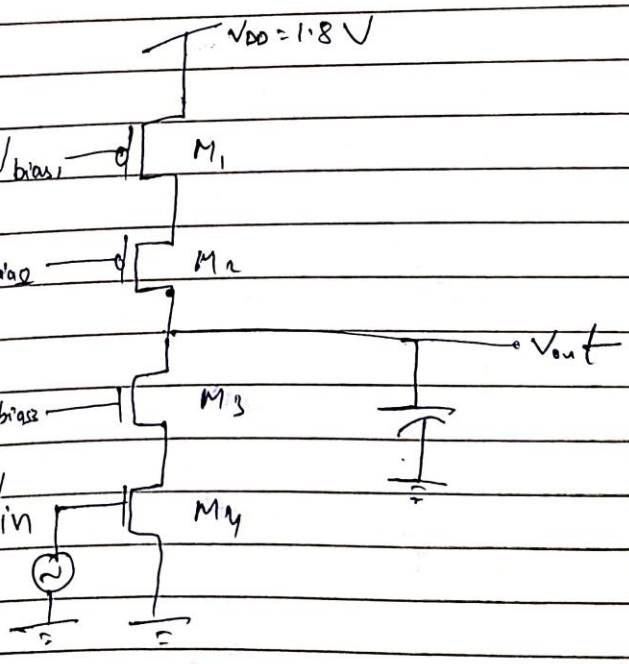
$\Rightarrow 0.2 \geq 1.8 - V_{bias1} - 0.5$ $\quad V_S = 1.8V \mid V_D = 1.6V$

$\Rightarrow \boxed{V_{bias1} \geq 1.09V}$

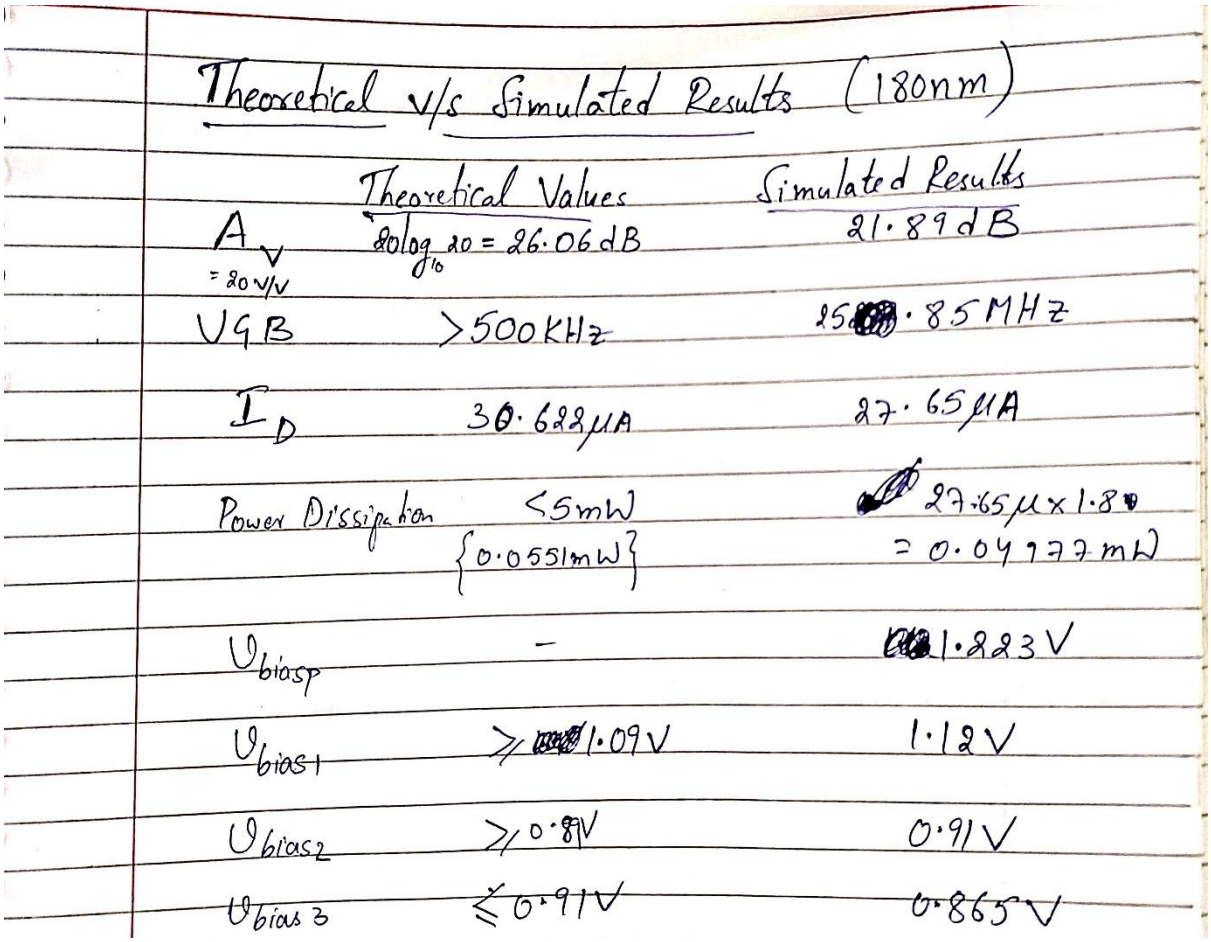
→ Power Dissipation (PD) = $V_{DD} \cdot I_d$

$= (1.8)(30.66)$

$\boxed{PD = 0.0551\,mW}$



Comparing theoretical and simulated values

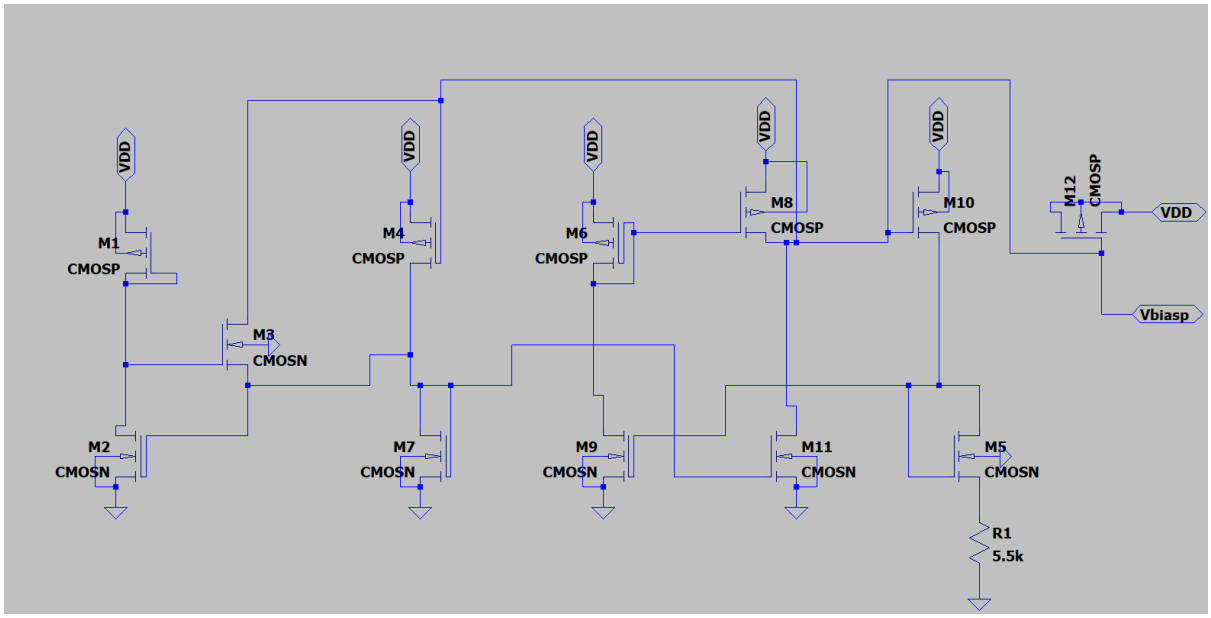


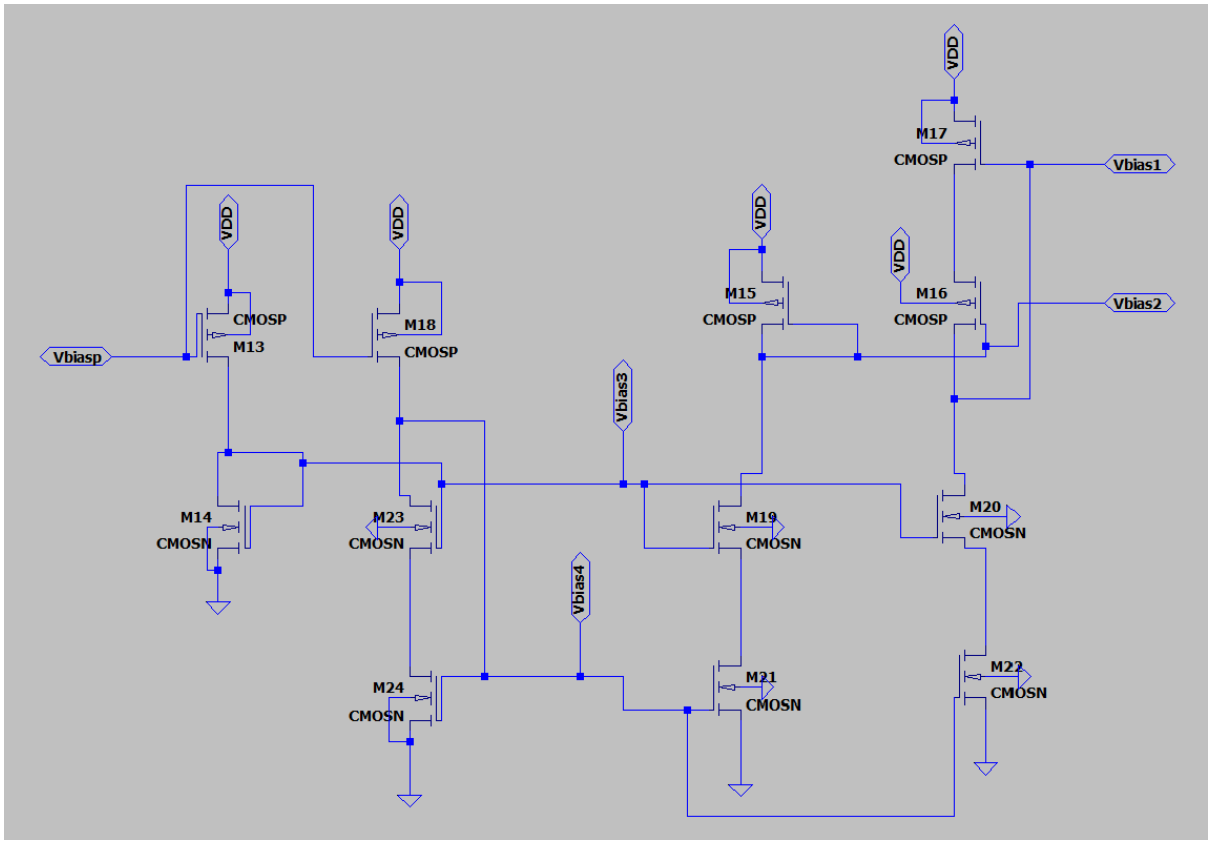
Theoretical v/s Simulated Results (180nm)

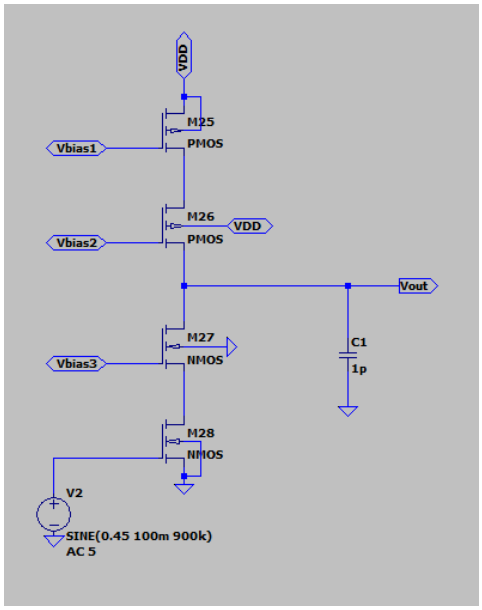
	Theoretical Values	Simulated Results
A_V = 20 V/V	$20\log_{10} 20 = 26.06$ dB	21.89 dB
UGB	> 500 KHz	25[illegible].85 MHz
I_D	30.622 μA	27.65 μA
Power Dissipation	< 5 mW {0.0551 mW}	27.65μ × 1.8 = 0.04977 mW
V_{biasp}	-	[illegible]1.223 V
V_{bias1}	≥ [illegible]1.09 V	1.12 V
V_{bias2}	≥ 0.8 V	0.91 V
V_{bias3}	≤ 0.91 V	0.865 V

❖ *22nm Technology Simulations*

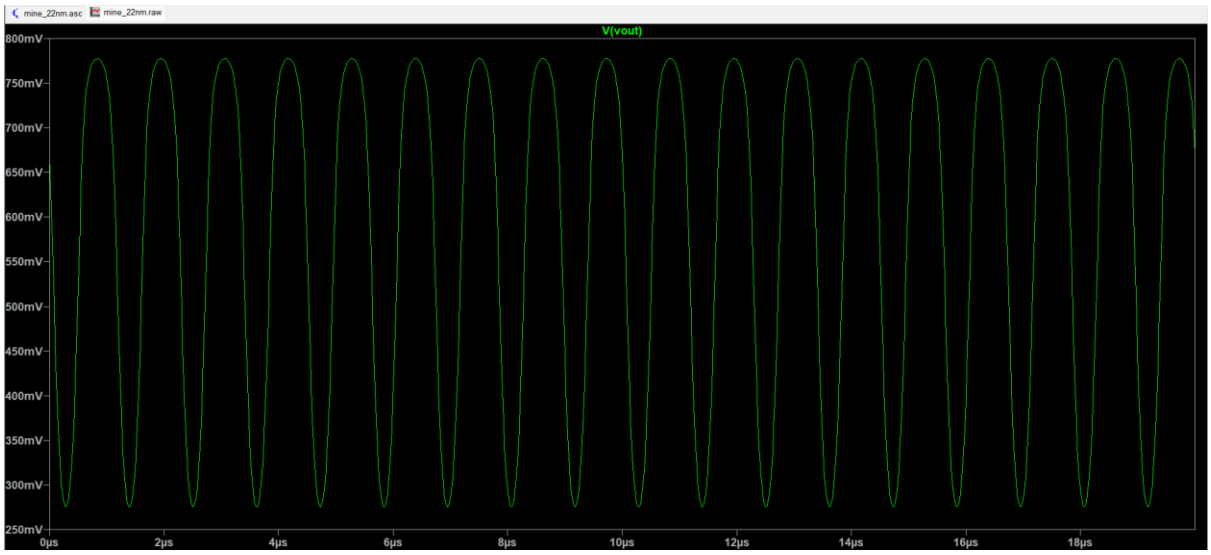
The below LTSpice schematics and respective simulations are set to perform according to the given (W/L) ratios and assigned target specifications for all 3 circuits.

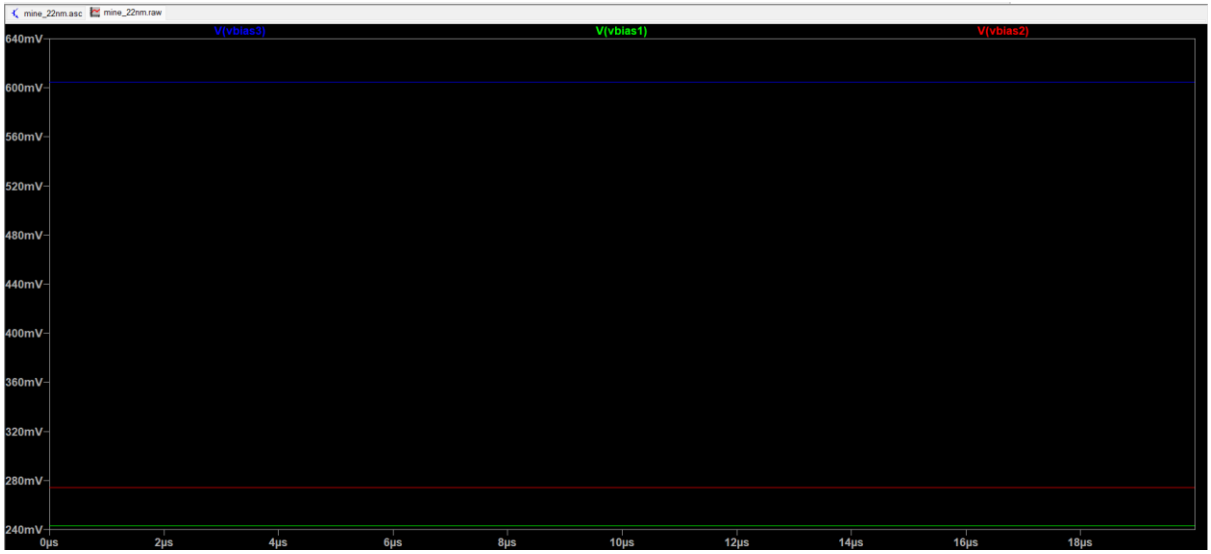

VDD
M1
CMOSP
M3
CMOSN
M2
CMOSN
M4
CMOSP
M7
CMOSN
M6
CMOSP
M9
CMOSN
M8
CMOSP
M11
CMOSN
M10
CMOSP
M5
CMOSN
R1
5.5k
M12
CMOSP
Vbiasp


VDD
M17
CMOSP
Vbias1
Vbiasp
M13
CMOSP
M18
CMOSP
M15
CMOSP
M16
CMOSP
Vbias2
Vbias3
M14
CMOSN
M23
CMOSN
M19
CMOSN
M20
CMOSN
Vbias4
M24
CMOSN
M21
CMOSN
M22
CMOSN



Output Simulations





Calculations for designing the cascode amplifier for target specifications (180nm tech)

As per given data $A_V = 20\ V/V$ and $C_L = 1\ pF$ (capacitive load), $V_{DD} = 0.8V$

$|V_{th}| = 0.3V$

$V_{ov} = 0.2V$

Frequency of pole (1st) $= 2.7\ MHz$

$$R_{out} = \frac{1}{2\pi f C_L} = \frac{1}{2\pi \times 2.7 \times 10^6 \times 10^{-12}} = 58946.27\ \Omega$$

And, $$g_m = \frac{A_V}{R_{out}} = \frac{20}{58946.27} = 0.0003392\ S$$

Since, $$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})$$

As per given values $\rightarrow \mu_n C_{ox} = 100\ \mu A/V^2$

$\mu_p C_{ox} = 50\ \mu A/V^2$

$$\Rightarrow \left(\frac{W}{L}\right)_n = \frac{0.0003392}{(0.2)(100 \times 10^{-6})} = 16.964$$

And, $$I_D = \frac{1}{2} \mu_n C_{ox} (V_{ov})^2 \left(\frac{W}{L}\right)_n \times (16.964)$$

$$= \frac{1}{2}(100 \times 10^{-6})(0.04)$$

$$= 33.928\ \mu A$$

$$\Rightarrow I_D = \frac{1}{2} \mu_p C_{ox} V_{ov} \left(\frac{W}{L}\right)_p$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = \frac{33.928 \times 10^{-6}}{(1/2)(50 \times 10^{-6})(0.04)} = 33.928$$

→ Power Dissipation (PD) = $V_{DD} \times I_D$

$= (0.8)(33.928\,\mu)$

$PD = 27.1424\,\mu W$

$\Rightarrow PD = 0.0271\,mW$

$\left(\frac{W}{L}\right)_n = 16.964$

$\left(\frac{W}{L}\right)_p = 33.928$

{ operating in Saturation region }

→ For NMOS - M4

$V_S = 0$

$V_{DS} = 0.2V$

$V_G = V_{in}$

$\Rightarrow 0.2 \geq V_{GS} - V_{th}$

$\Rightarrow \boxed{V_{in} \leq 0.5V}$

→ For NMOS - M3

$V_D = 0.4V$

$V_S = 0.2V$

$V_{DS} \geq V_{GS} - V_{th}$

$\Rightarrow 0.2 \geq V_{bias3} - 0.2 - 0.3$

$\Rightarrow \boxed{V_{bias3} \leq 0.7V}$

→ For PMOS - M2

$V_{SD} \geq V_{SG} - V_{thp}$

$0.2 \geq 0.6 - V_{bias2} - 0.3$

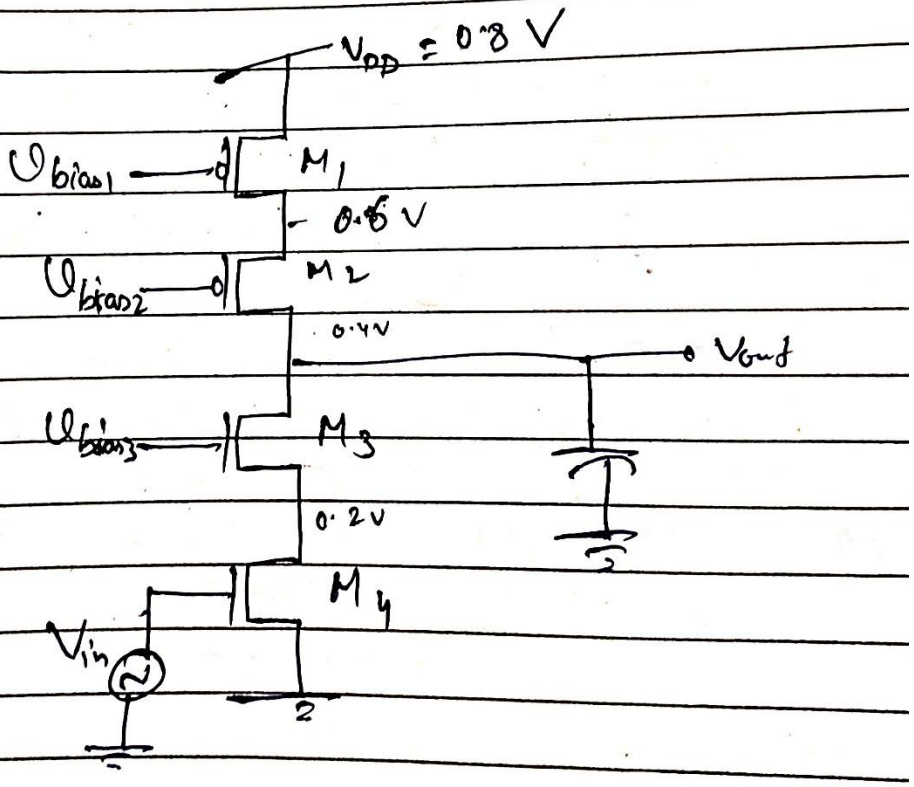
$\Rightarrow \boxed{V_{bias2} \geq 0.1V}$

→ For PMOS - M_1

$$V_{SD} \geq V_{SG} - V_{thp}$$

$$\Rightarrow 0.2 \geq 0.8 - V_{bias1} - 0.3$$

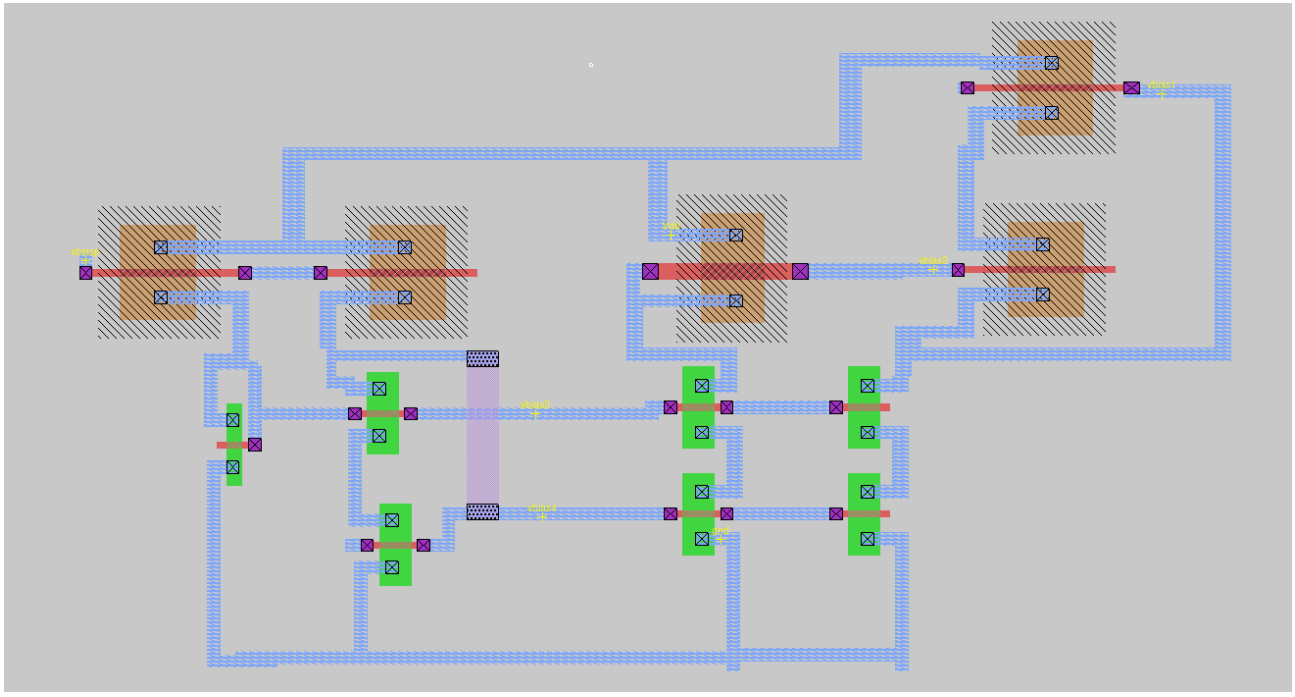
$$\Rightarrow \boxed{V_{bias1} \geq 0.3V}$$



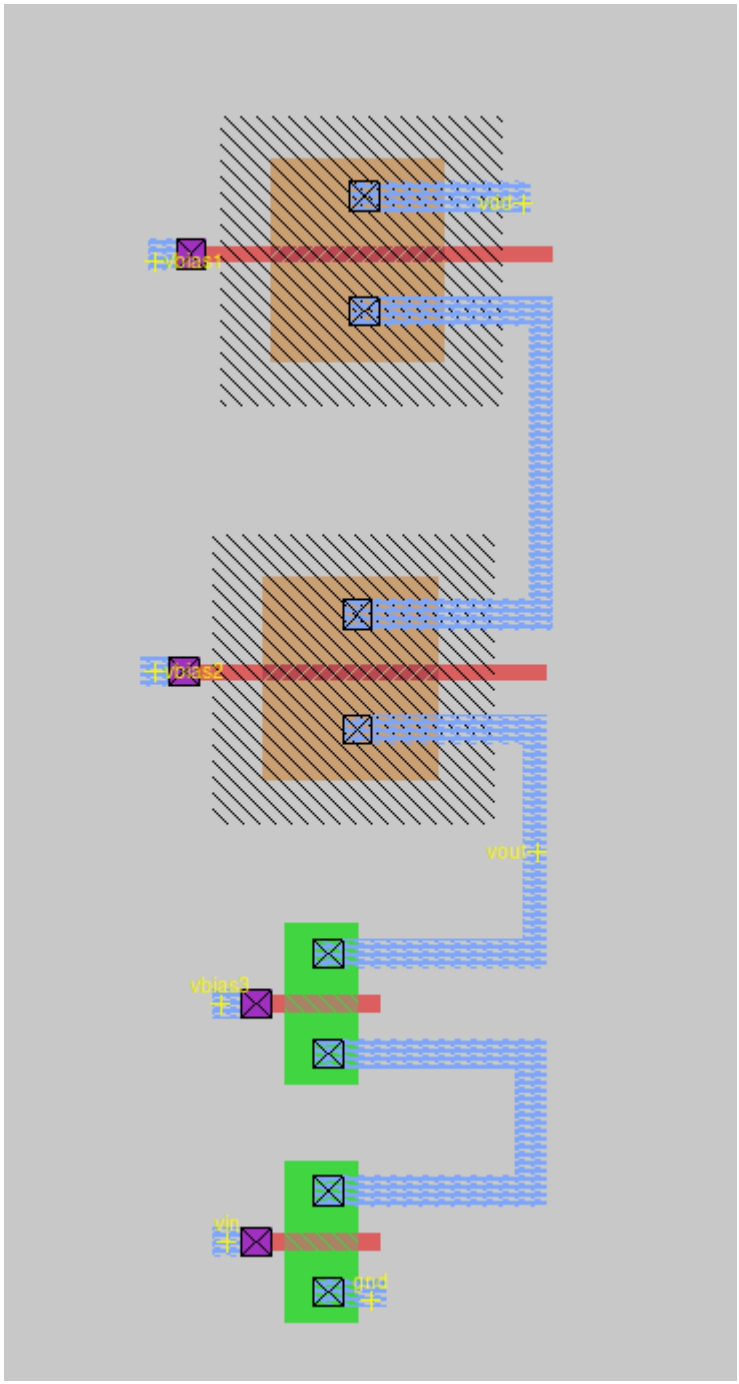
Theoretical v/s Simulated Results (22nm)

	Theoretical Values	Simulated Results
Av (20 V/V)	$20\log_{10} 20 = 26.06$ dB	23.30 dB
UGB	> 500kHz	275 MHz
Power Dissipation	< 5mW {0.027mW}	0.62396 mW
I_D	33.92 μA	29.95 μA
V_{biasp}	-	248.48 mV
V_{bias1}	≥ 0.3V	243.08 mV
V_{bias2}	≥ 0.1 V	274.5 mV
V_{bia3}	≤ 0.7V	604.538 mV

MAGIC LAYOUTS



Current Mirror Circuit Layout



Cascode Amplifier Circuit

Comparison between 180nm and 22nm Technology:

- **Compact Design**: The smaller size of 22nm transistors (roughly 8 times smaller than 180nm transistors) allows for more components on a chip, improving overall performance and efficiency.
- **Manufacturing Complexity**: With the smaller size of 22nm transistors, layouts are more challenging to design, which may result in higher manufacturing costs.
- **Power Efficiency**: 22nm technology requires lower bias voltages and currents, leading to lower power consumption compared to 180nm technology. This makes it a more energy-efficient option for applications requiring low power usage.
- **Heat Dissipation**: Due to reduced power consumption, 22nm technology can contribute to lower heat generation, which helps in maintaining device longevity and performance stability.
- **Higher Frequency Response**: 22nm technology provides a higher Unity Gain Bandwidth, resulting in a higher cut-off frequency. This allows devices to operate at higher speeds and with improved frequency performance.
- **Potential for Increased Density**: 22nm technology can lead to higher density of transistors on a chip, allowing for more functionality and complex designs in a smaller physical space.

Conclusion:

We simulated various components (Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier) on both 180nm and 22nm technology using LTSpice. The simulation results are same as theoretical values and met performance requirements. Additionally, we designed layouts for Cascode Current Mirror and Cascode Amplifier using Magic software for the 180nm technology. This allowed us to compare 180nm and 22nm technology based on LTSpice simulations and layout design in Magic.