Design of power efficient SPI interface

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Abstract- The paper discusses the design of an SPI interface based on the specifications mentioned in the SPI block guide V03.06 by Motorola. The present design incorporates additional power down mode - stop mode for power optimization and the standard design was modified by using clock gating technique for additional power reduction .The shift registers are replaced by double buffer registers to prevent the loss of data due to overflow .Using clock gating in the design has reduced the power of the shift register by 13%. Verilog is used for coding and I-Sim (Xilinx) is used to verify the design performance.

***Keywords*— SPI, master-slave, power down modes, power reduction techniques**

I. INTRODUCTION

Several synchronous serial communication interfaces are being used for on-board communication. Some of these interfaces are inter- integrated circuit (I2C), serial peripheral interface (SPI), and 1-Wire. Out of these interfaces the SPI interface is the one most widely used interface for exchanging data.[1] Some of the applications for which SPI is used are as follows[1]:

1. Used to transfer data from sensors like temperature, pressure etc.
2. Used for communication with Ethernet, USB, IEEE 802.11.
3. Used to exchange data with Flash and EEPROM.
4. LCD displays

The Serial Peripheral Interface (SPI) is a 4-wire interface which has been first designed by Motorola. Later, several other organizations like Texas instruments, digital core design, cadence etc. developed their own SPI devices [2]. All these organizations have followed the basic specifications of the SPI interface and have included some special features to their device to make it unique.

The SPI interface design discussed in this paper is a unique design which follows the basic design specifications of the SPI, with integrated special features present in several variants of SPI which are being used presently. These features are

1. In addition to reset, idle, run/debug, wait/sleep states introduced additional stop state for power conservation which is not present in product of Microchip and digital core design [2][3].
2. Double buffered register included in the design to control overflow of data which was not available in the products of Microchip, Digital core design, Texas instruments and Cadence [2] [3] [4] [5].
3. The SPI clock frequency can be divided of clk/2 to clk/2048. Such wide range of baud rates is not present in the design of Motorola, microchip, digital core design and Texas instruments [3] [4] [6] [7].

Efforts are put to reduce the power consumption of the SPI interface.

II. SPECIFICATIONS

The specifications of the SPI interface designed are as follows:-

- Master mode and slave mode of operation
- Programmable Unidirectional and Bidirectional mode for exchange of data
- Slave select output
- Has mode fault error flag and CPU interrupt capability
- Double-buffered data register
- Clock with programmable polarity and phase
- Control of SPI operation during wait mode and stop mode.
- Selectable baud rate with 12 KHz (min) to 12 MHz (max).
- Selectable data packet size (8 bit or 16 bit) for data exchange.

III. DESIGN

The block diagram of the SPI interface designed is as shown in fig 1.

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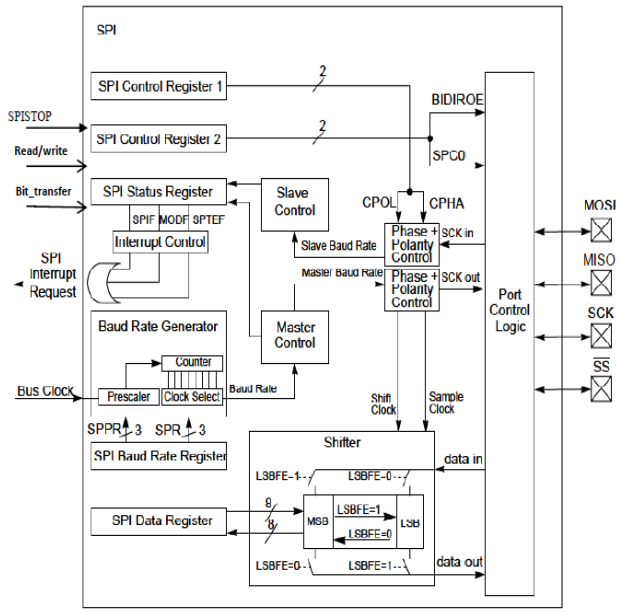

Fig 1: Block diagram of the SPI interface [8]

As shown in the above block diagram the SPI interface has 5 registers which control the functioning of the interface. Each of the registers is 8 bits wide. The input 'read/write' is used to set if the SPI interface is used to function as a full duplex or half duplex interface.There are also four modes of operation of the interface based on the clock polarity and clock phase [4] which is as shown in the table.

TABLE I. MODES OF OPERATION OF THE SPI INTERFACE [4]

Mode	Polarity	Phase	Description
0	0	0	Data is output at rising edge of clock and input is latched at falling edge of clock
1	0	1	Data is output one-half clock cycle before the rising edge of the clock and on the subsequent falling edge of the clock. Input data is latched at the rising edge of the clock.
2	1	0	Data is output at the falling edge of the clock and input is latched at the rising edge of the clock.
3	1	1	Data is output one-half clock cycle before the falling edge of the clock and the subsequent rising edge of the clock. Input data is latched at the falling edge of the clock.

There are five states of operation of the SPI interface which are reset, idle, run, wait and stop states.

The 'reset state' is the state in which all the registers of the SPI are in reset to '0'. The' idle state' is the state where only the status register is reset to '0'. The 'run state' is the state where the data exchange takes place. The 'wait state' is the state in which the SPI clock is disabled for a short period of time. The 'stop state' is the state where the whole device is turned off.

The state of the SPI changes from the reset state to the idle state if the SPE bit is set. In the run state, first the baud rate is set, next the SPI is set in either the master/slave mode, later the data exchange type is chosen as either uni-directional or bi-directional,

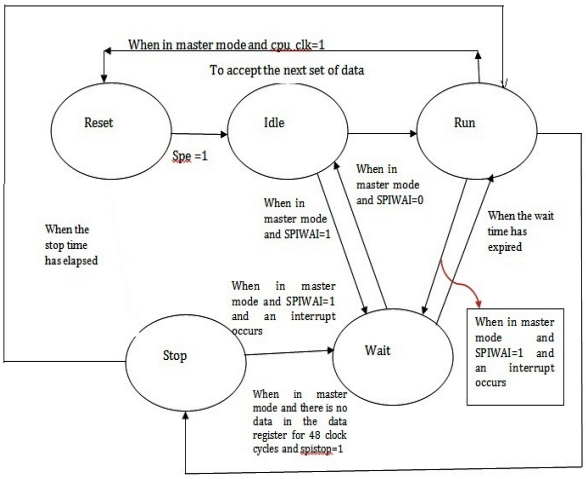

Fig 2: States of operation of the SPI interface

then it is chosen if the data to be exchanged is either 8 bit mode or 16 bit mode by setting the input 'bit_transfer' and finally the data is transferred according to the mode set by the clock polarity and clock phase. The 'wait state' is set when the bit 'SPISWAI' is set in the control register 2 of the SPI during which the clock of the SPI is disabled, when the clock of the SPI is resumed the exchange of data is resumed from where it had previously stopped. The 'stop state' is set when the input SPISTOP is set. The details of the stop state are explained in the next section.

IV. POWER OPTIMIZATION

The power reduction is achieved as follows:

a) By introducing an additional state for SPI, the stop state. In this state the clock is disabled for all modules. This reduces the power consumed by the device.

The SPI interface enters the stop state when 'SPISTOP' is active there is no data being exchanged between the master and slave of the SPI interface for 48 clock cycles. During the stop state, the clock of the interface is stopped for a short interval of time. When the clock is resumed the SPI starts to function from the run state instead reset state.

b) By reducing the power consumed by the modules of the interface.

Among the modules present in the interface which are the baud rate generator, master clock control, shift register, port

control logic and the slave clock control, the shift register is chosen for optimization in terms of area as it can be easily synchronized with the rest of the modules without many changes in the overall design of the SPI,

The various methods that can be used to reduce the power consumed by the shift register are:

a) By designing separate modules in the shift register to shift data in each direction.

b) By using double edge triggered flip flops

c) By using clock gating technique.

The advantage of using the double edge triggered flip flops is that there can be an area reduction of up to 50%. The drawback with this technique is that the coding and simulation of such a flip flop is quite complex. [9]

The technique of using clock gating can reduce the power consumption of the SPI interface by 30% [10].

The technique to design separate modules in the shift register to shift data in each direction can reduce the area by an average of 20.79% which reduces the power consumed by an average of 23.12% [11].

On optimizing the design of the shift register using clock gating a change is noticed in the power of the shift register of the design which is shown in the next section.

V. SIMULATION RESULTS

The figures below show the simulated results of the designed SPI interface:-

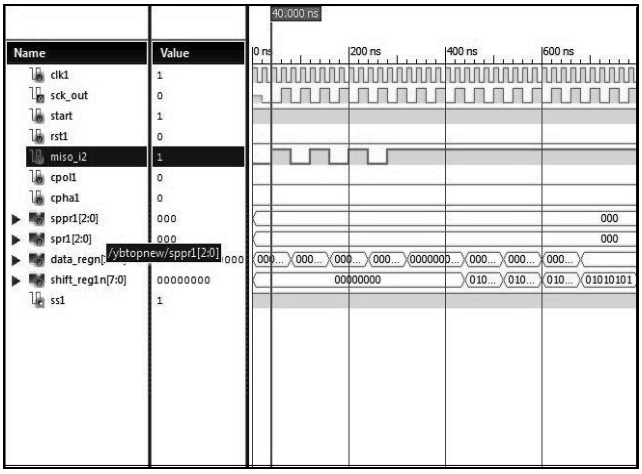

Fig 3: Simulated result for input in mode 0

The above simulated result is of obtaining an input to the master from the slave.

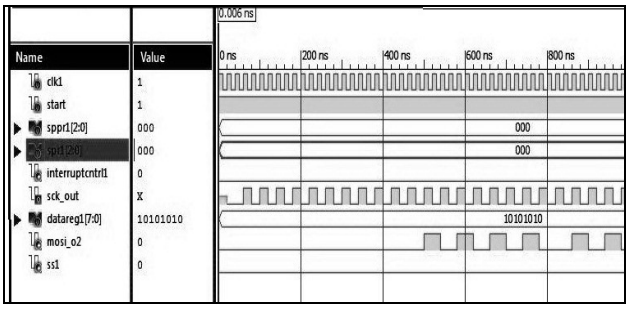

Fig 4: Simulated result for output in mode 0

The above simulated output shows the data being sent from the master to the slave in mode 0.

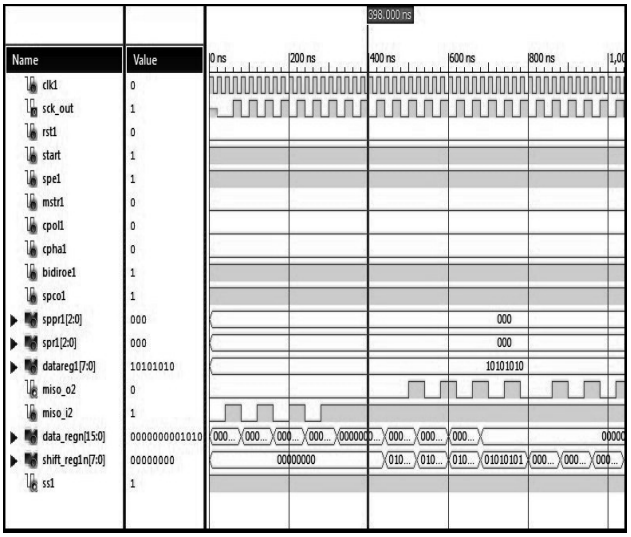

Fig 5: Simulated result when slave is in mode 0 and data is transferred bidirectional

This simulated result shows the transfer of data from the master to the slave and from slave to the master taking place at on the same wire.

On performing clock gating for the shift register module of the SPI interface the power optimization results are as shown in the table below.

TABLE II. POWER OPTIMIZATION RESULTS

Shift register design	Without clock gating	With clock gating
Leakage power (nW)	202809.832	193988.985
Dynamic power (nW)	691610.935	603325.273
Total power (nW)	894420.767	797314.258

The difference in the total power in the design of the shift register on performing clock gating is 10.85%.The difference

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in the dynamic power in the design of the shift register is 12.7% and the difference in the leakage power is 4.34%.

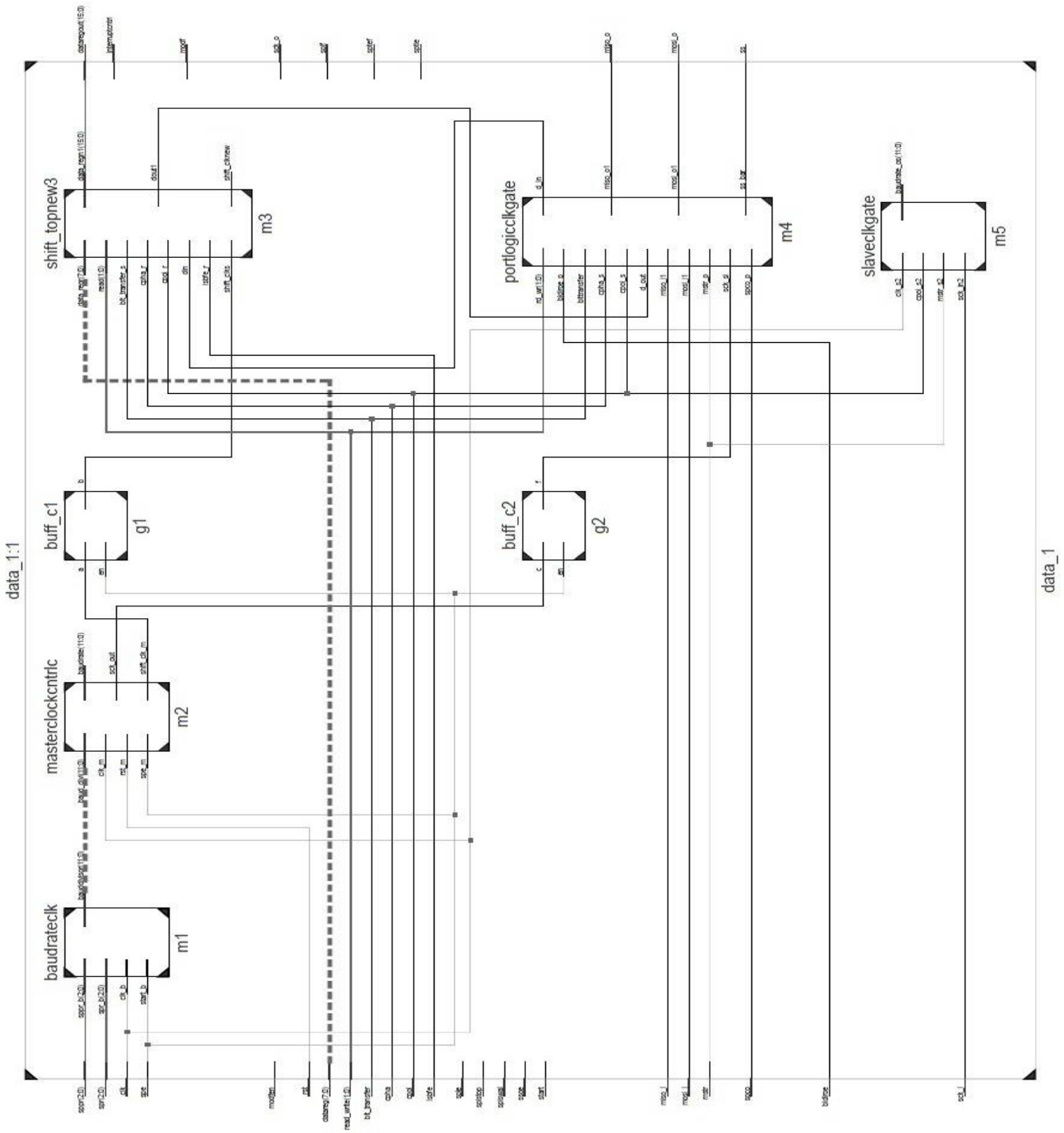

Fig 6: RTL schematic of the SPI interface

VI. CONCUSION

The design of the SPI interface has been completed successfully and verified the performance with simulated data using a test bench. Power down mode (stop mode) has been implemented and verified. The power reduction due to clock gating of the shift register module has been observed to be 10.85% in the total power, 12.7% in dynamic power and 4.34% in leakage power.

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