



Course Name: Digital System Design

Course Number and Section: 14:332:437:02

Experiment: Lab 6

Lab Instructor: Zhenghao Li

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Prelab

Register file SysV Code

```
module register_file (
    input logic clk, rst,
    input logic [4:0] A1, A2, A3, //A1=rs, A2=rt ,A3=rd
    input logic [31:0] WD3,      //data from data memory
    input logic WE3,            //write enable
    output logic [31:0] RD1,    //output port one for register file
    output logic [31:0] RD2,    //output port two for register file
    output logic [31:0] prode    //prode to check the result in the register file
);

    logic [31:0] regs [31:0];

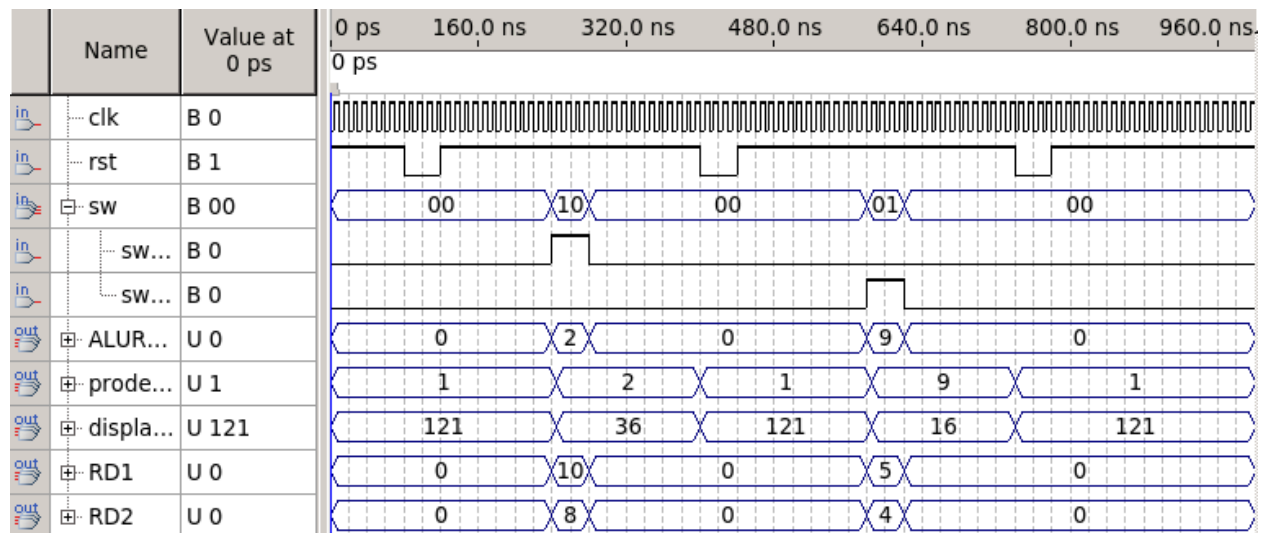
    assign RD1 = regs[A1];
    assign RD2 = regs[A2];
    assign prode = regs[1];

    always_ff @(posedge clk or negedge rst)
    begin
        if (!rst) begin
            for (int i = 0; i < 32; i++) begin
                regs[i] <= i;
            end
        end
        else begin
            if (WE3) begin
                regs[A3] <= WD3;
            end
        end
    end
endmodule
```

ALU file SysV Code

```
1 module ALU(
2     input logic[31:0] SrcA, SrcB,
3     input logic[2:0] ALUControl,
4     output logic[31:0] ALUResult);
5
6     always_comb begin
7         case (ALUControl)
8             3'b010: ALUResult = SrcA + SrcB;
9             3'b110: ALUResult = SrcA - SrcB;
10            default: ALUResult = 32'b0;
11        endcase
12    end
13 endmodule
```

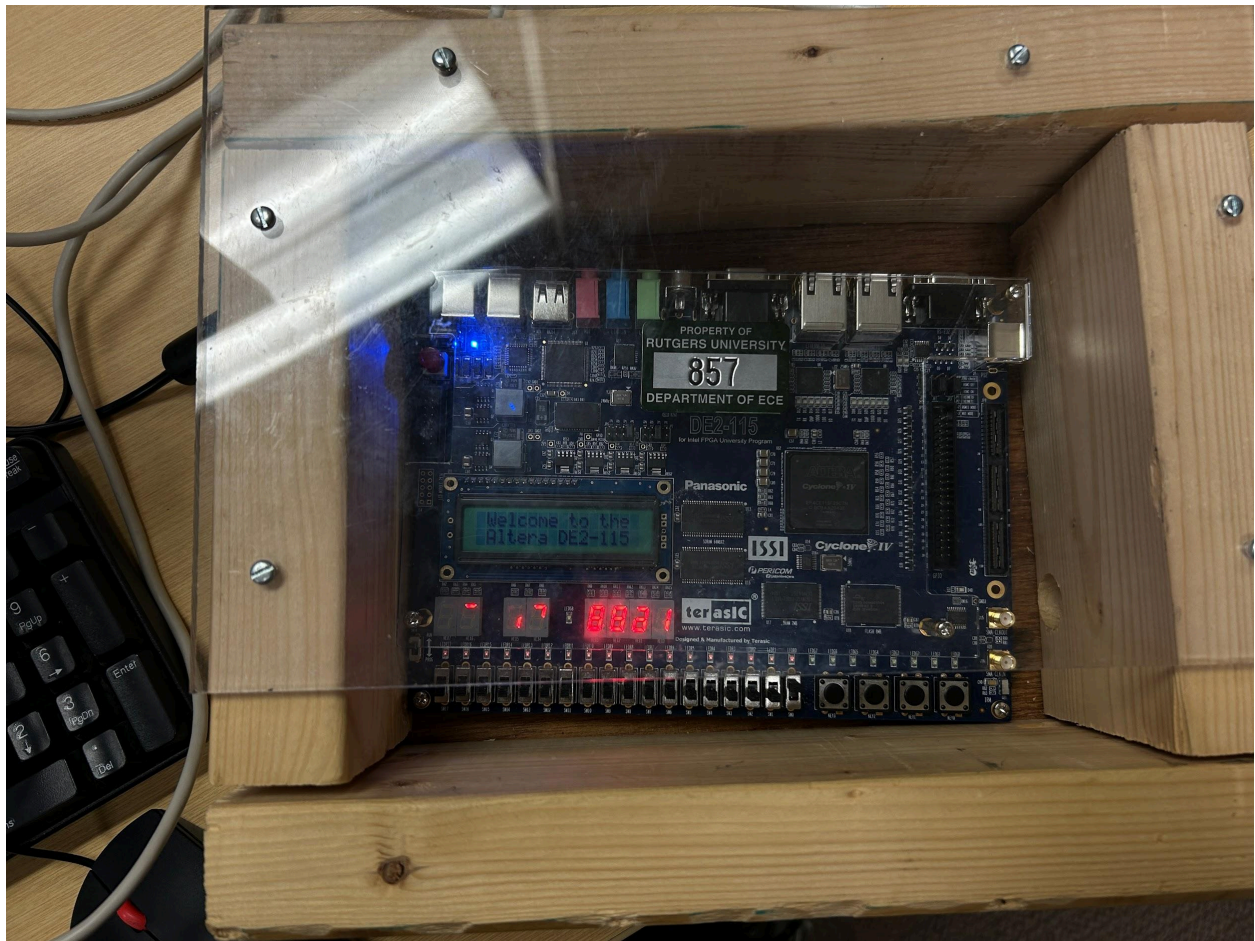
Waveform



Pin assignment

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		disp...d[0]	Location	PIN_G18	Yes			
2	✓		disp...d[1]	Location	PIN_F22	Yes			
3	✓		disp...d[2]	Location	PIN_E17	Yes			
4	✓		disp...d[3]	Location	PIN_L26	Yes			
5	✓		disp...d[4]	Location	PIN_L25	Yes			
6	✓		disp...d[5]	Location	PIN_J22	Yes			
7	✓		disp...d[6]	Location	PIN_H22	Yes			
8	✓		clk	Location	PIN_Y2	Yes			
9	✓		rst	Location	PIN_AB28	Yes			
10	✓		sw[0]	Location	PIN_AC28	Yes			
11	✓		sw[1]	Location	PIN_AC27	Yes			
12		<<new>>	<<new>>	<<new>>					

Reset



Sub



Add



I worked on this lab for 6 hours.