



**RUTGERS**  
UNIVERSITY

**Course Name:** Digital System Design

**Course Number and Section:** 14:332:437:02

**Experiment:** Lab 3 Prelab

**Lab Instructor:** Zhenghao Li

**Date Performed:** 9/26/24

**Date Submitted:** 9/26/24

**Submitted by:** Nikhil Chandra Donepudi Venkata Sambasiva

Hexadecimal Digit	Inputs				Outputs								(in hex)
	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	S <sub>g</sub>	S <sub>f</sub>	S <sub>e</sub>	S <sub>d</sub>	S <sub>c</sub>	S <sub>b</sub>	S <sub>a</sub>		
0	0	0	0	0	1	0	0	0	0	0	0	0	40
1	0	0	0	1	1	1	1	1	0	0	1	0	79
2	0	0	1	0	0	1	0	0	1	0	0	0	24
3	0	0	1	1	0	1	1	0	0	0	0	0	30
4	0	1	0	0	0	0	1	1	0	0	1	0	19
5	0	1	0	1	0	0	1	0	0	1	0	0	12
6	0	1	1	0	0	0	0	0	0	1	0	0	02
7	0	1	1	1	1	1	1	0	0	0	0	0	78
8	1	0	0	0	0	0	0	0	0	0	0	0	00
9	1	0	0	1	0	0	1	1	0	0	0	0	18
A	1	0	1	0	0	0	0	1	0	0	0	0	08
B	1	0	1	1	0	0	0	0	0	1	1	0	03
C	1	1	0	0	0	1	0	0	1	1	1	0	27
D	1	1	0	1	0	1	0	0	0	0	1	0	21
E	1	1	1	0	0	0	0	0	1	1	0	0	06
F	1	1	1	1	0	0	0	1	1	1	0	0	0E

Table 1. Truth table for 7-segment display decoder

S <sub>a</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	10	11
00	0	0	1	0	0
01	1	1	0	0	0
10	1	0	1	0	0
11	0	0	0	1	0

$$S_a = D_3 D_2 \bar{D}_1 + \bar{D}_3 \bar{D}_2 \bar{D}_1 D_0 + D_2 \bar{D}_1 \bar{D}_0 + D_3 \bar{D}_2 D_1$$

S <sub>b</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	10	11
00	0	0	0	0	0
01	0	1	0	0	1
10	1	0	0	1	0
11	0	0	1	1	0

$$S_b = \bar{D}_3 D_2 \bar{D}_1 D_0 + D_2 \bar{D}_1 \bar{D}_0 + D_3 D_2 D_1 + D_3 D_2 \bar{D}_0$$

S <sub>c</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	10	11
00	0	0	0	0	0
01	0	0	0	0	0
10	1	0	1	1	0
11	0	0	0	0	0

$$S_c = \bar{D}_3 \bar{D}_2 D_1 D_0 + D_3 D_2 D_1 + D_3 D_2 \bar{D}_0$$

S <sub>d</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	10	11
00	0	0	1	0	0
01	1	0	0	1	0
10	0	0	0	1	0
11	0	1	0	0	1

$$S_d = D_3 \bar{D}_2 D_1 D_0 + D_2 \bar{D}_1 D_0 + \bar{D}_3 D_2 \bar{D}_1 + \bar{D}_2 D_1 D_0$$

S <sub>e</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	10	11
00	0	0	1	1	0
01	1	1	0	0	0
10	0	0	0	0	0
11	0	1	0	0	0

$$S_e = \bar{D}_3 \bar{D}_2 D_1 + \bar{D}_3 D_2 + \bar{D}_2 \bar{D}_1 D_0$$

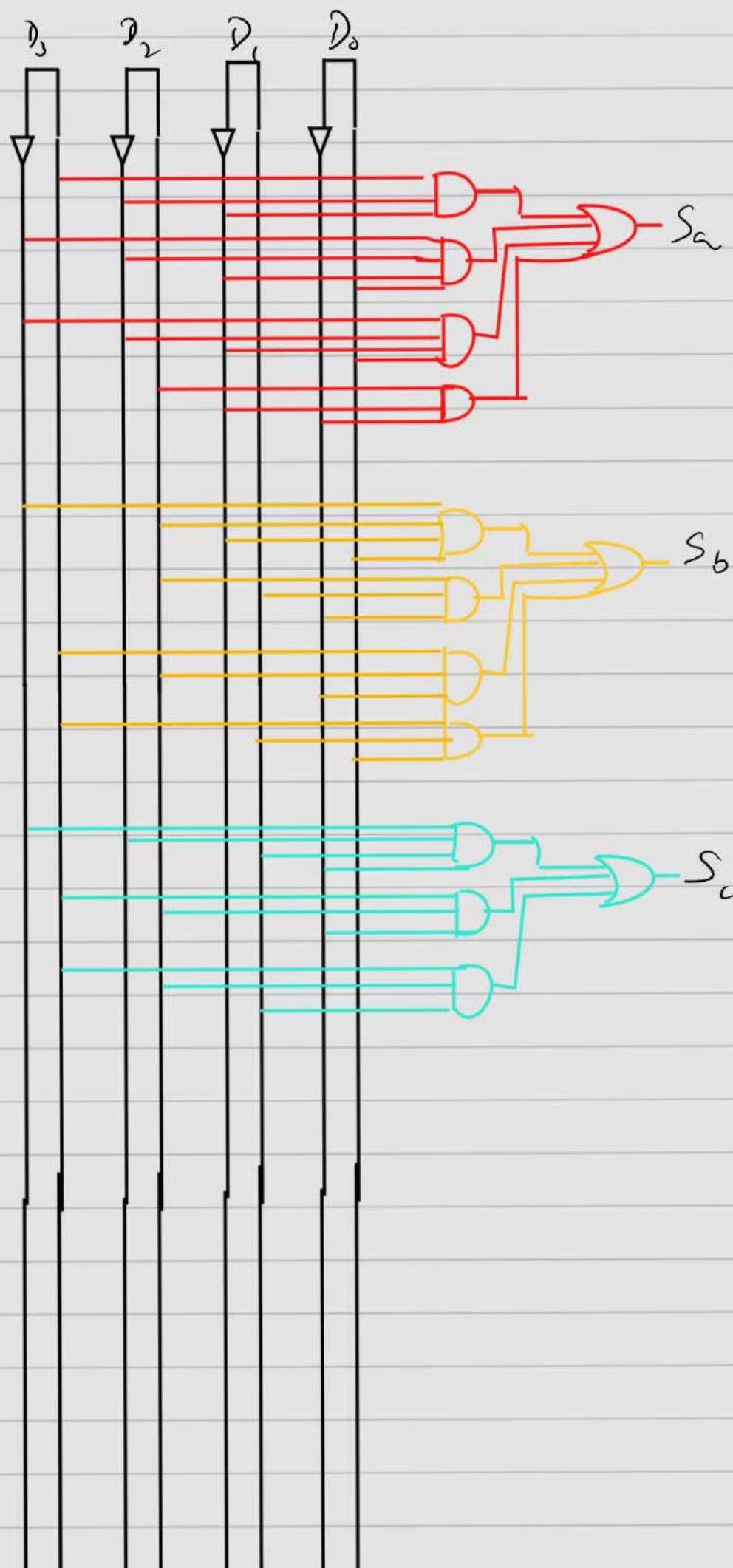
S <sub>f</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	11	10
00	0	0	1	0	0
01	0	0	0	1	0
11	1	1	0	0	0
10	0	1	0	0	0

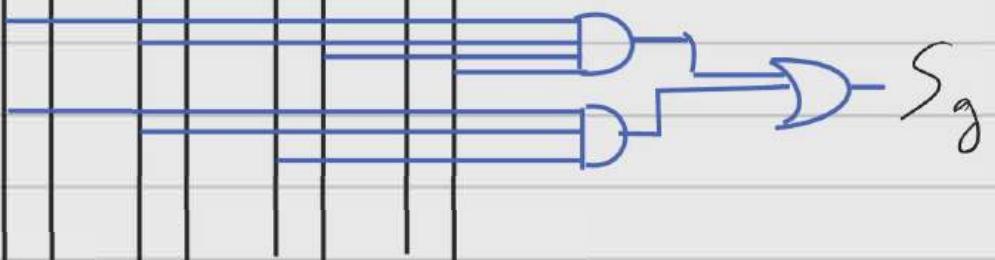
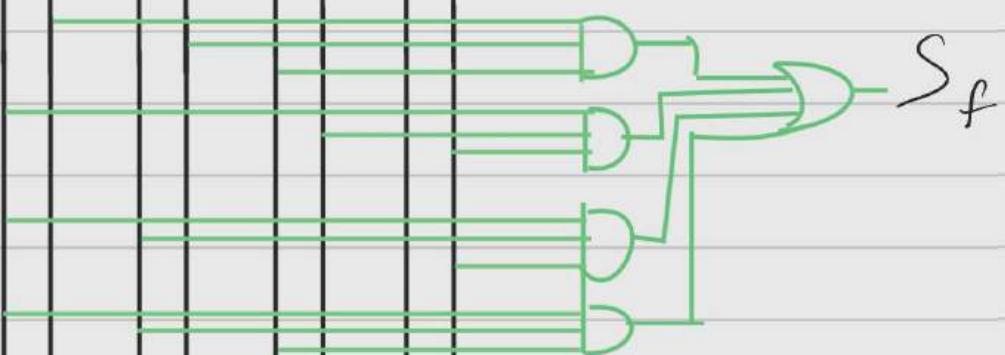
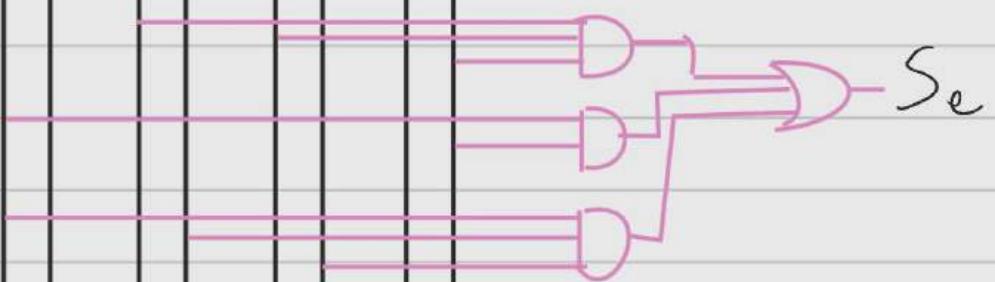
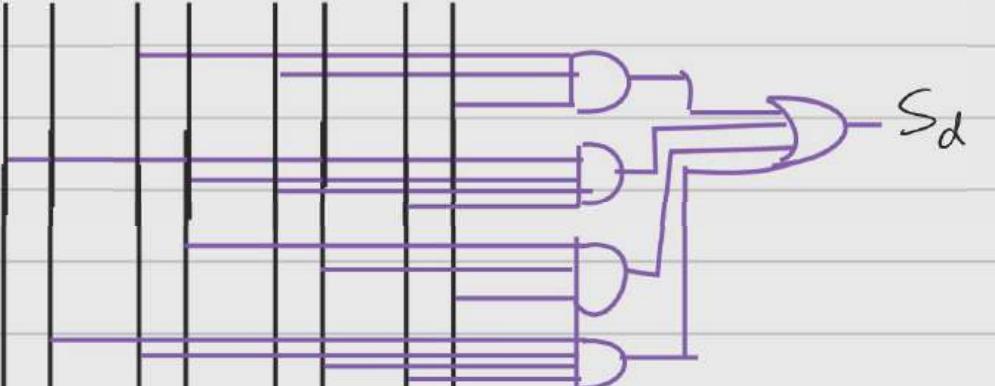
$$S_f = D_3 D_2 \bar{D}_1 + \bar{D}_3 \bar{D}_2 D_1 + \bar{D}_3 D_2 D_1 + \bar{D}_2 D_1 D_0$$

S <sub>g</sub>	D <sub>3</sub> , P <sub>2</sub>	00	01	11	10
00	0	1	1	0	0
01	0	0	0	0	0
11	0	0	0	0	0
10	0	0	0	0	0

$$S_g = \bar{D}_3 \bar{D}_2 \bar{D}_1 + \bar{D}_3 D_2 D_1$$

Sketch:



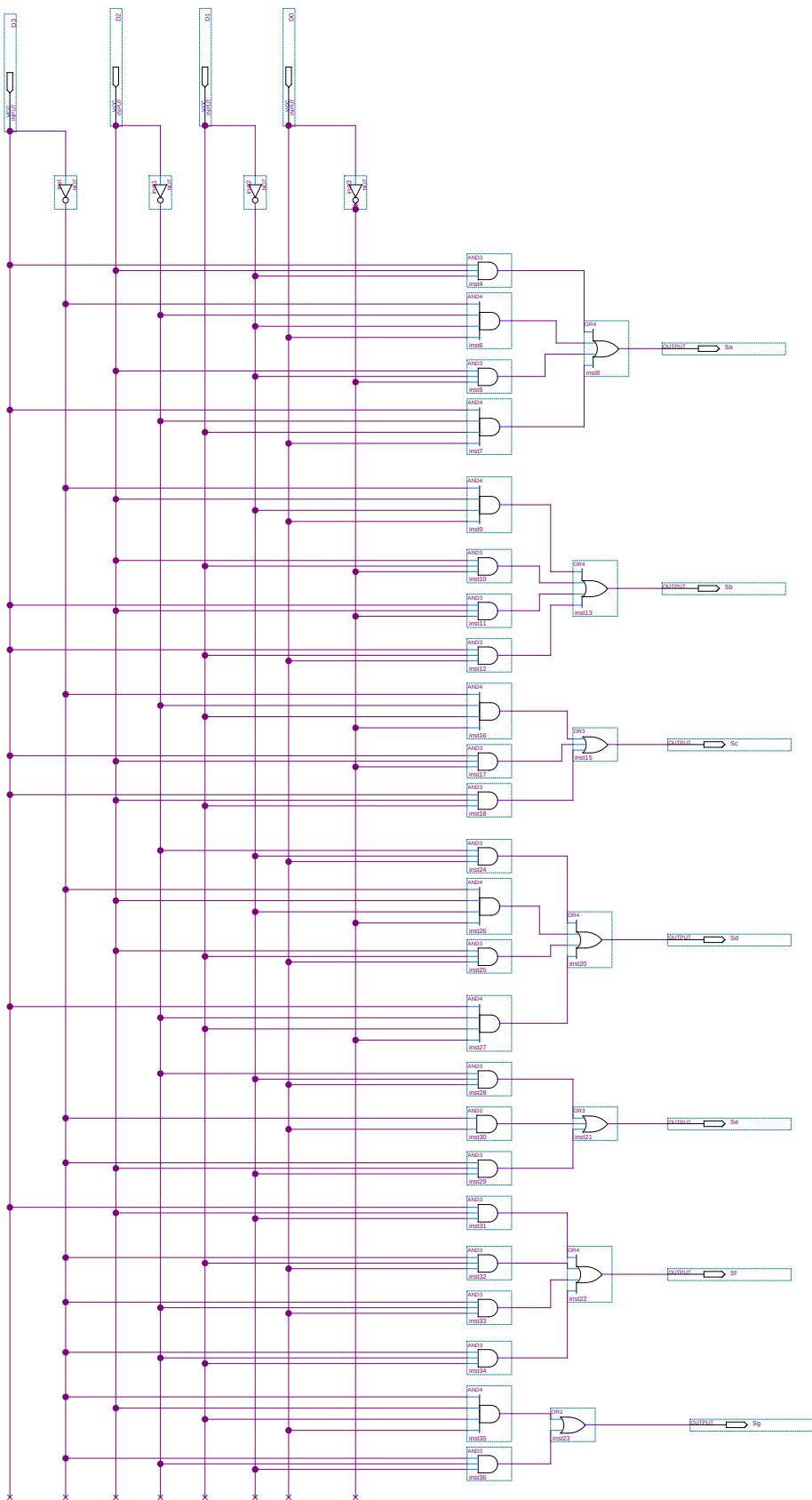


Schematic from Quartus

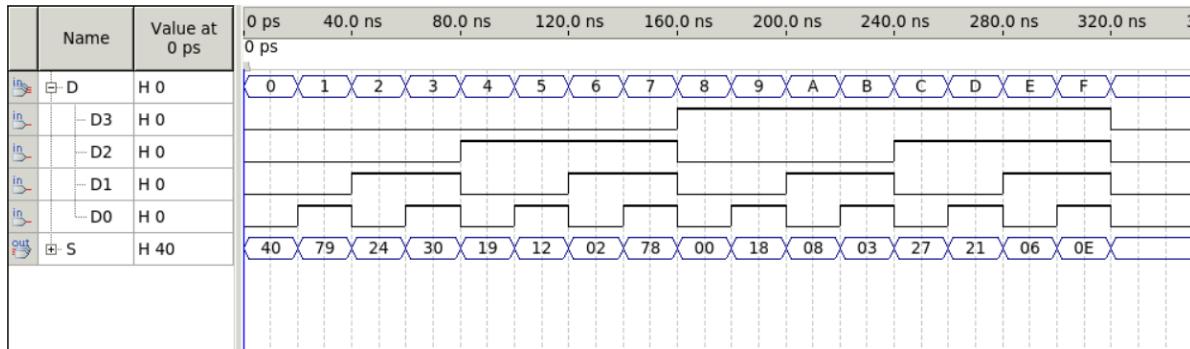
Date: September 25, 2024

Lab3.bdf

Project: Lab3



## Simulation waveform



This design needed several steps that were fundamental to each other.

First, I filled out the truth table for the decoder and wrote the boolean equations for each output node.

Then, I used the two above to create the logical circuit in Quartus, after which I used the rough sketch from above to make the schematic that was the basis of the decoder in Quartus.

I compiled the schematic and simulated it to generate the waveforms seen above.

This prelab took me around 8 hours from start to end. The most tedious task was the schematic sketch on paper.

This was long and I was prone to mistakes. The other tasks were straightforward and not as time-taking.

Index	Status	From	To	Assignment Name	Value	Enabled	Entity
1	✓		in D1	Location	PIN_AC28	Yes	
2	✓		in D2	Location	PIN_AC27	Yes	
3	✓		in D3	Location	PIN_AD27	Yes	
4	✓		out Sa	Location	PIN_G18	Yes	
5	✓		out Sb	Location	PIN_F22	Yes	
6	✓		out Sc	Location	PIN_E17	Yes	
7	✓		out Sd	Location	PIN_L26	Yes	
8	✓		out Se	Location	PIN_L25	Yes	
9	✓		out Sf	Location	PIN_J22	Yes	
10	✓		out Sg	Location	PIN_H22	Yes	
11	✓		in D0	Location	PIN_AB28	Yes	
12		<<new>>	<<new>>	<<new>>			

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
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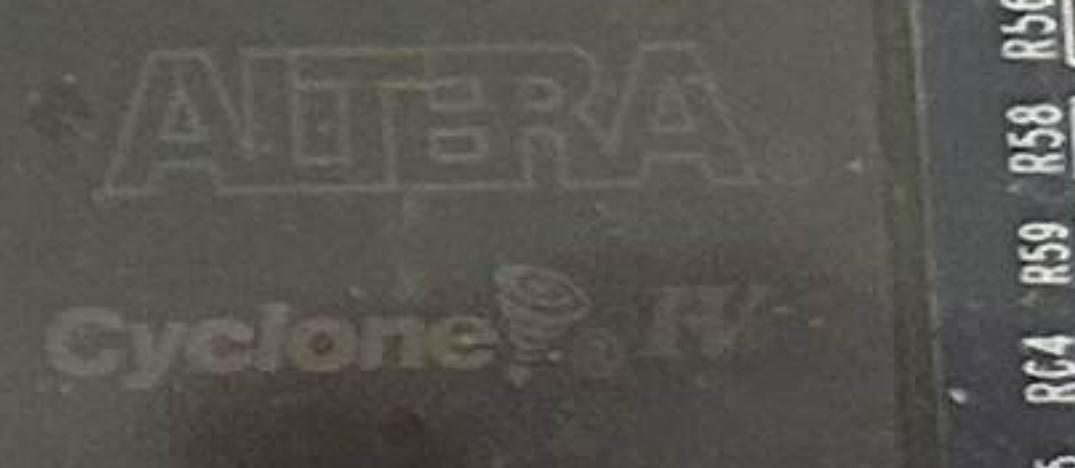


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
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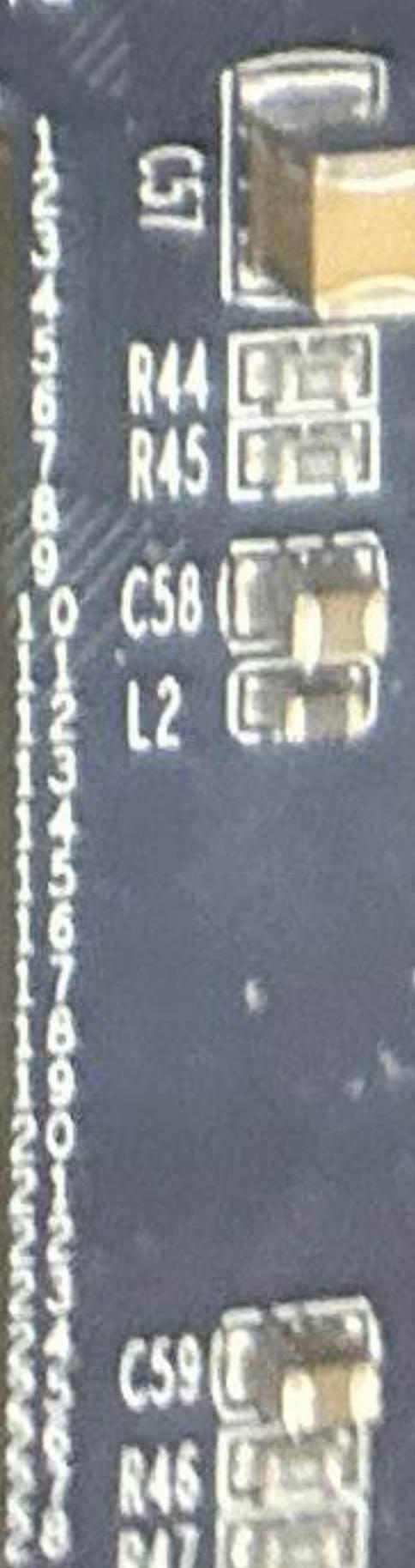
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SW17 SW16 SW15 SW14 SW13 SW12 SW11 SW10 SW9 SW8 SW7 SW6 SW5 SW4 SW3 SW2 SW1 SW0 ALT1 KEY0

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U12  
C57  
R44  
R45  
C58  
L2

R62  
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C18  
C19  
C20

ISSI  
T1S2515S00X-71L  
T1S2515S00X-202

SDRAM 64MBx2



U13

C82

U14  
C85  
ISSI  
T1S2515S00X-71L  
T1S2515S00X-202



U15

C86

U16

C87

U17

SRAM 2MB

U18

C88

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