



Course Name: EMBEDDED SYSTEMS I / III

Course Number and Section: 14:332:493:03 / 16:332:579:05

Year: Spring 2025

Lab Report #: Synthesis Lab

Lab Instructor: Milton Diaz

Student Name and RUID: Nikhil Chandra, 208005066

Date Submitted: 2/14/2025

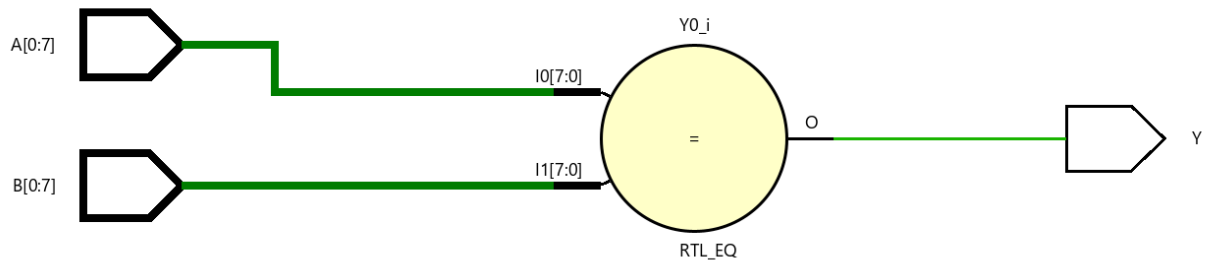
GitHub Link:

<https://github.com/embedded-systems-1-spring-2025-labs/lab-synthesis-1-nikhilChandra-coder>

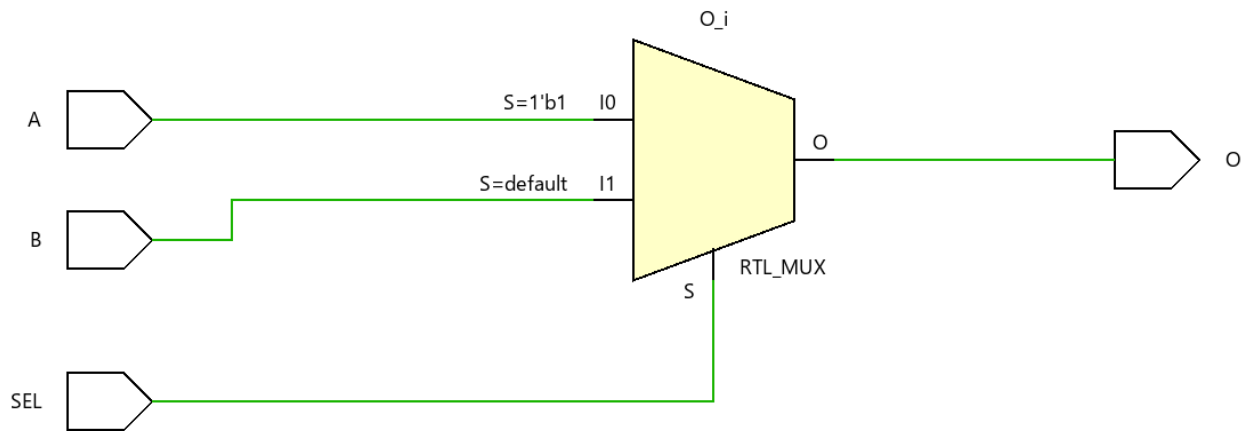
<https://github.com/embedded-systems-1-spring-2025-labs/lab-synthesis-2-nikhilChandra-coder>

Vivado Schematics:

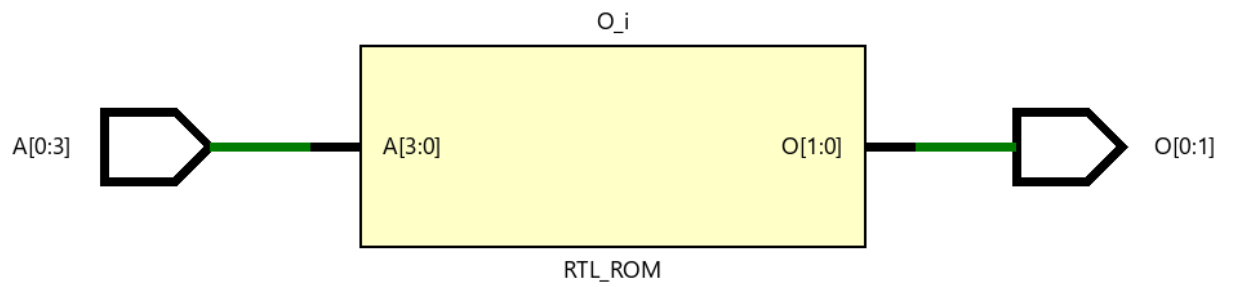
a) Vivado Elaboration Schematic



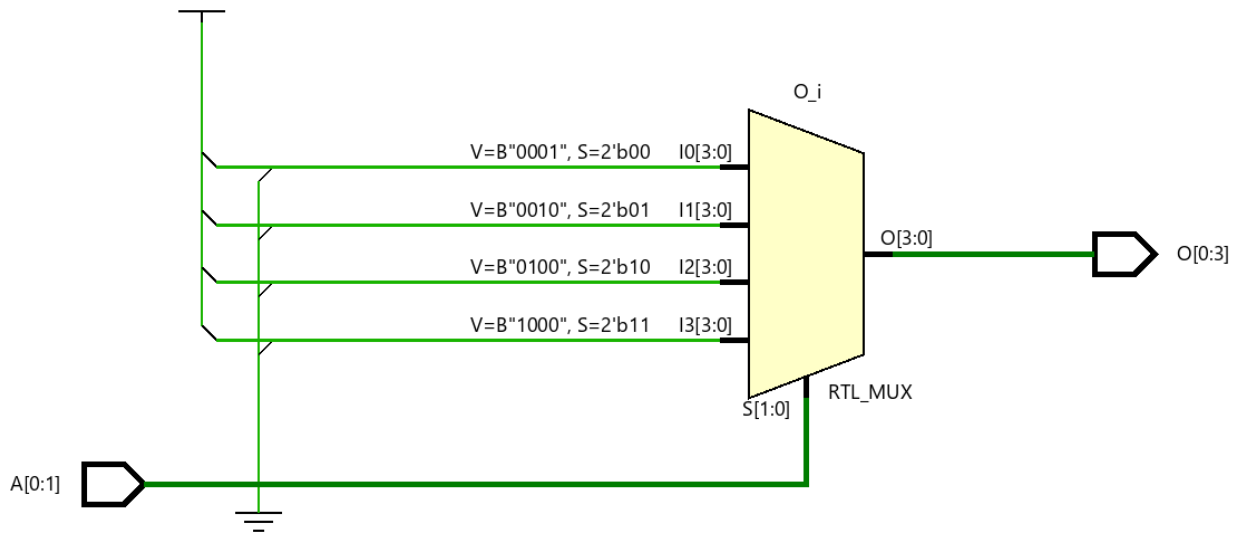
8 bit comparator



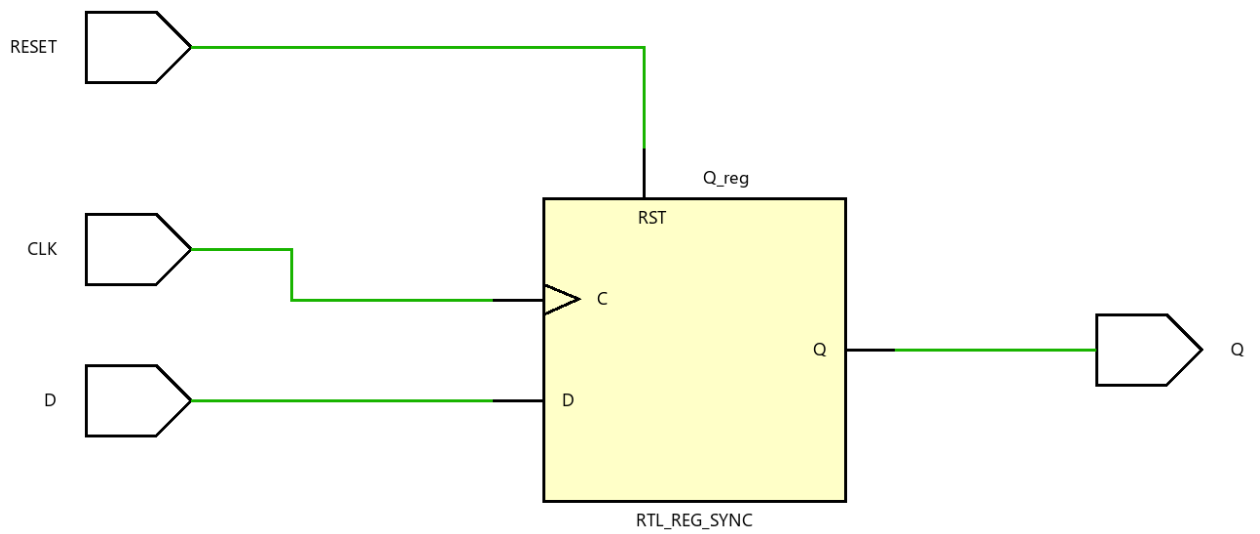
2 to 1 Mux



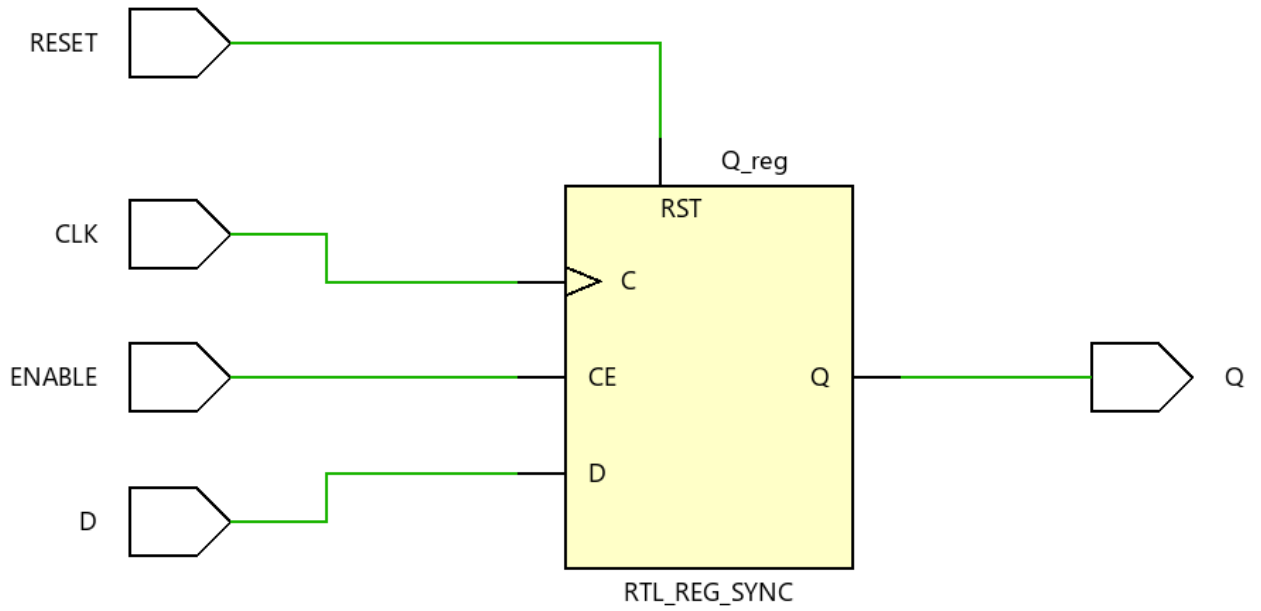
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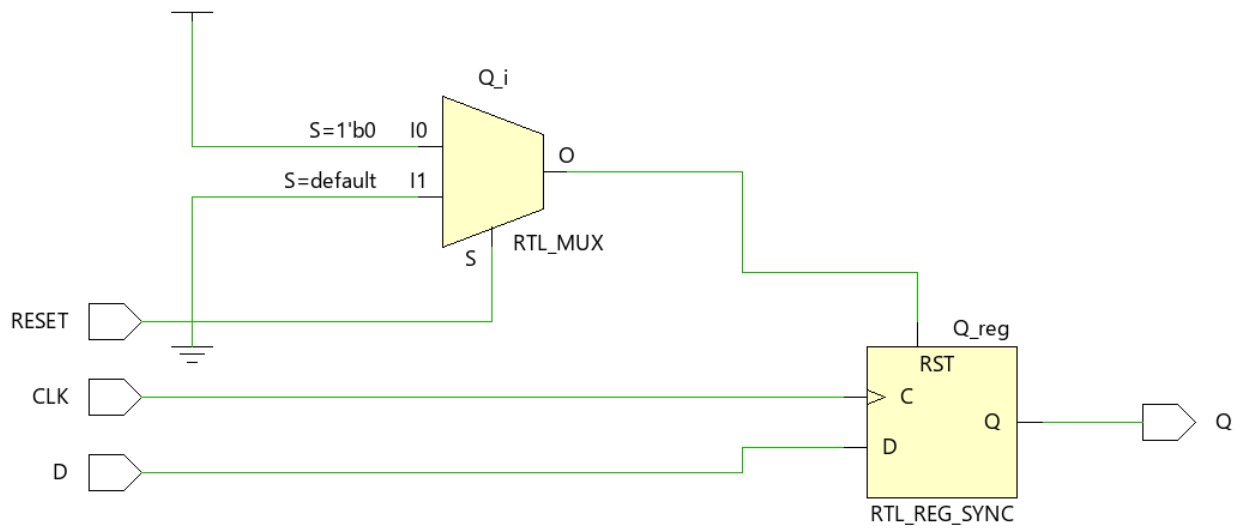
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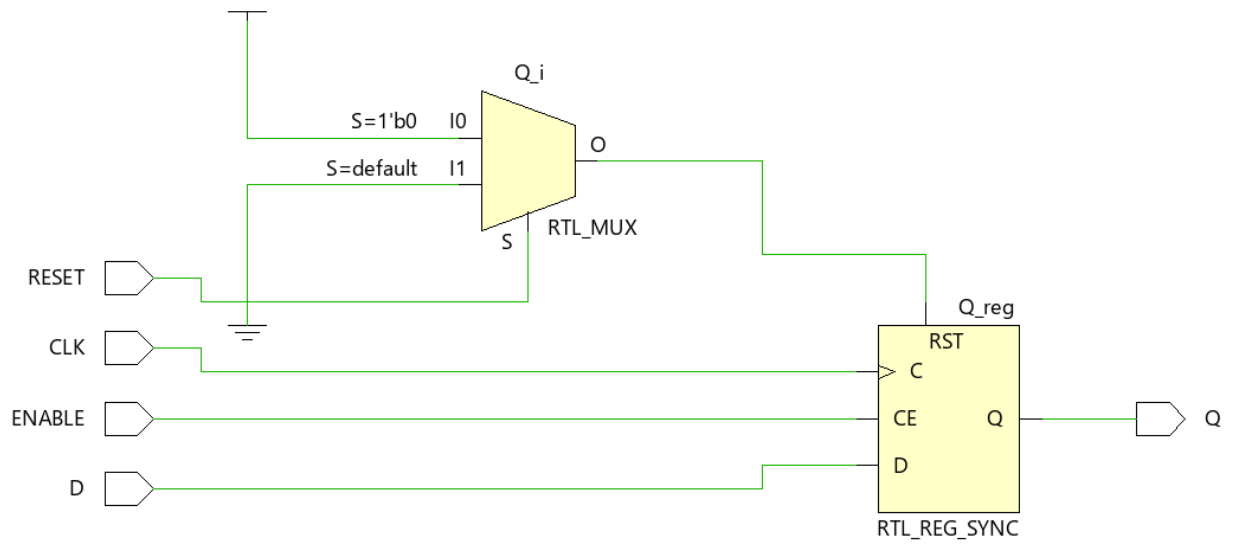
Synchronous_Active_High_Reset



Synchronous_Active_High_Reset_CE

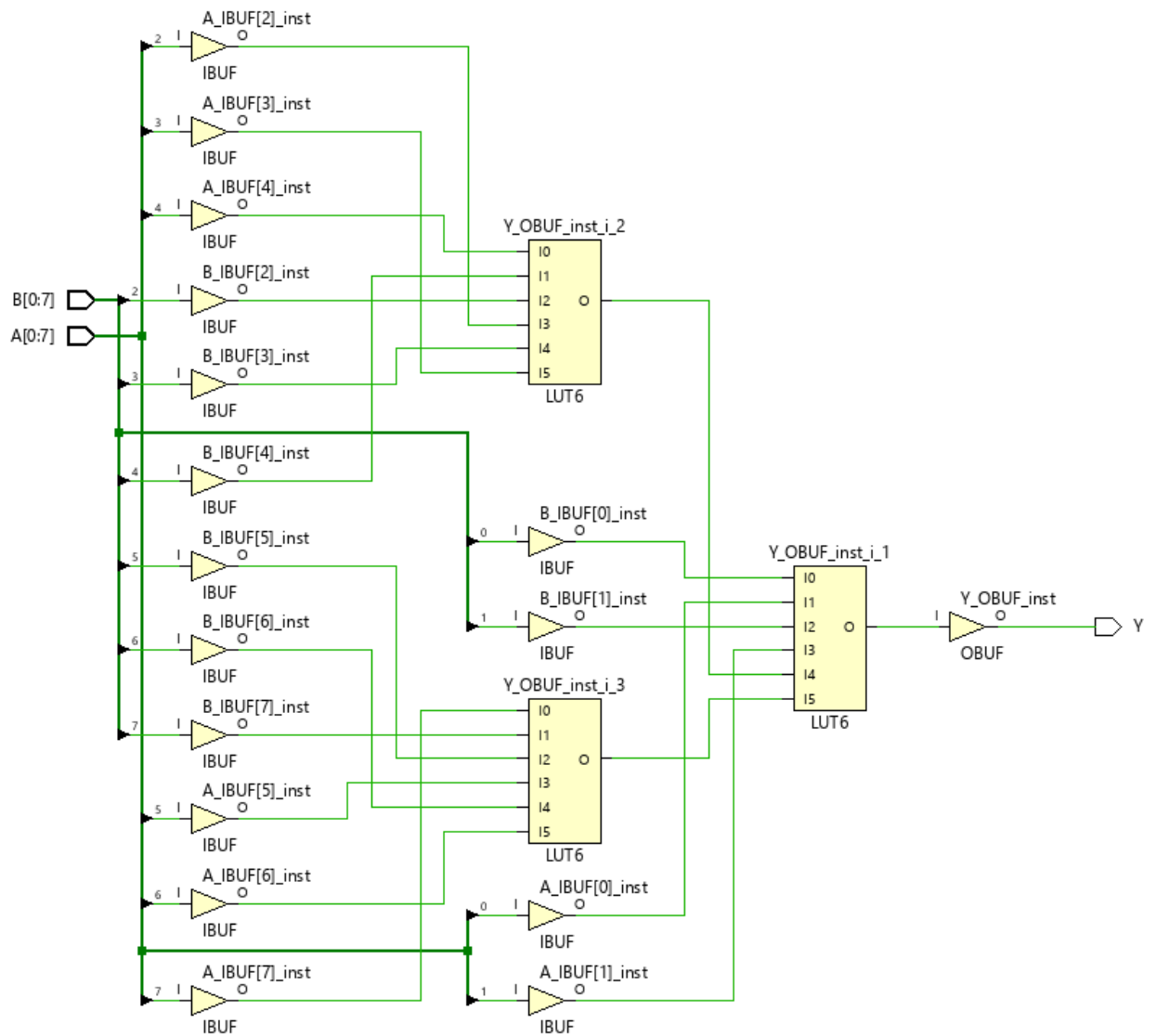


Synchronous_Active_Low_Reset

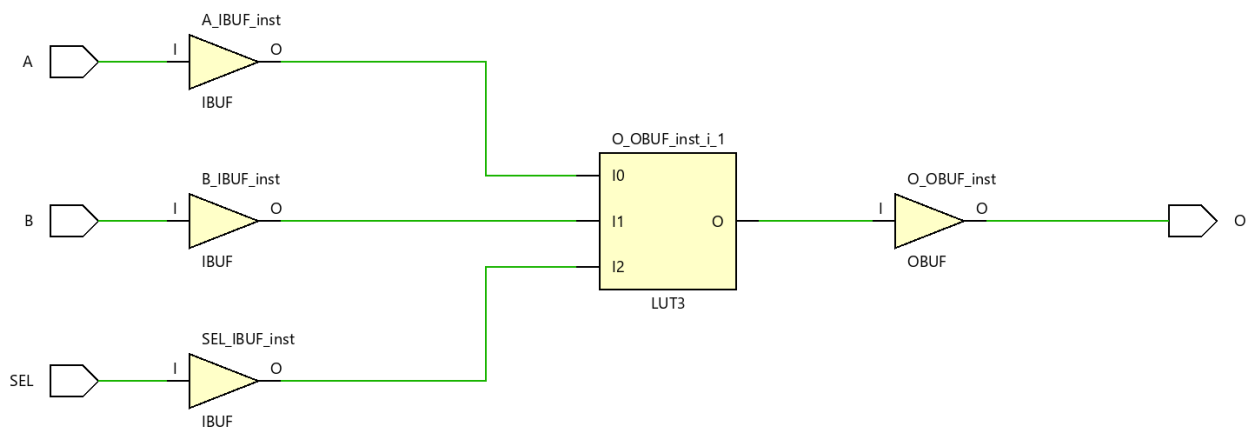


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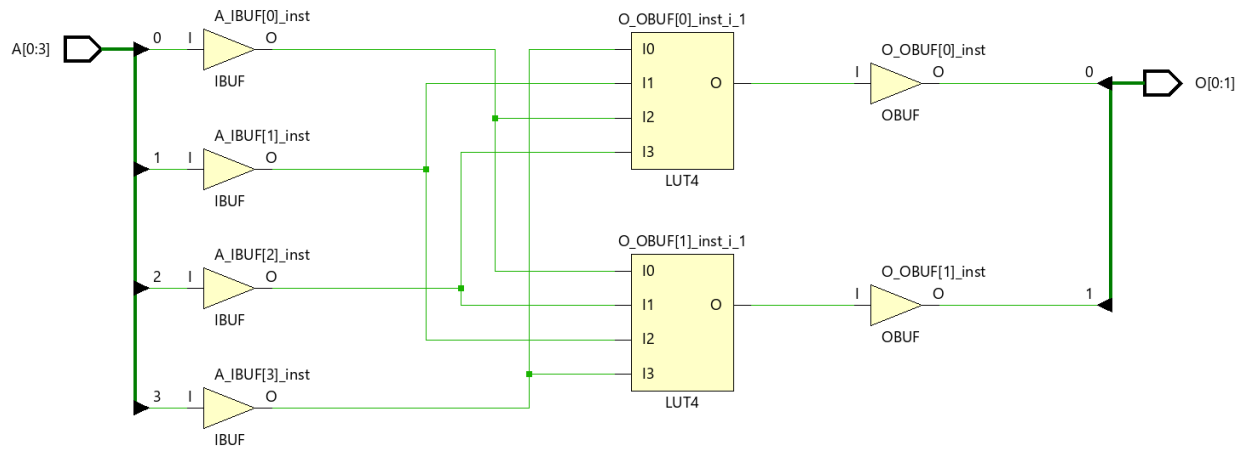
b) Vivado Synthesis Schematic



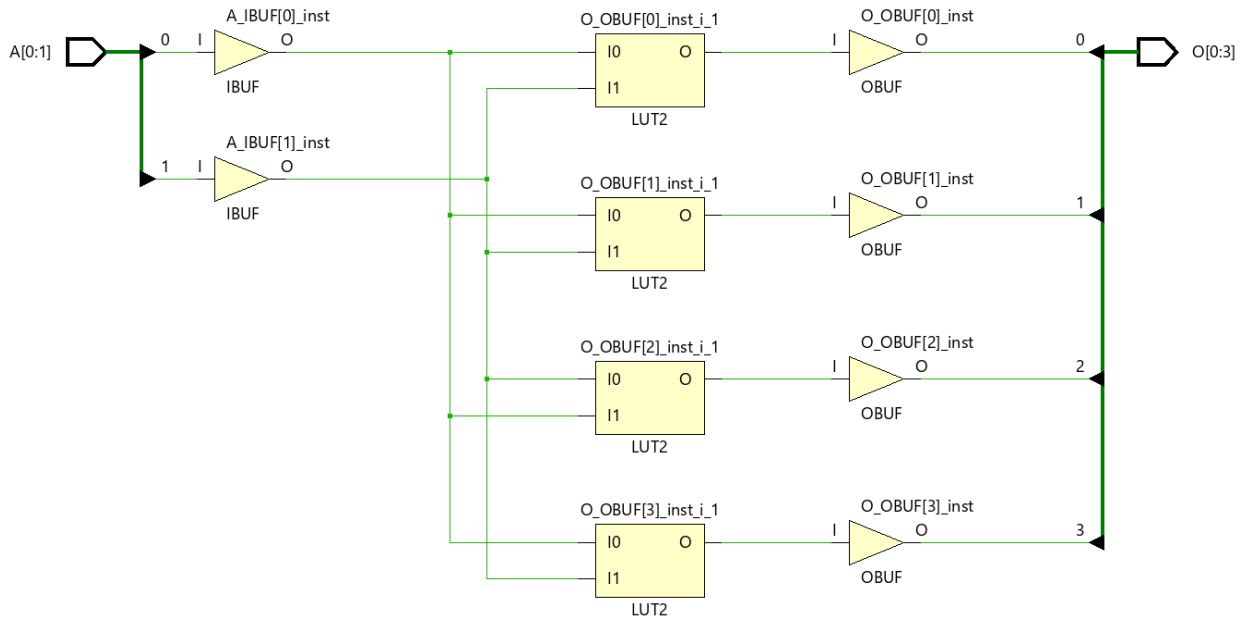
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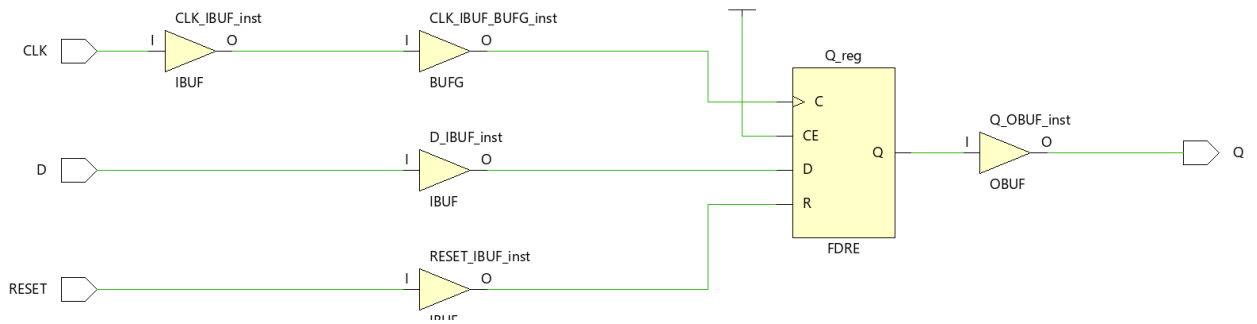
2 to 1 Mux



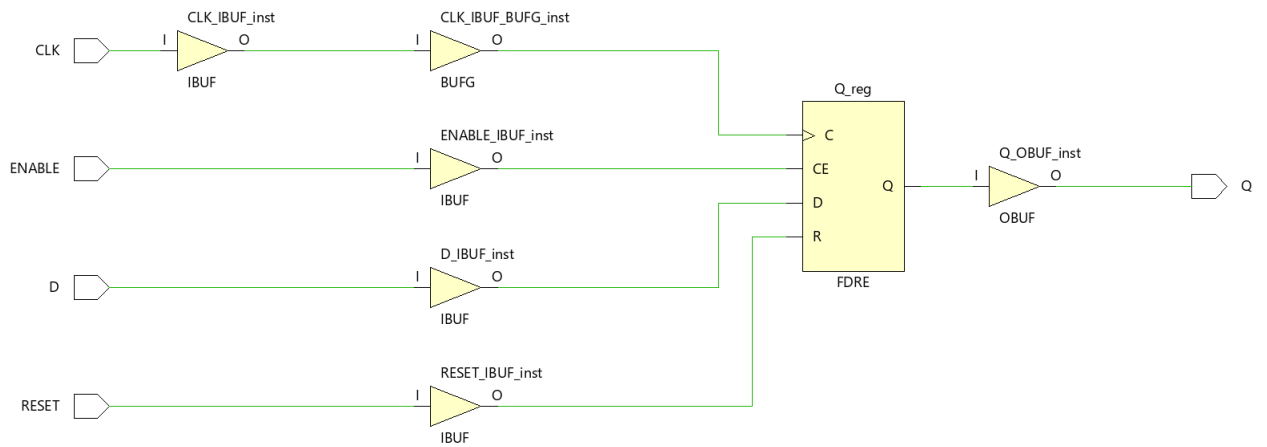
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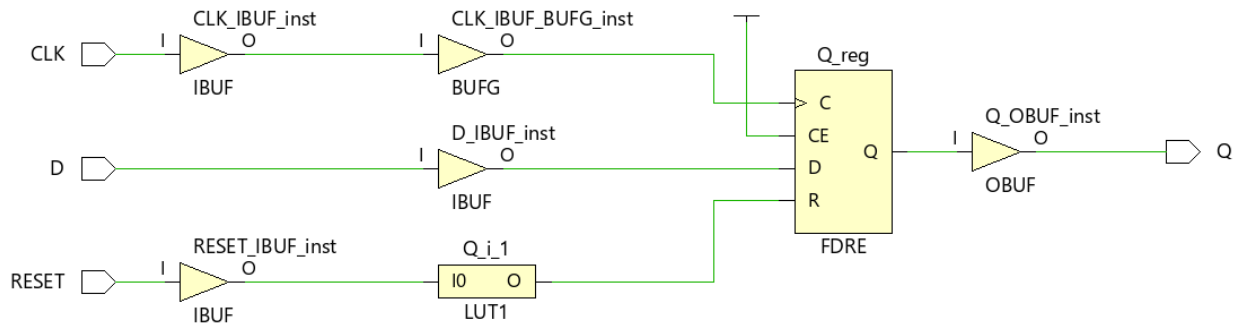
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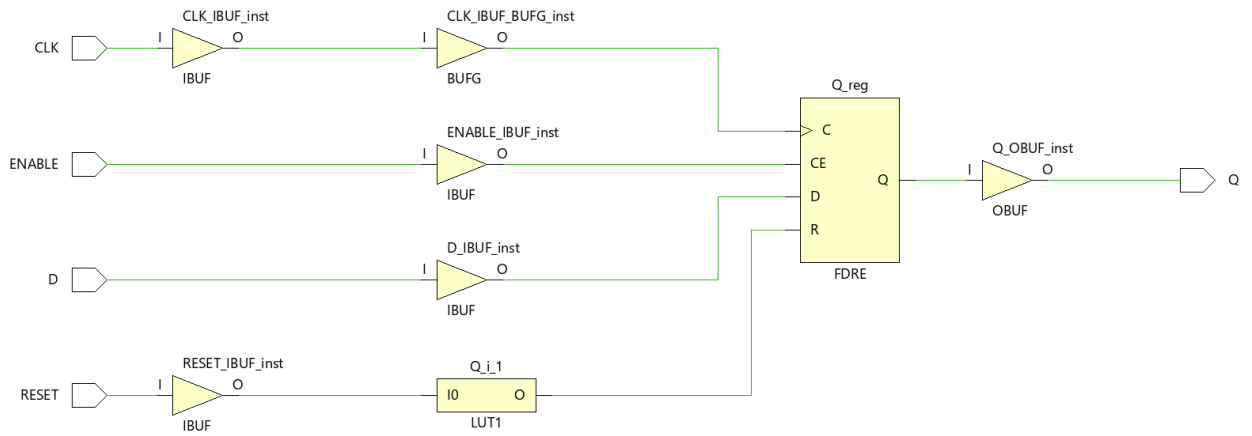
Synchronous_Active_High_Reset



Synchronous_Active_High_Reset_CE

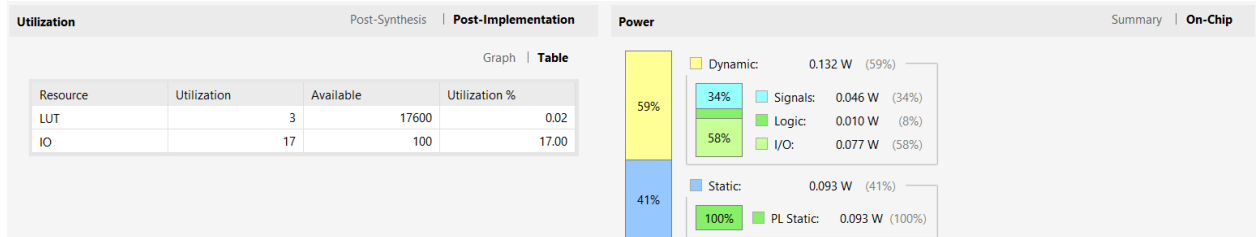


Synchronous_Active_Low_Reset

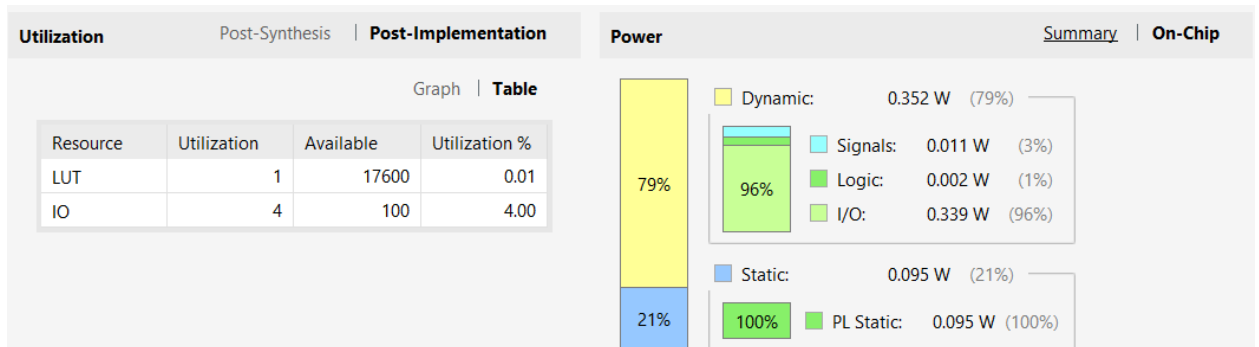


Synchronous_Active_Low_Reset_CE

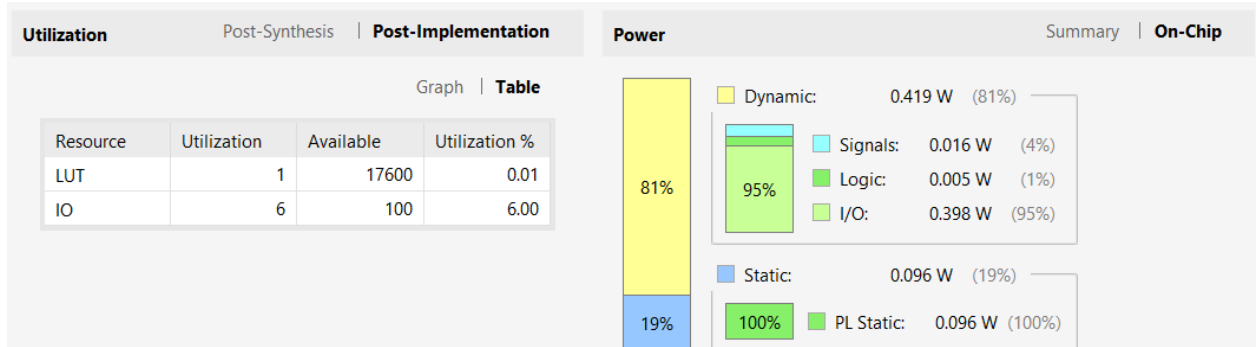
c) Post- Synthesis Utilization Table and On-Chip Power Graphs



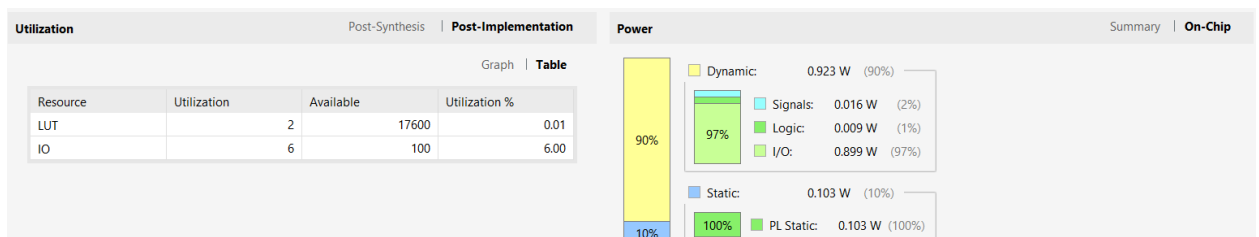
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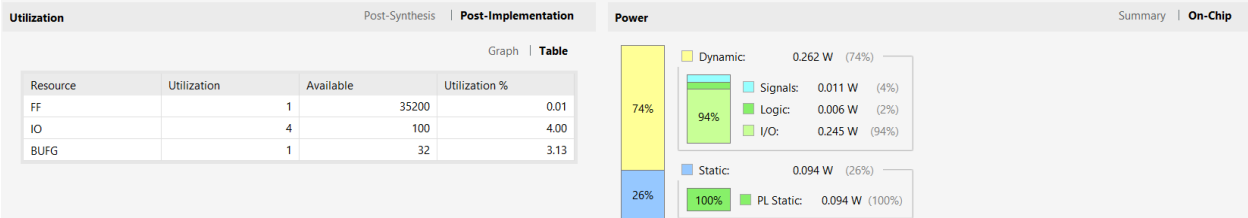
2 to 1 Mux



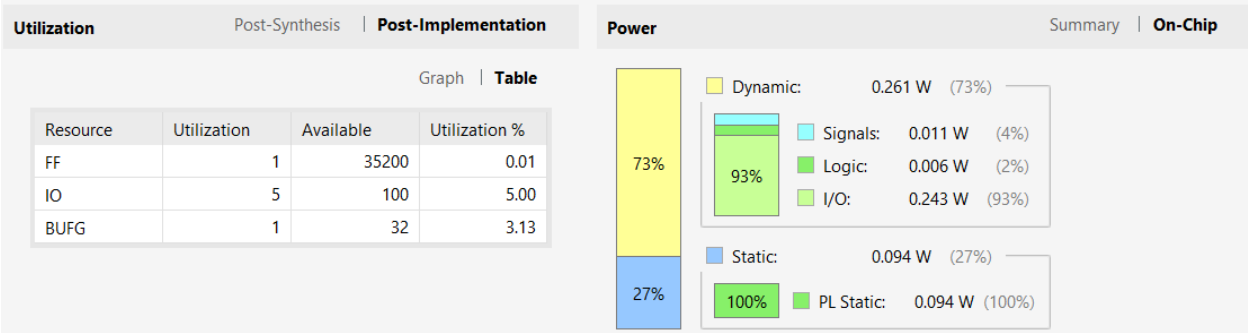
4 bit encoder



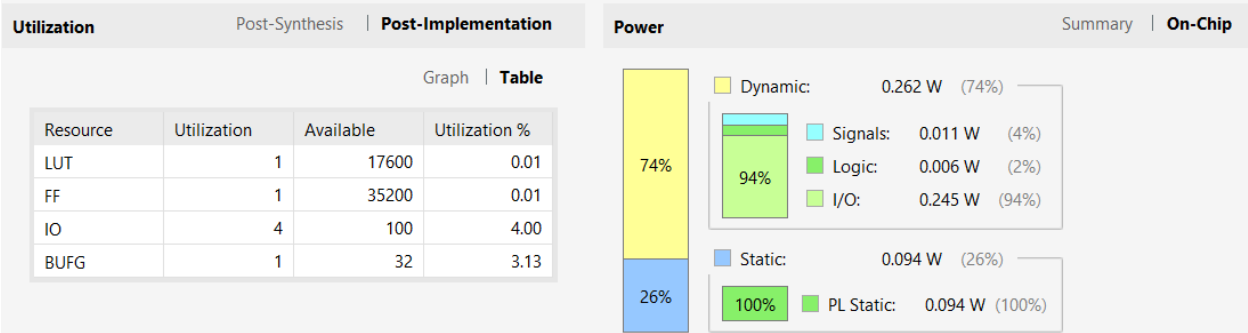
4 bit decoder



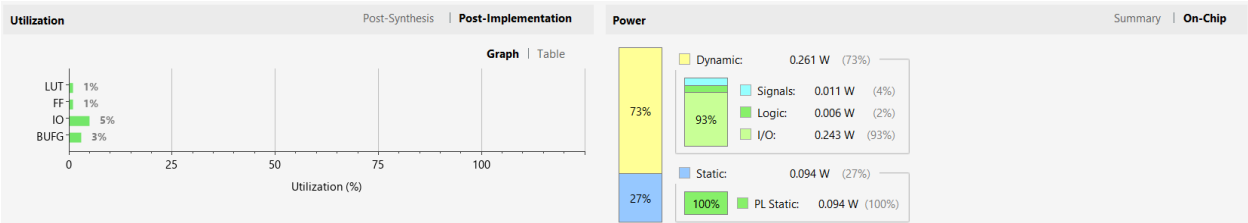
Synchronous_Active_High_Reset



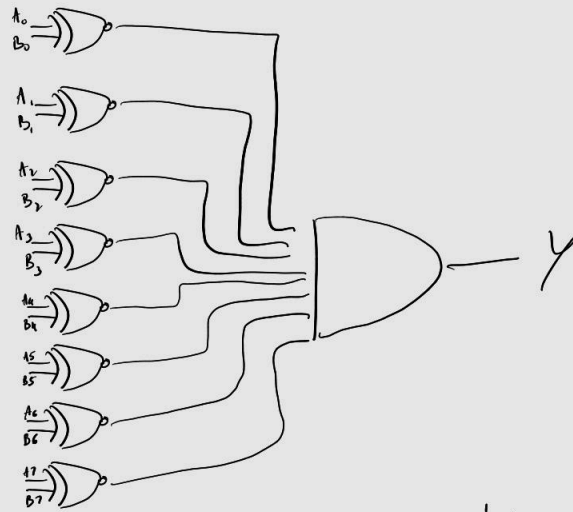
Synchronous_Active_High_Reset_CE



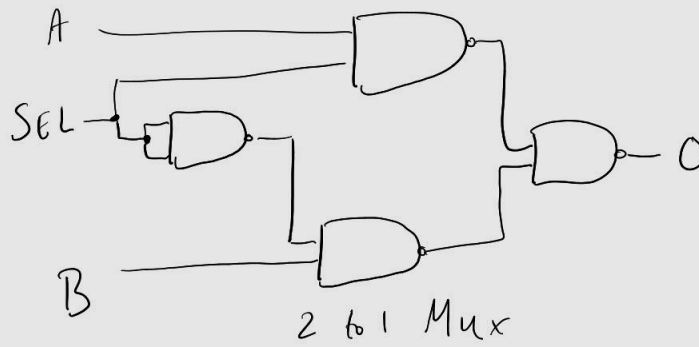
Synchronous_Active_Low_Reset



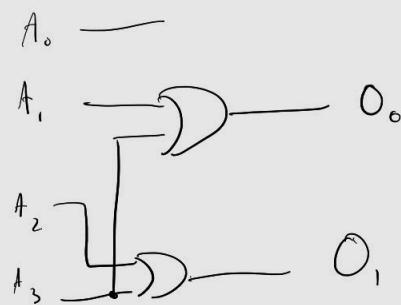
Synchronous_Active_Low_Reset_CE



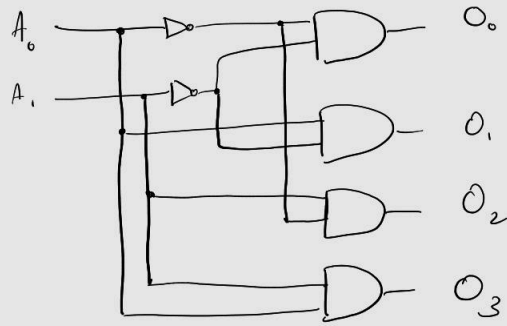
8-bit comparator



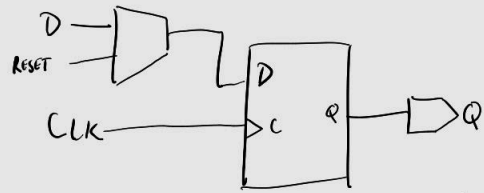
2 to 1 Mux



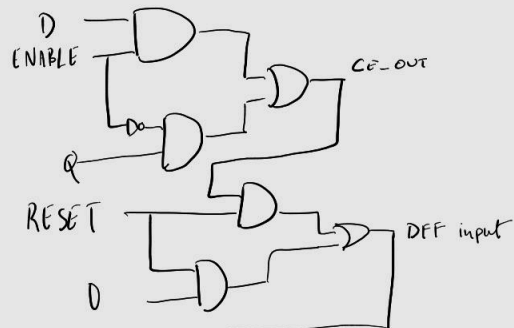
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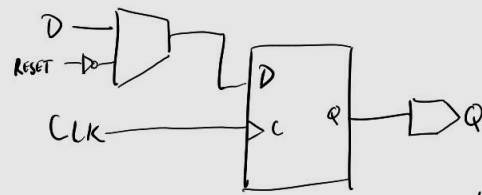
4 bit decoder



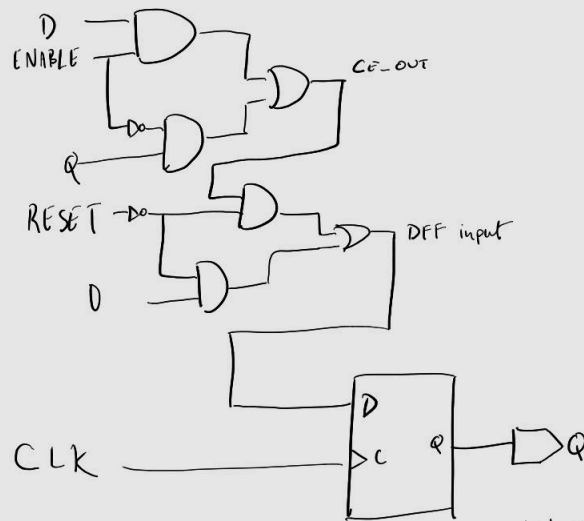
DFF w/ synchronous active high reset



DFF w/ synchronous active high reset w/ CE



DFF w/ synchronous active low reset



DFF w/ synchronous active high reset w/ CE