Department of Computer Science and Engineering School of Electrical and Computer Sciences Indian Institute of Technology, Bhubaneswar

HIGH PERFORMANCE COMPUTER ARCHITECTURE

PROJECT PHASE 2

Analytical Modeling of LLM Computation and Communication on Real CPU/GPU Hardware



Team Members

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1 Introduction

Large Language Models (LLMs) have become essential for tasks like summarization, translation, question answering, and code generation. However, their high computational demands and varying hardware constraints pose challenges for real-world deployment. Efficient inference is crucial for reducing latency, optimizing resource utilization, and ensuring scalability across different platforms.

Understanding the computational behavior of LLMs across different hardware setups helps in identifying performance bottlenecks and improving execution efficiency. Profiling various models under diverse workloads provides insights into optimizing resource allocation. Such analysis is essential for designing scalable AI solutions while balancing speed, accuracy, and energy efficiency.

2 Methodology

2.1 Models Evaluated

We profiled four models:

• Decoder-Only Models: OPT-350M, BLOOM-560M

• Encoder-Decoder Models: T5-Small, BART-Base

2.2 Experiment Setup

• Device: Tesla GPU

• Batch Sizes: 1, 8, 32, 128

• Metrics: Latency, CUDA Execution Time, CPU Execution Time, Memory Bandwidth

• Workloads: Summarization, Question Answering, Code Generation, Translation

3 Initial Results and Observations

3.1 Latency vs. Batch Size

Trend: Latency increases with batch size but varies by model

Observation: Encoder-decoder models (T5, BART) have higher latency due to additional decoder computations.

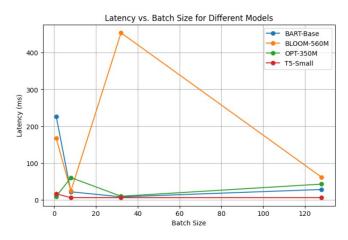


Figure 1: Latency vs Batch Size for different Models

3.2 CUDA vs. CPU Execution Time

Trend: Decoder-only models rely more on CUDA acceleration, while encoder-decoder models involve higher CPU computation overhead.

Observation: CPU bottlenecks impact performance at higher batch sizes.

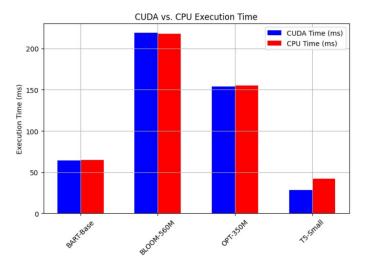


Figure 2: CUDA VS CPU Execution Time Across Models

3.3 Workload-Specific Performance

Summarization & Translation: Encoder-decoder models perform well but at higher latency.

Question Answering & Code Generation: Decoderonly models like OPT-350M are more efficient.

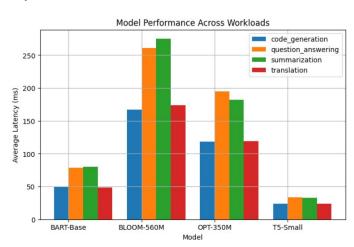


Figure 3: Latency Analysis Across Models

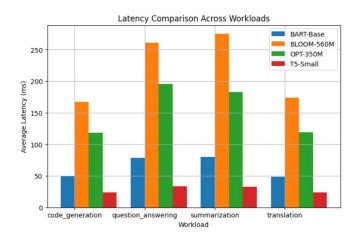
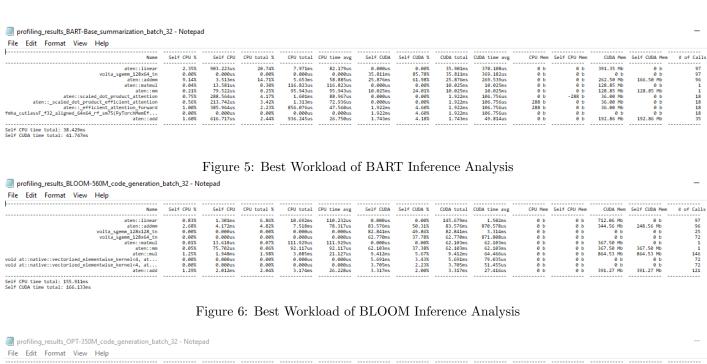


Figure 4: Latency Analysis Across Workloads



| Name | Self CPU % | Self CPU | CPU total % | CPU total | CPU time avg | Self CUDA | Self CUDA % | CUDA total | CUDA time avg | CPU Mem | Self CPU Mem | CUDA Mem | Self CUDA Mem | # of Call |
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| aten::linear | 0.98% | 1.243ms | 9.49% | 12.021ms | 81.773us | 0.000us | 0.00% | 119.884ms | 815.540us | 0 b | 0 b | 474.15 Mb | 0 b | 147 |
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| aten::mm | 0.19% | 234.390us | 0.24% | 299.033us | 99.678us | 9.118ms | 6.86% | 9.118ms | 3.039ms | 0 b | 0 b | 82.40 Mb | 82.40 Mb | 3 |
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Figure 8: Best Workload of T5 Inference Analysis

4 Project Timeline

Table 1: Project Timeline

| Task | Duration | Status |
|-----------------------------|----------|-----------|
| | | |
| Model Selection | Week 1 | Completed |
| Profiling Implementation | Week 2 | Completed |
| of Basic Models | | |
| Data Collection & GPU Setup | Week 3 | Ongoing |
| Advanced Profiling (FLOPs) | Week 4 | Planned |
| Optimization Strategies | Week 5 | Planned |
| Report & Documentation | Week 6 | Planned |

5 Next Steps

- Memory Profiling: Use nvidia-smi to track memory consumption across models.
- Compute FLOPs Estimation: Integrate fv-core.nn.FlopCountAnalysis to estimate model computational complexity.
- Optimization Strategies: Investigate quantization and pruning techniques to improve efficiency.

• Validation on Real Hardware: Test models on different GPU architectures to analyze scalability.

6 Conclusion

This project analyzed the computational and communication characteristics of LLMs on real CPU/GPU hardware. Our profiling indicates that decoder-only models are more efficient for tasks like code generation and QA, while encoder-decoder models offer better summarization and translation accuracy but with higher latency. CPU execution overhead highlights the need for CUDA acceleration.

References

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