**SYNTHESIS\_TOP**

* SINGLE\_PRECISION\_FP\_MULTIPLIER
  + BOOTH
* FLOAT\_MEM (Memory module for storing the input vectors. This can be replaced with a BRAM also)
* MEMORY\_CONTROLLER

For FPGA synthesis

* LCD\_CLK\_UNIT(Clock divider will generate a one microsecond clock)
* NIBBLE\_CONVERTER
* INSTRUCTION\_WORD\_GENERATOR (This is the modified version of the original code taken from<https://reference.digilentinc.com/reference/pmod/pmodclp/reference-manual>.)