Nikhil Chaturvedi
CMPE265 Project Report

1. Clock Distribution for a Backplane

2. Objective : To design a clock distribution for a backplane, on a Daisy-Chain Topology with a Clock Driver (up to 200MHz). ICS553 as the clock driver is used to drive various number of clock receivers, also ICS553.

3. Block Diagram:

The diagram below shows the clock driver ICS553 @ 200MHz (and 133MHz) supporting 4 slots each with an ICS553 clock receiver. Subsequent sections show different schemes of connection and the number of slots as well.

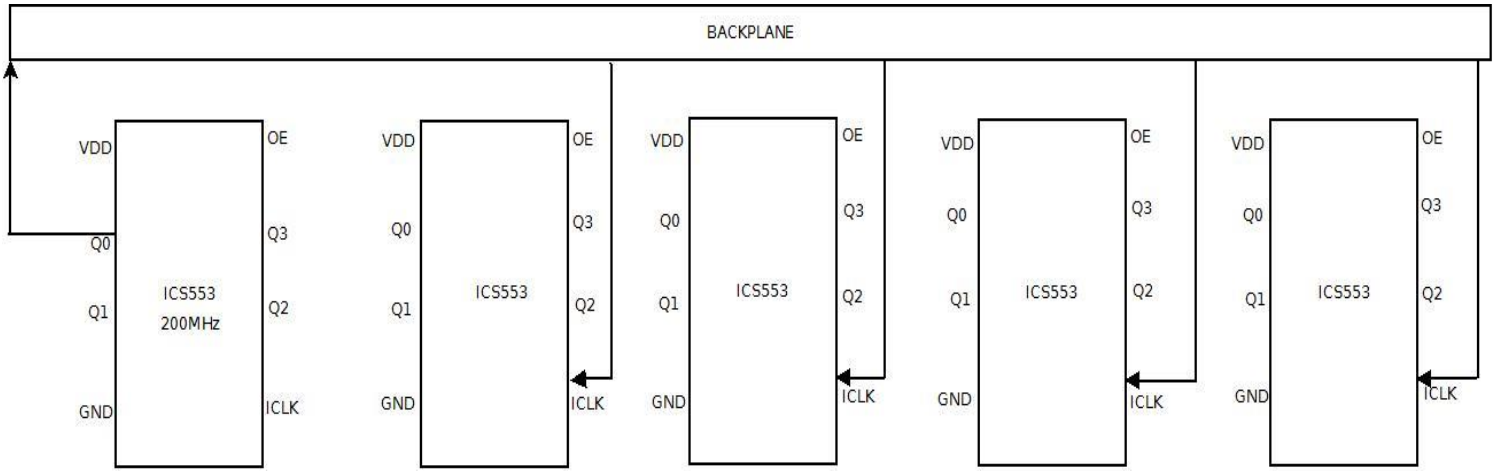

Fig 1: Block diagram of the system

4. Description:

Parameter	**Symbol**	**Min.**	**Typical**	**Max.**
Input High Voltage	VIH	VDD/2+0.7 V		5.5V
Input Low Voltage	VIL			VDD/2 – 0.7 V
Output High Voltage	VOH	2.4 V		
Output Low Voltage	VOL			0.4 V
Nominal Output Impedence	Zo		20 Ohm	
Input Capacitance	CIN		5 pF	

DC Electrical Characteristics for VDD = 3.3 V+-5%

Parameter	**Symbol**	**Min.**	**Typical**	**Max.**
Input Frequency				200 MHz
Output Rise Time	Tor		0.6 ns	1 ns
Output Fall Time	Tof		0.6 ns	1 ns
Propagation Delay		2 ns	2.4 ns	4 ns
Output to output skew			0 ns	50 ps
Device to Device skew				500 ps

AC Electrical Characteristics VDD = 3.3 V +- 5%

The idea behind the design and the backing simulations is branched in two ways. One, to find the skew and operating frequency of a topology that supports various slots(here 4 ,6 and 7) that are driven by a clock driver. The other is to have a completely different topology(as described in section 5, figure 6) as opposed to the one shown in Fig.1 and determine the skew and operating frequency. By this, we intend to draw out different solutions with different combinations of receivers and the topologies used to connect them.

5. Topology:

Fig. 2 shows the topology where the load on the clock driver is a single slot. The backplane trace is not assigned a trace length value as it would depend on the number of slots that we intend to support and the type of design that we choose to connect the clock driver to the receivers(covered in further sections). For the case shown in Fig.2, the backplane trace length was swept from 1” - 20” with 1” increments.

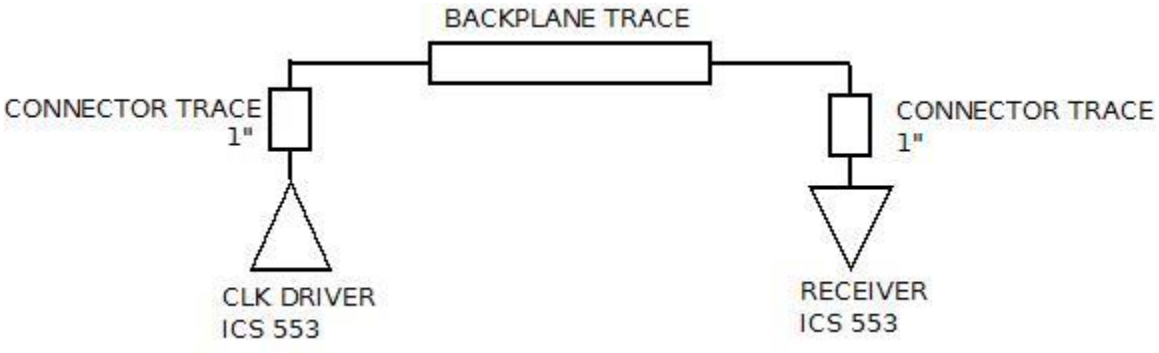

Fig 2: A topology with a clk driver driving one receiver.

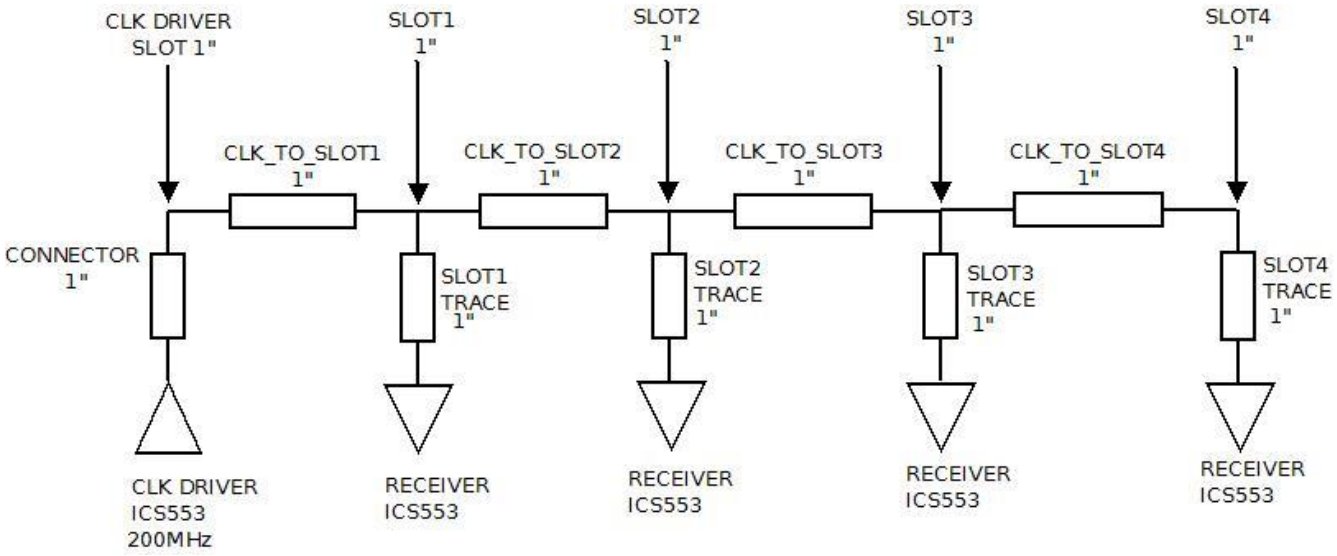

Fig.3. A topology that supports 4 slots at 200MHz

Fig.3 shows a topology where the clock driver @ 200MHz supports 4 slots.

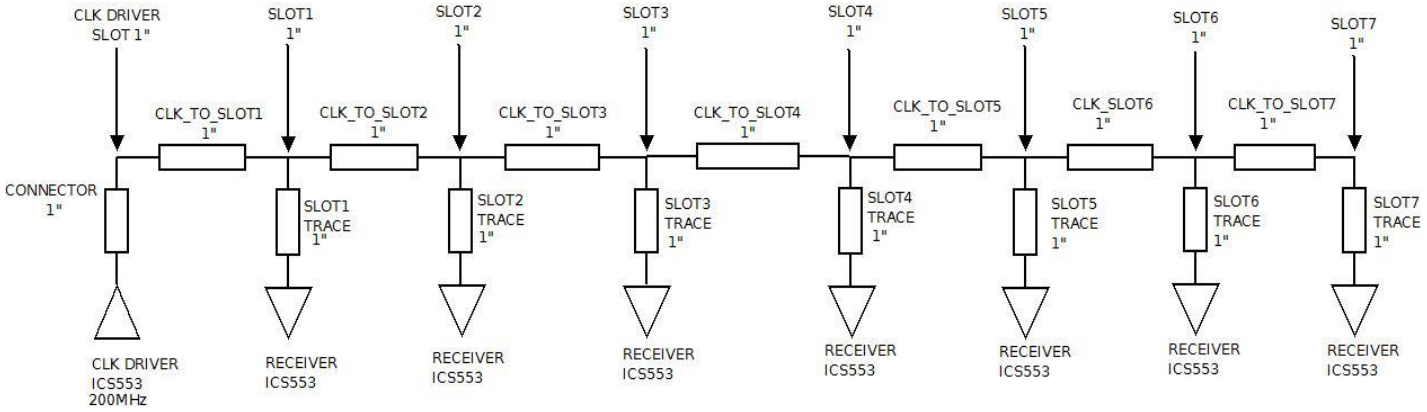

Fig.4. A topology that supports 7 slots at 200MHz

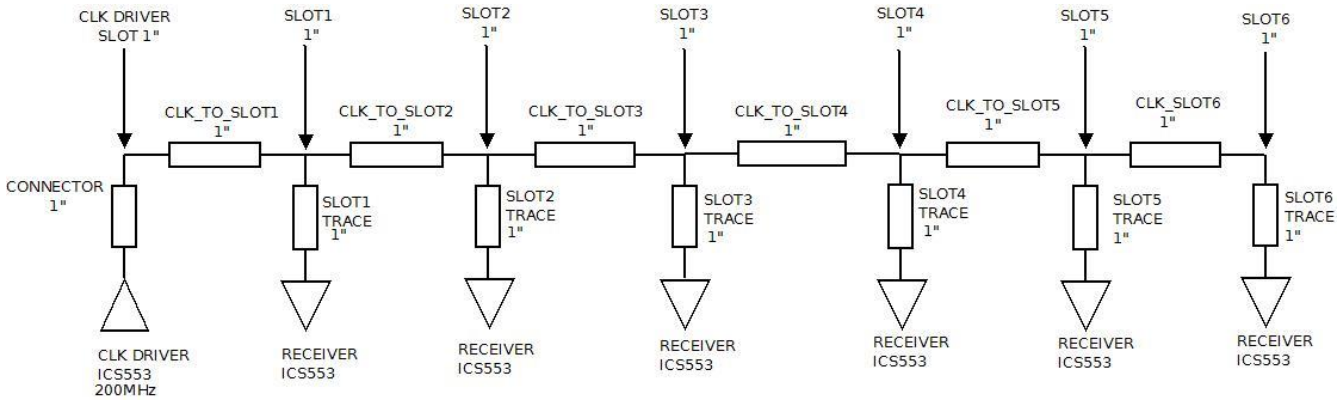

Fig.5. A topology that supports 6 slots at 200MHz

As mentioned in section 3, another possible scheme of connections can be,

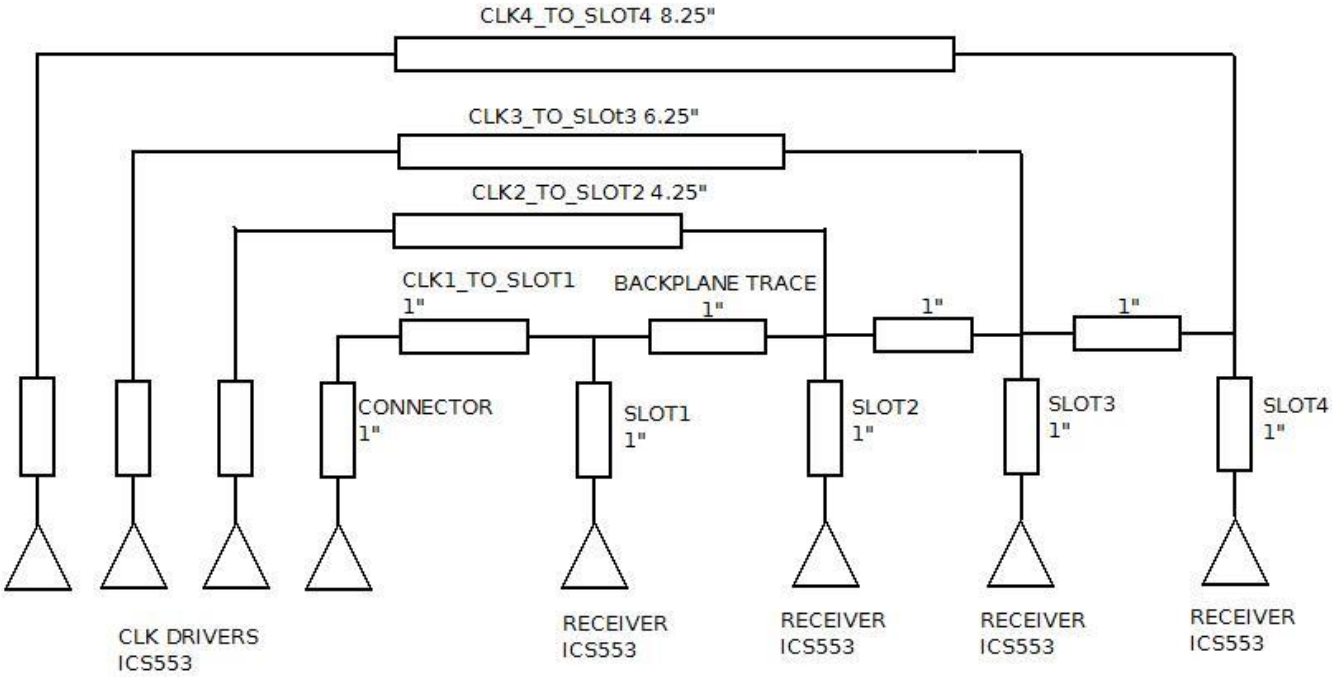

Fig.6. A topology with 4 different drivers connected to 4 slots.

Fig.6 shows connections made to 4 slots each driven by 4 different drivers. This topology was conceived to compare the signal waveforms of this scheme with that of the earlier topologies, due to the fact that a single driver driving 4 different slots at different lengths has more load than each slot driven by a single driver. The results are discussed in the subsequent sections.

6. Simulation Plan:

6.1. Assumptions

As discussed in section 4, the plan is divided into two ways. One plan was a series of changes in the topology with respect to the number of slots we support and the other being the way the clock drivers are connected to the receivers.

First, let us go through the simulation plan for the topologies as shown in figures 2 through 5.
For deciding the length of the backplane, two approaches were made. One, the number of slots supported by the clock driver was assumed to be 4, in which case, the backplane trace length would be constant, with 1” for slots, 1” between slots and 1” for connectors. The other, where the backplane trace length was incremented by 1” from a length of 1” through 20”, thereby determining the number of slots that can be supported, judging by the waveforms and the propagation delay. In this case, the waveforms were satisfactory even at a length of 20” from the clock driver. But a length of less than (or equal to) 15” was chosen since 20” is a large distance with respect to a circuit board.
For the second design shown in fig.6, the distance between each slot was kept a constant 1” and the trace length from each driver to an individual receiver was kept at 1”, 4.25”, 6.25” and 8.25” respectively.

6.2. Simulation Setup:

- The series termination at the clock driver was swept from 1Ohm to 10 Ohm, to determine the correct value (as opposed to using a constant 33 Ohm which the data sheet suggested, which resulted in poor waveforms). This case is true for all the topologies mentioned in the previous sections.
- To find the maximum length of the backplane trace, the trace length from the driver to the receiver was swept from 1" to 20" with 1" increments, following parameters were used (for the topology in Fig.2).

Parameters

Name	Value	Count
⊟ CIRCUIT		**1**
autoSolve	Off	1
tlineDelayMode	length	1
userRevision	1.0	1
⊟ DESIGN		**1**
⊟ LOAD1		**1**
bufferModel	553_3IN_IN6_3	1
mappingTag		1
⊟ CLKDRIVER		**1**
bufferModel	553_3IN_3V6XX	1
mappingTag		1
⊟ CLKSERIES		**1**
resistance	1 Ohm	1
⊟ R3		**1**
resistance	50 Ohm	1
⊟ CLKTRACE		**1**
impedance	51 ohm	1
length	1000.00 MIL, 20000.00 MIL: 100	20
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊟ V1		**1**
voltage	1.8 V	1

- Parameters for the case where the number of slots is maintained at a constant 4, is shown below,

Parameters

Name	Value	Count
⊟ CIRCUIT		**10**
autoSolve	Off	1
tlineDelayMode	length	1
userRevision	1.0	1
⊟ DESIGN		**10**
⊟ CLKDRIVER		**1**
bufferModel	553_3IN_3V6XX	1
mappingTag		1
⊟ CLKSERIES		**10**
resistance	1 Ohm, 10 Ohm: 1 Ohm	10
⊟ CLKSLOT4		**1**
impedance	CLKTRACE.impedance	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ CLKTOSLOT1		**1**
⊞ CLKTOSLOT2		**1**
⊞ CLKTOSLOT3		**1**
⊟ CLKTRACE		**1**
impedance	51 ohm	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊟ LOAD1		**1**
bufferModel	553_3IN_IN6_3	1
mappingTag		1
⊞ LOAD2		**1**
⊞ LOAD3		**1**
⊞ LOAD4		**1**
⊞ R19		**1**
⊟ SLOT1		**1**
impedance	50 ohm	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊟ SLOT1_2		**1**
impedance	CLKTRACE.impedance	1
length	500.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ SLOT2		**1**
⊞ SLOT2_1		**1**
⊞ SLOT2_2		**1**
⊞ SLOT3		**1**
⊞ SLOT3_1		**1**
⊞ SLOT3_2		**1**
⊞ SLOT4		**1**
⊞ SLOT4_1		**1**
⊞ V15		**1**

- Parameters for topology with support for 7 slots is shown below, with repeating values not shown.

Parameters

Name	Value	Count
⊟ CIRCUIT		**10**
autoSolve	Off	1
tlineDelayMode	length	1
userRevision	1.0	1
⊟ DESIGN		**10**
⊞ CLKDRIVER		**1**
⊟ CLKSERIES		**10**
resistance	1 Ohm, 10 Ohm: 1 Ohm	10
⊟ CLKTOSLOT1		**1**
impedance	CLKTRACE.impedance	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ CLKTOSLOT2		**1**
⊞ CLKTOSLOT3		**1**
⊞ CLKTOSLOT4		**1**
⊞ CLKTOSLOT5		**1**
⊞ CLKTOSLOT6		**1**
⊞ CLKTOSLOT7		**1**
⊟ CLKTRACE		**1**
impedance	51 ohm	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ LOAD7		**1**
⊟ LOAD1		**1**
bufferModel	553_3IN_IN6_3	1
mappingTag		1
⊞ LOAD2		**1**
⊞ LOAD3		**1**
⊞ LOAD4		**1**
⊞ LOAD5		**1**
⊞ LOAD6		**1**
⊞ R24		**1**
⊟ SLOT1		**1**
impedance	50 ohm	1
length	1000.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ SLOT1_2		**1**
⊞ SLOT2		**1**
⊞ SLOT2_1		**1**
⊟ SLOT2_2		**1**
impedance	CLKTRACE.impedance	1
length	500.00 MIL	1
traceGeometry	Microstrip	1
velocity	5600 mil/ns	1
⊞ SLOT3		**1**
⊞ SLOT3_1		**1**
⊞ SLOT3_2		**1**
⊞ SLOT4		**1**
⊞ SLOT4_1		**1**
⊞ SLOT4_2		**1**
⊞ SLOT5		**1**
⊞ SLOT5_1		**1**
⊞ SLOT5_2		**1**

- Parameters for support for 6 slots are the same as that for 7 slots. 6 slots were chosen to be simulated when the backplane trace length for 7 slots seemed to high.

6.3. Simulation Methodology:

- Vary the series resistance to the clock from 1 Ohm to 10 Ohm with 1 Ohm increments.
- The frequency simulated is 200Mhz with stimulus frequency set at 400Mhz.
- For topology in Fig.2, vary the backplane trace length from 1" to 20" with 1" increments.
- The connector trace length is kept a constant 1", the distance between each slot is kept a constant 1", the slot width is kept at a constant 1". This is true for all topologies from Fig.2 through Fig.5.
- For the topology is Fig.2, the maximum length is 20" which was reduced to lesser values as mentioned in section 6.1.
- For topologies from Fig.3 through Fig.5, keep the values constant as mentioned in step 4.
- Impedance of the traces is 51 Ohm.
- The propagation delay between clock driver-slot1, slot1-maximum slot supported, clock driver-maximum slot supported is determined from the waveforms after running the simulations, at the Vref level, which is 1.65V. The waveforms are checked for their correctness by looking for monotonic factors, at VIH and VIL levels, which are 2.35V and 0.95V respectively.
- Termination (pull-up, 40-50Ohm resistance, 1.8V) is provided at the last slot. This is determined by trial-error method for different values for resistance; the voltage level is chosen as VDD/2 ((3.3V + 5%)/ 2 ~ 1.8V).
- Repeat steps 3 through 9 for 133Mhz frequency and stimulus frequency set at 266Mhz.
- For the topology shown in Fig.6, the frequency simulated is 200MHz. The connector traces are a constant 1", the distance between each slot is a constant 1", the trace length from each clock driver to their individual receivers are 1", 4.25", 6.25" and 8.25" respectively. These length were chosen from topology with 4 slots Fig.3 and adding extra trace length to account for individual routing for each driver except the routing from clock driver to slot1.

7. Simulation Results:

The simulated topologies for all the cases discussed and their results are shown below, for both 200MHz and 133Mhz cases and the also the secondary design (Fig.6)

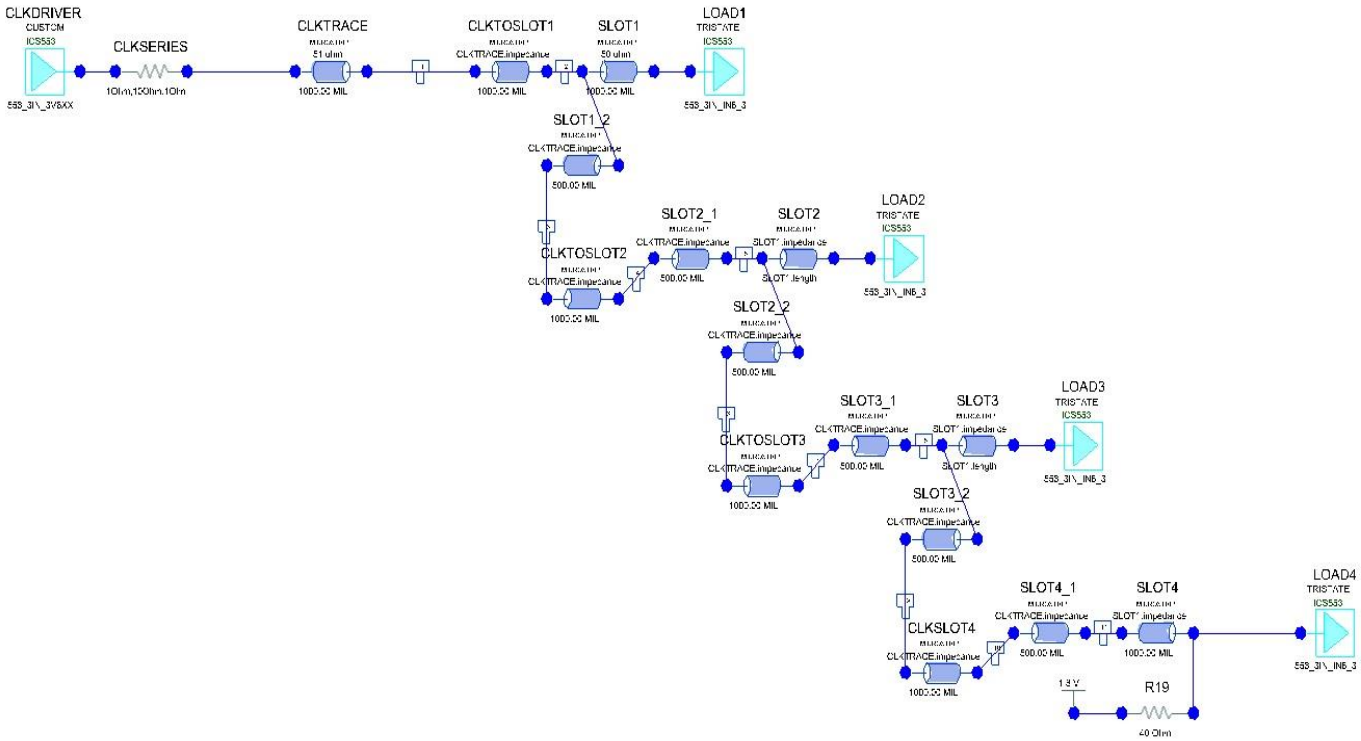

Fig.10: Simulation topology for 4 slots.

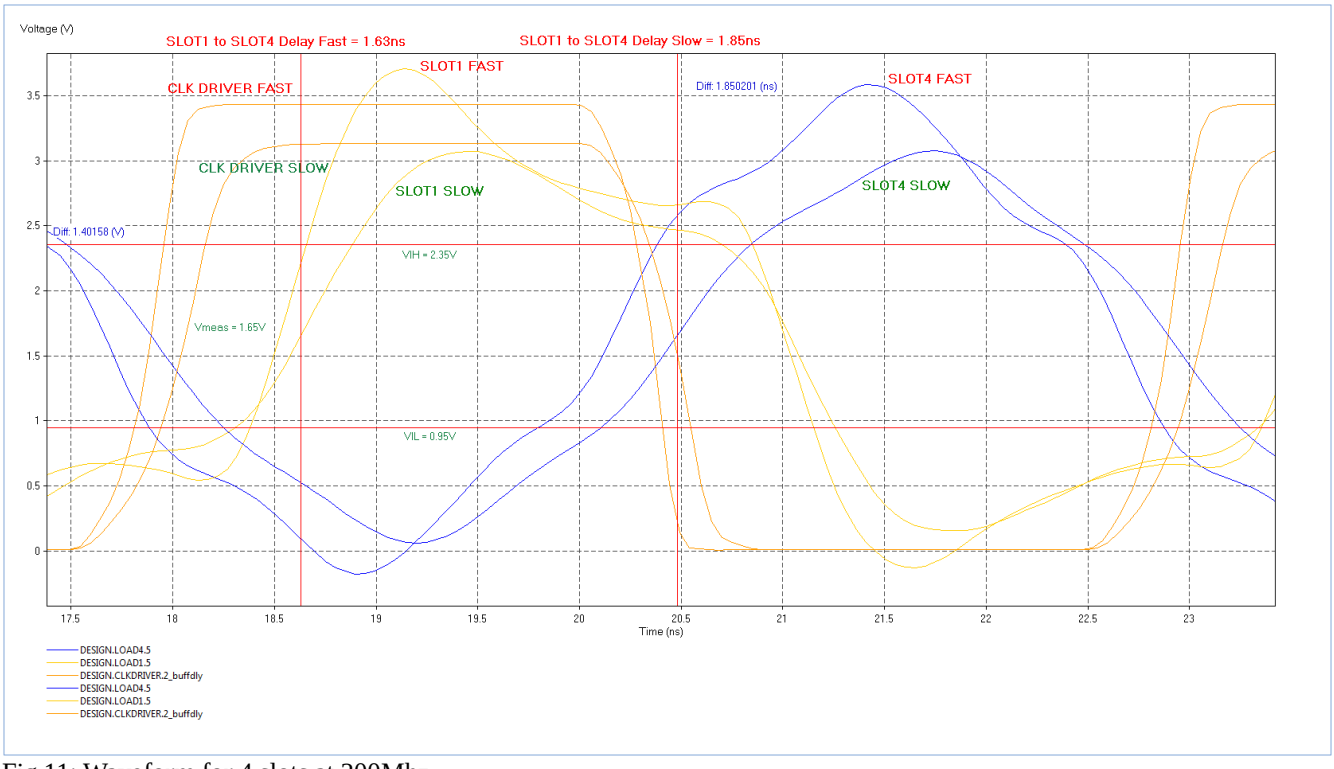

Fig.11: Waveform for 4 slots at 200Mhz

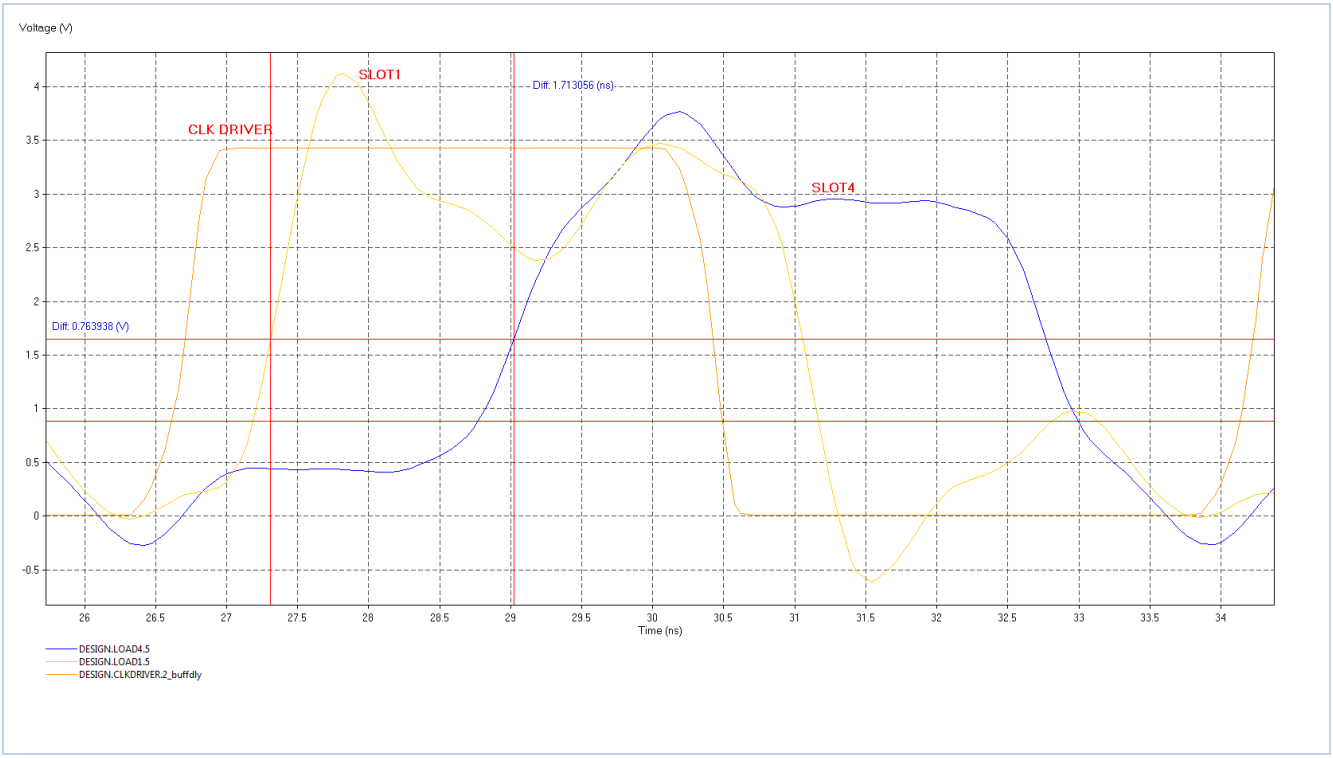

Fig.12: Waveform for 4 slots at 133Mhz, showing skew between Slot1 and Slot4.

Fig.13: Simulation topology for 7 slots.

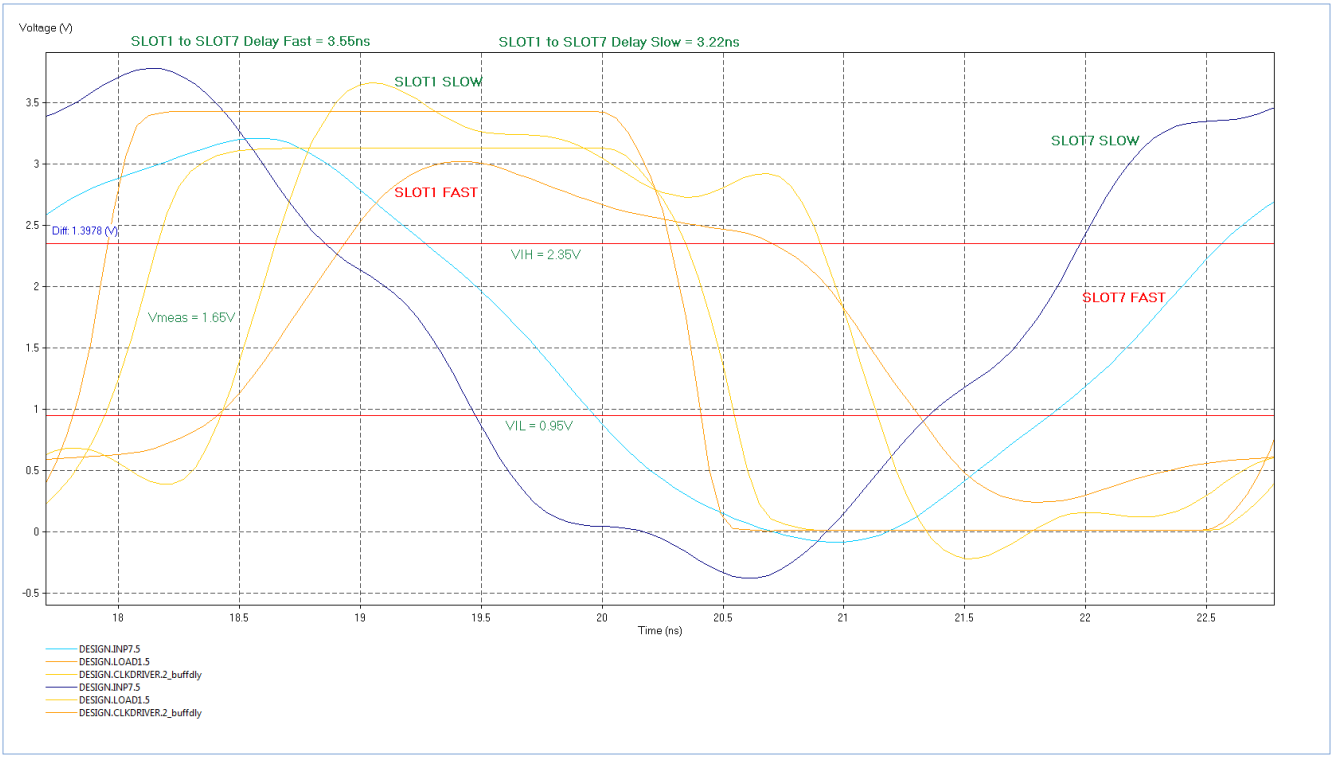

Fig.14: Waveforms for 7 slots at 200MHz.

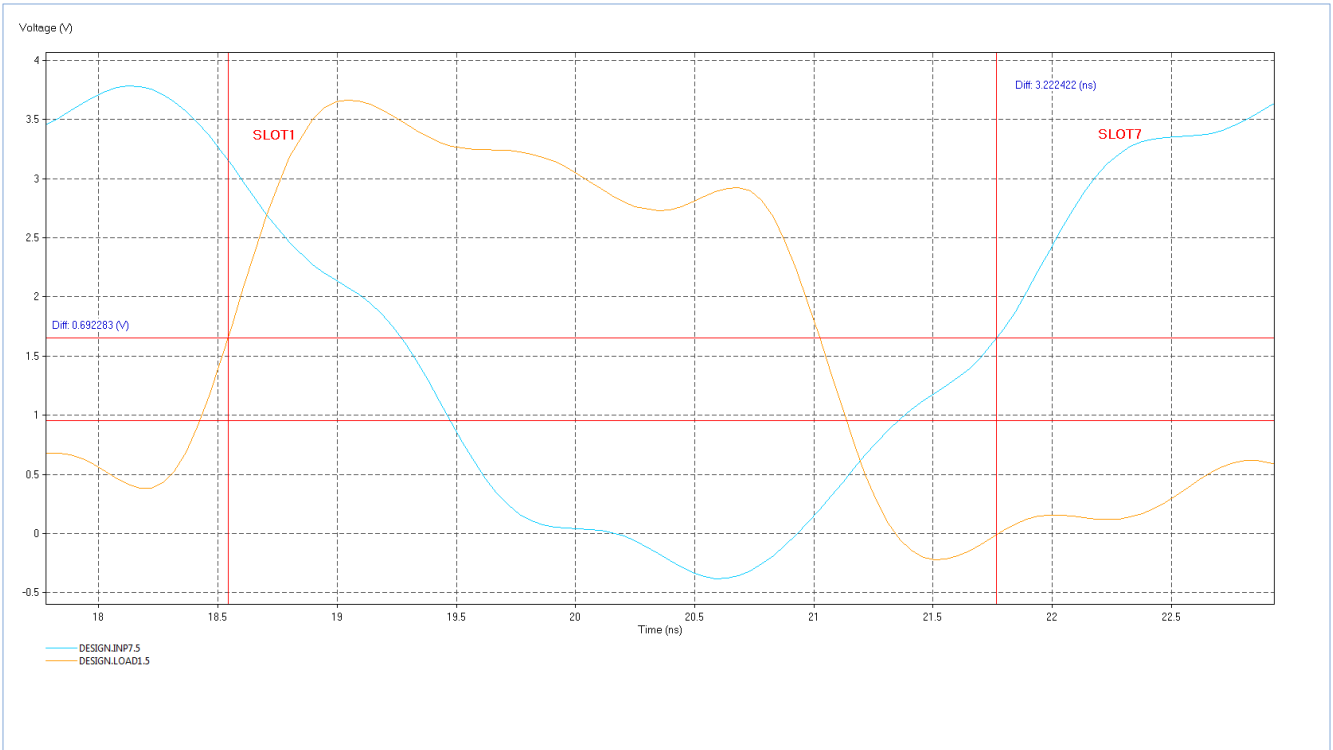

Fig.15: Waveforms for 7 slots at 133MHz

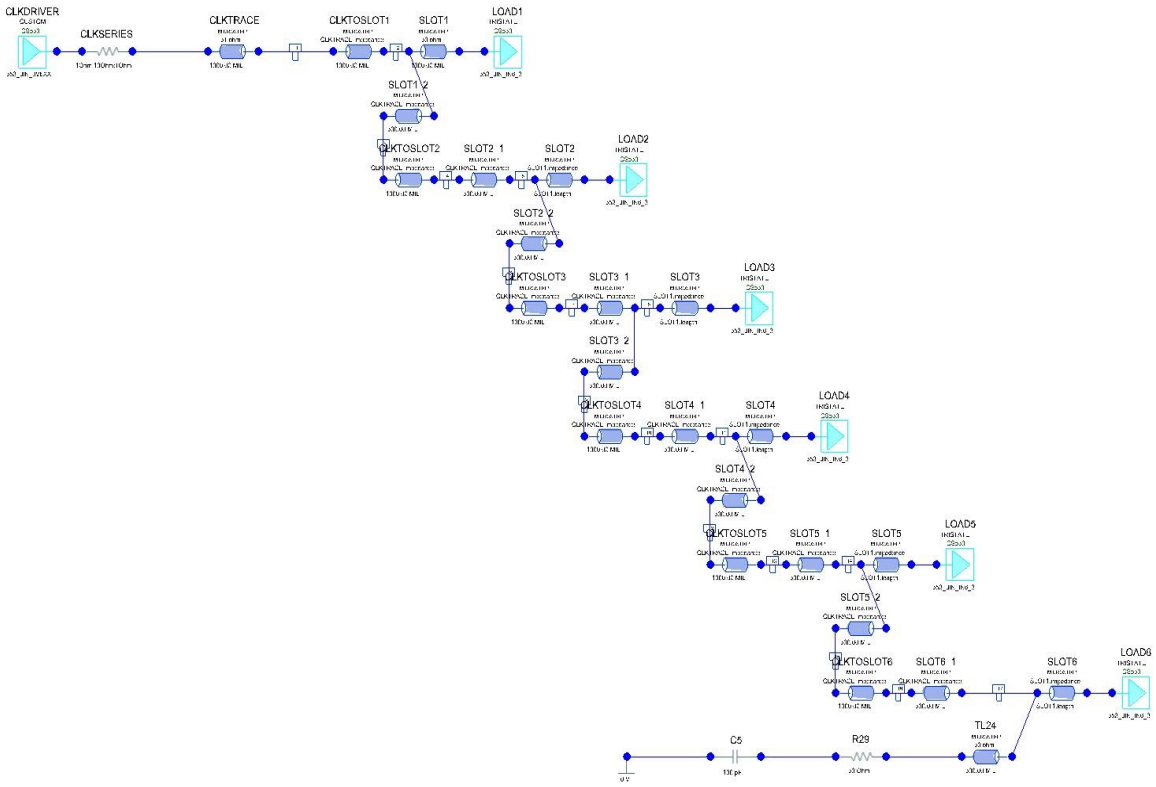

Fig.16: Simulation topology for 6 slots.

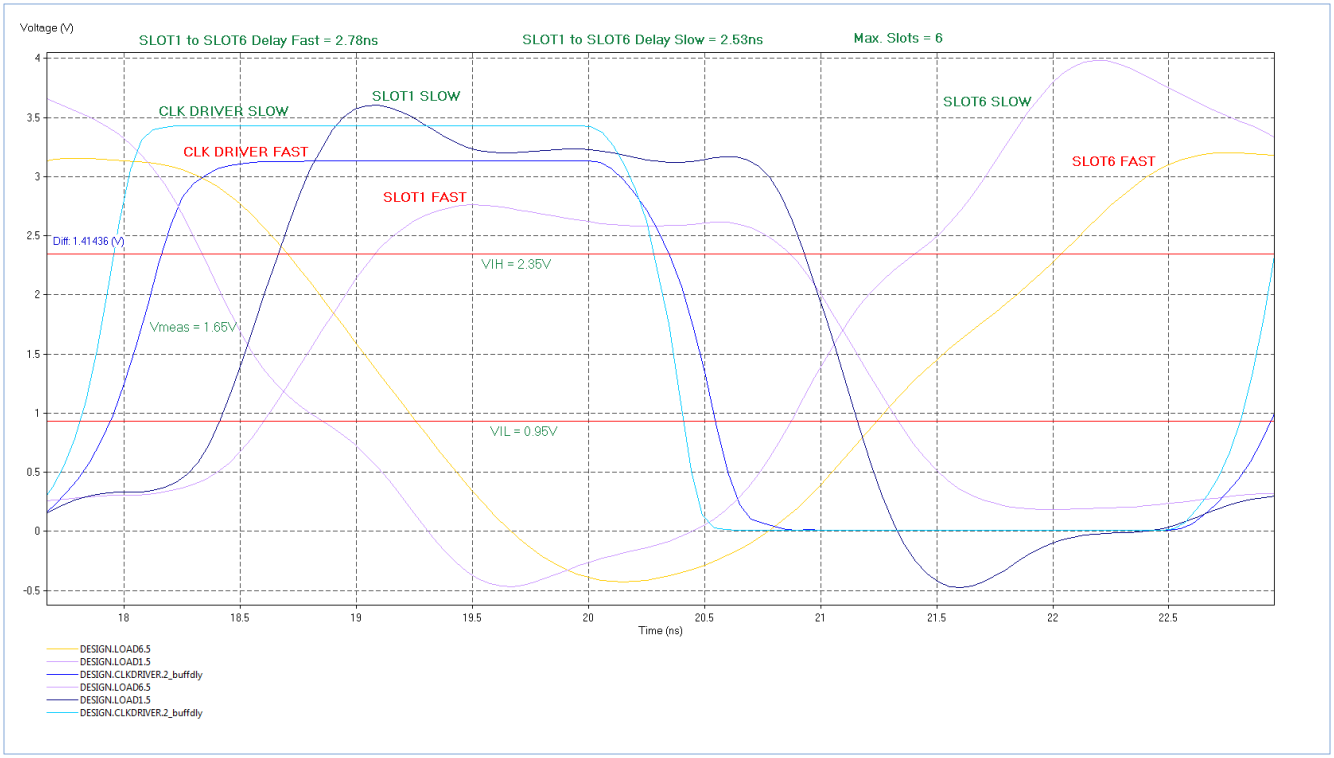

Fig.17: Waveforms for 6 slots at 200MHz

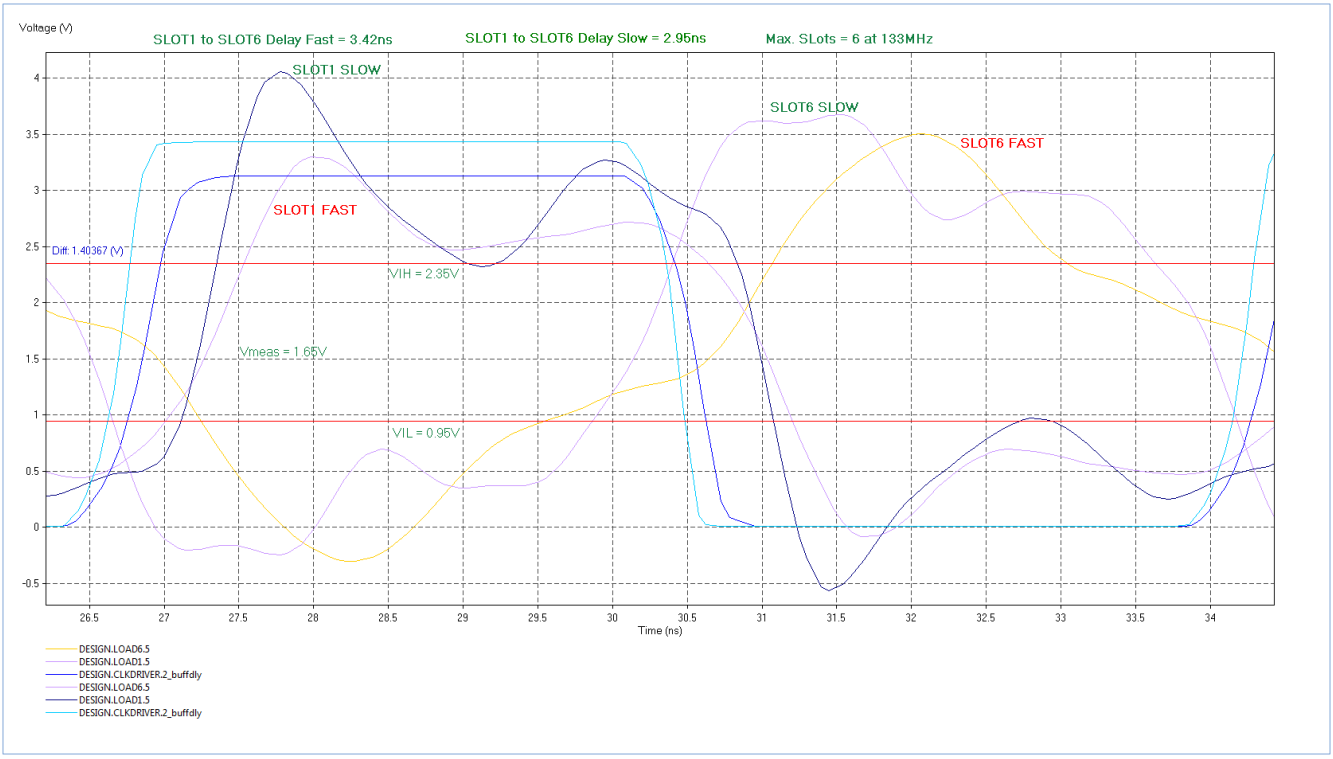

Fig.18: Waveforms for 6 slots at 133MHz.

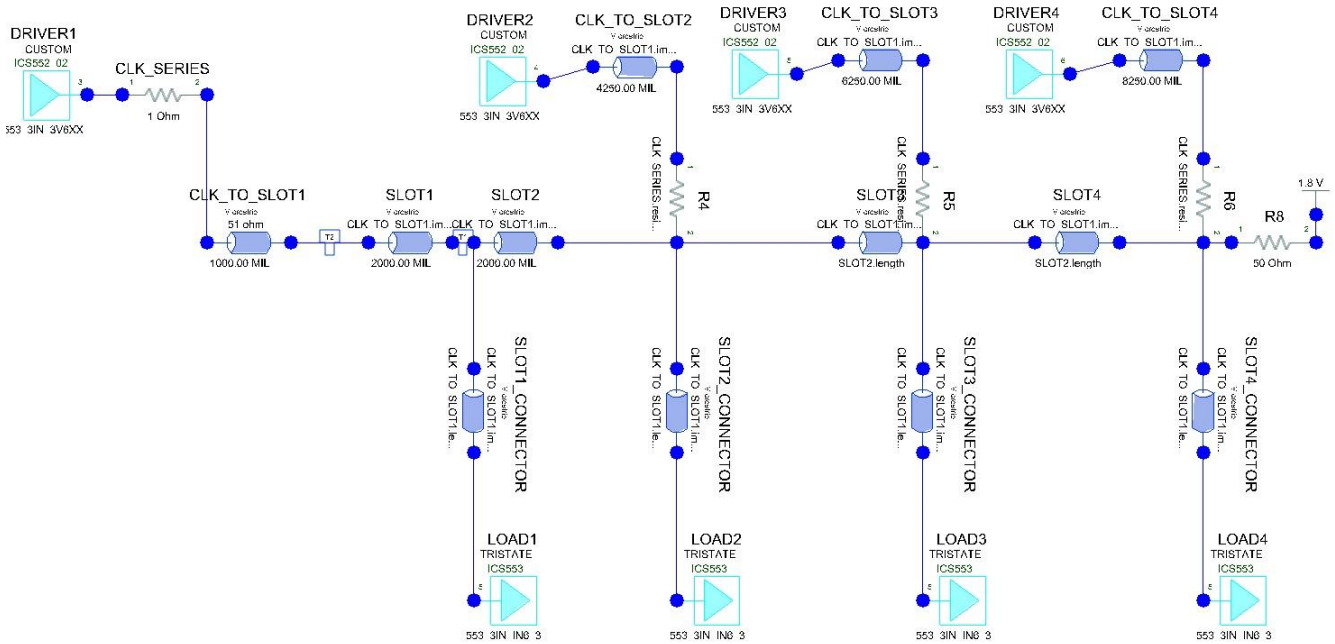

Fig.19: Simulation topology for the second design.

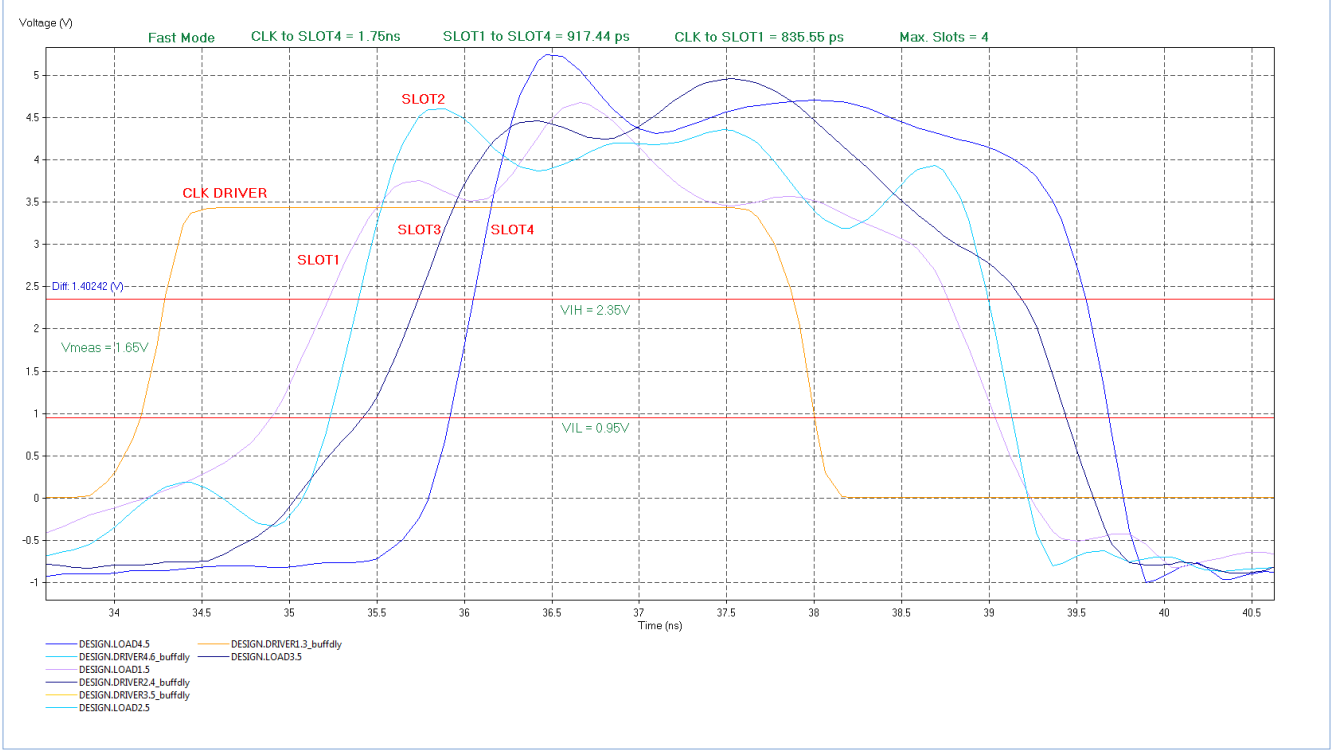

Fig.20: Waveforms for the second design at 200MHz, fast mode.

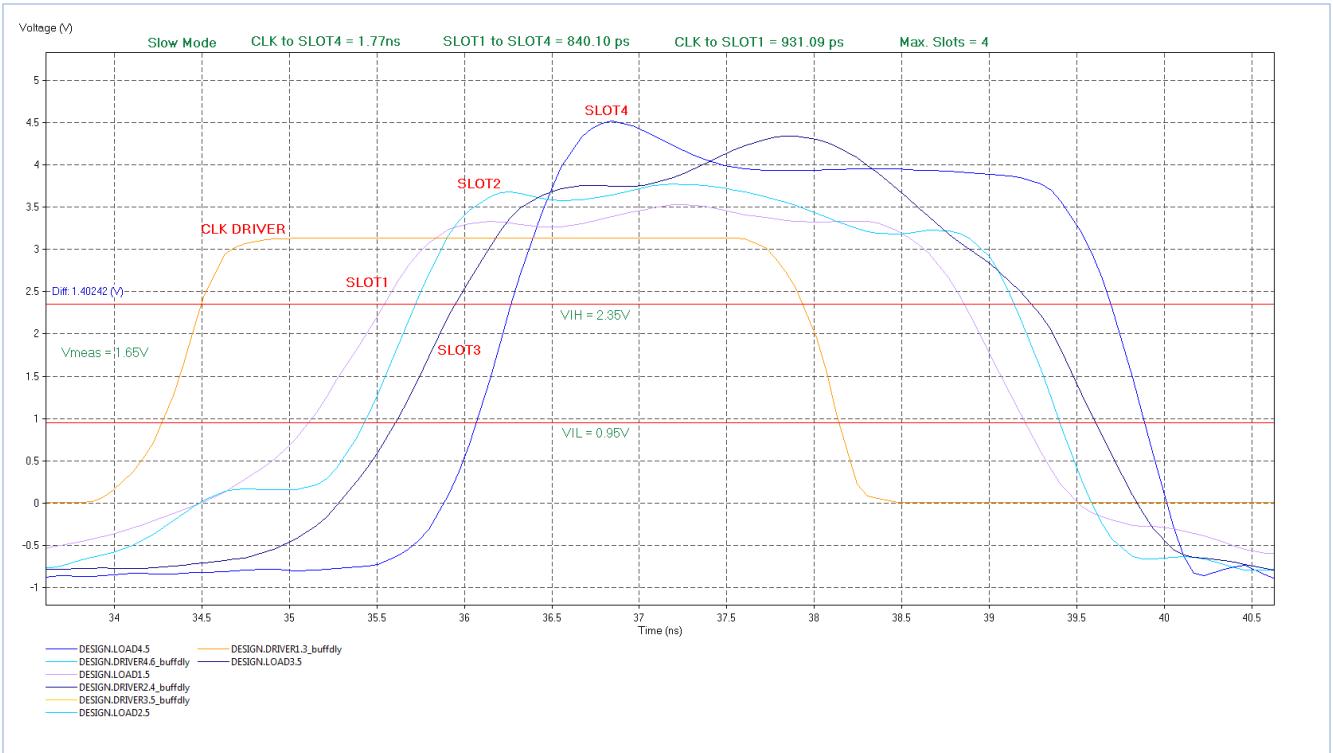

Fig.21: Waveforms for the second design at 200MHz, slow mode.

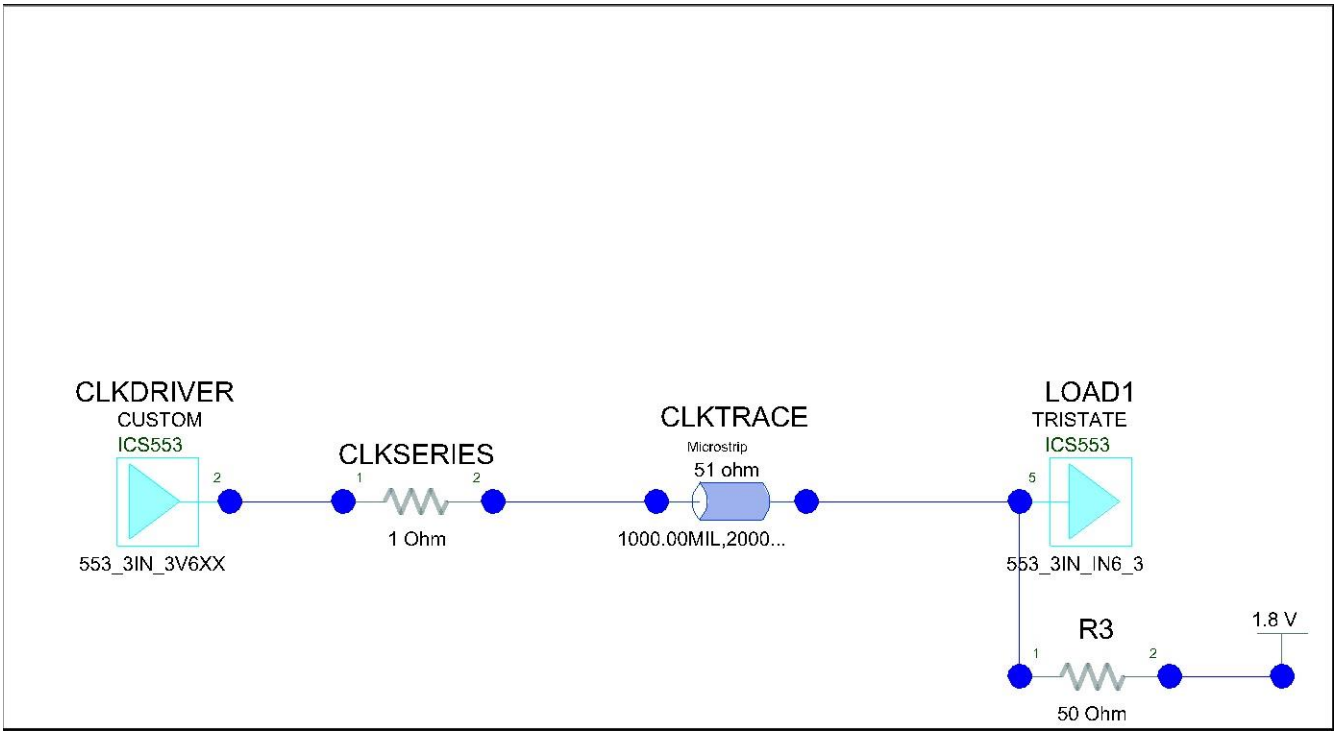

Fig.22: Simulation topology for finding maximum backplane trace length.

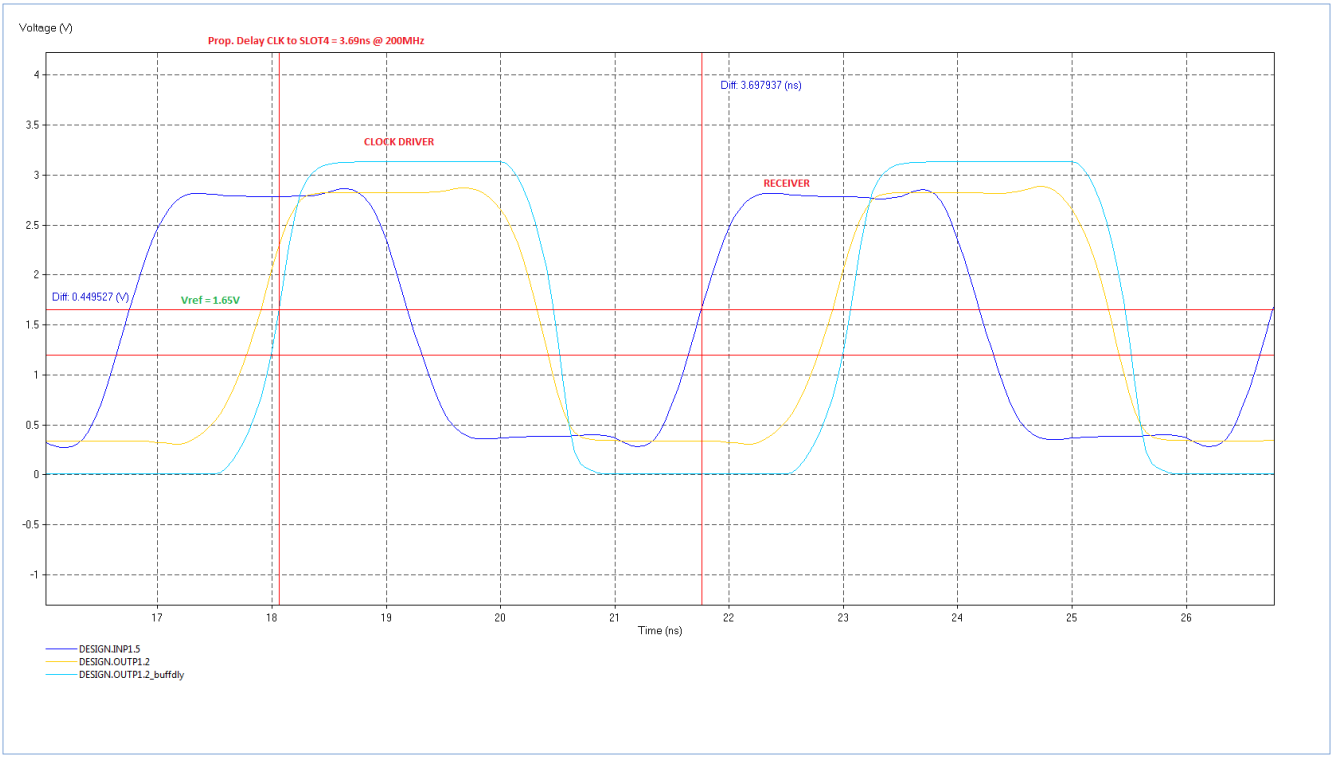

Fig.23: Waveforms for the topology to find the maximum length of the backplane trace at 200MHz.