

Nikhil Pratap Ghanathe

PHD CANDIDATE AT UNIVERSITY OF BRITISH COLUMBIA

✉ nikhilghanathe@ece.ubc.ca 🏠 nikhilghanathe.github.io 📧 [nikhilghanathe](https://twitter.com/nikhilghanathe) 📄 [nikhil-pratap-ghanathe](https://github.com/nikhil-pratap-ghanathe)

Education

University of British Columbia (UBC)

DOCTOR OF PHILOSOPHY IN ELECTRICAL AND COMPUTER ENGINEERING

Vancouver, BC, Canada

September 2019-PRESENT

University of Florida (UFL)

MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

Gainesville, FL, USA

August 2014-May 2016

Visvesvaraya Technological University

BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION

Bangalore, India

September 2010 - July 2014

Publications

QUTE: Quantifying Uncertainty in TinyML models with Early-exit-assisted ensembles

NIKHIL P GHANATHE, STEVE WILTON

Preprint Version, Under Review.

T-RECX: Tiny-Resource Efficient Convolutional neural networks with early-eXit (**BEST PAPER AWARD**)

NIKHIL P GHANATHE, STEVE WILTON

Proceedings of the 20th ACM International Conference on Computing Frontiers (CF '23), , pp. 123–133, 2023

MAFIA: Machine Learning Acceleration on FPGAs for IoT Applications

NIKHIL P GHANATHE, VIVEK SESHADRI, RAHUL SHARMA, STEVE WILTON, AAYAN KUMAR

In 2021 31st International Conference on Field-Programmable Logic and Applications (FPL) (pp. 347-354). IEEE.

Compiling KB-sized machine learning models to tiny IoT devices

SRIDHAR GOPINATH, NIKHIL P GHANATHE, VIVEK SESHADRI, RAHUL SHARMA

In 40th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI 2019). ACM, New York, NY, USA, 79-95

Software and firmware co-development using high-level synthesis

NIKHIL P GHANATHE, ALEXANDER MADORSKY, HERMAN LAM, DARIN ACOSTA *et al.*

Presented at the Topical Workshop on Electronics for Particle Physics (TWEPP2016)

Published in the Journal of Instrumentation, Volume 12, January 2017

Work Experience

Microsoft Research

RESEARCH FELLOW

Bangalore, India

Aug. 2017 - Aug. 2019

- Developed and integrated a FPGA-backend for a Domain Specific Language to run KB-sized ML models on low-cost FPGAs for IoT
 - Improved productivity and performance by achieving 10x speedup compared to Vivado High-level Synthesis Compiler and 211x better than microcontroller implementations
- Collaborated with University of Toronto to explore training of deep Neural Networks (LSTMs) on FPGAs

University of Florida

RESEARCH ENGINEER + GRADUATE RESEARCH ASSISTANT

Gainesville, FL-USA

May 2015 - July 2017

- Co-developed Software & Firmware (Verilog) models for the CMS Level-1 Muon Track finder at the Large Hadron Collider at CERN
 - Led a team to investigate & formulate high-level synthesis techniques to boost productivity of FPGA-firmware development
 - Developed novel techniques and code optimizations for latency control, improving throughput and scheduling functions
 - Code-base integrated into Compact Muon Solenoid Software framework (CMSSW)
 - Achieved improvement in latency (by one clock cycle) and resource consumption (~15%) using methods developed

Indian Space Research Organization

ENGINEERING INTERN

Bangalore, India

Feb 2014 - May 2014

- Designed a system to detect and estimate relative speed between star sensor and celestial bodies
 - Developed FPGA-based image acquisition hardware on a rad-hard FPGA; Novel algorithm reduced resource usage by 50%

Presentations and Non-peer reviewed Contributions

Improving battery-life in ultra-low-power devices using early-exit networks

TALK | UBC ECE RESEARCH DAY

Vancouver, Canada

February 2024

Accelerating edge machine learning algorithms on low-cost FPGAs

TALK | NSERC COHESA ANNUAL GENERAL MEETING

Vancouver, Canada

October 2022

Compiling Machine learning to low-cost Hardware

INDUSTRY PRESENTATION | MICROSOFT TECHFEST

Redmond, Washington-USA

February 2019

Endcap Muon Trigger firmware and software co-development using Vivado HLS

INVITED TALK | EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH (CERN)

CERN, Geneva-Switzerland

April 2016

High-level synthesis for CMS Endcap Muon Trackfinder

INVITED TALK | FERMI NATIONAL ACCELERATOR LABORATORY

Batavia, Illinois-USA

March 2016

Systolic Array Based SGEMM on Arria10

PRESENTATION | SUPERCOMPUTING CONFERENCE

Austin, Texas-USA

November 2015

Leadership and Volunteer

- **UBC Engineering Mentor** (mentoring two students) Oct 2023- April 2024
- **UBC ECE Graduate Student Lab Ambassador** Sept 2022- Aug 2024
- **UBC Graduate Student Well-being Ambassador** Sept 2022- Aug 2023
- **Collaborator**, Workshop on Machine Learning on Constrained Hardware by **Microsoft Research**, India Aug 2018-Oct 2018
- **Collaborator**, Center for High-performance and Reconfigurable Computing Annual Workshop at **Kennedy Space Center, NASA** Dec 2015

Achievements and Extracurriculars

- **Distinguished Lightning Talk Award** at UBC ECE Research Day
- **ACM Best Paper Award** at International Conference on Computing Frontiers (CF'23)
- **College of Engineering Achievement Award Scholarship**, University of Florida
- **Academic Excellence Award** by the **Indian Space Research Organization**