IT209: Tutorial

- 1. The ARM processor registers R13, R14, and R15 are architecturally used for special purposes. Which is the correct respective sequence of special purpose registers?
 - A) PC, LR, SP
 - B) LR, PC, SP
 - C) SP, LR, PC
 - D) LR, SP, PC
- 2. A cache that supports dirty bits to manage the most recently written value to a given memory location in the memory hierarchy is referred to as a
 - A) Write-back cache.
 - B) Write-through cache.
 - C) Set-associative cache.
 - D) Fully-associative cache.
- 3. What the above program is doing?

```
AREA PROGRAM, CODE, READONLY
ENTRY
MOV R1, #0X14
MOVS R2, R1, LSR #0X06
MOVEQ R1, R1, LSL #0X05
```

END

- A) Shift left 5 bits conditionally when zero is set.
- B) Shift left 5 bits conditionally when zero is reset.
- C) Shift right 5 bits conditionally when zero is set.
- D) Shift right 5 bits conditionally when zero is reset.
- 4. The given program calculates the largest number of two. Fill in the instruction accordingly to get the correct result.

```
AREA PROGRAM, CODE, READONLY
ENTRY

MAIN LDR R1, VALUE1
LDR R2, VALUE2
CMP R1, R2
MOV R1, R2
DONE STR R1, RESULT
END
```

- 5. What does I=1 and F=1 in the Program Status Register on reset signify?
- 6. What function does the given program perform?

```
AREA PROGRAM, CODE, READONLY
ENTRY
MAIN LDR R1, VALUE1
MVN R1, R1
STR R1, RESULT
END
```

7. What will be the content of the register R7 after the execution of the following program?

```
AREA PROGRAM, CODE, READONLY
ENTRY
MOV R6, #10
MOV R7, #1
LOOP CMP R6, #0
MULGT R7, R6, R7
SUBGT R6, R6, #1
STOP B STOP
END
```

- A) 0x00000009
- B) 0x000000A
- C) 0x00375F00
- D) 0x00000000
- 8. What will be the content of the register R2 after the execution of the following program?

```
AREA PROGRAM, CODE, READONLY
ENTRY
MOV R0, #0X11
LSL R1, R0, #1
LSL R2, R1, #1
END
```

- A) 0x00000110
- B) 0x00000022
- C) 0x00000101
- D) 0x00001101

9. What will be the output of the following program?

```
AREA PROGRAM, CODE, READONLY
ENTRY

MOV R0, #4

MOV R1, #3

MUL R1, R1, R0

END
```

- A) 12
- B) 0
- C) 4
- D) Error occurs

10. What will be the content of the register R1 and R5 after the execution of the following program?

```
AREA PROGRAM, CODE, READONLY
ENTRY

LDR R1, =-4
LDR R5, =-4
LDR R3, =2
ASR R1, #7
LSR R5, #7
END

A) R1 = 0xfffffffff , R5 = 0x01ffffff
B) R1 = 0xffffffff , R5 = 0x02ffffff
C) R1 = 0xfffffff , R5 = 0x02ffffff
D) R1 = 0xfffffff , R5 = 0x01efffff
```

11. Match the following

| Field Mnemonic | | | Meaning |
|----------------|----|---|------------------|
| А | EQ | Р | Signed ≥ |
| В | VS | Q | Negative |
| С | GT | R | Positive or zero |
| D | PL | S | Equal |
| Е | MI | Т | Overflow |

12. Let A and B be two unknown 8-bit 2's complement numbers. We know the results of A ^ B(A ex-or B) and A & B(A and B) as shown below. Find A + B (sum).

```
A ^ B = 00110100
A & B = 11001001
```

13. Euclid's algorithm for computing the GCD of two positive integers (a,b) can be written as

```
while (a != b) {
    if (a > b)
        a = a - b;
    else
        b = b - a;
}
```

Write an equivalent ARM assembly program using only instructions [B(branch), CMP(compare), SUB(subtraction)]

NOTE: you can use appropriate conditional code after instruction. Let's say two numbers are stored in the register R0, R1.

- 14. Which combination of instructions correctly saves and retrieves register values for a subroutine?
 - A) STMDB SP!, {R0-R12, LR}
 - ; Subroutine instructions
 - LDMIA SP!, {R0-R12, PC}
 - B) STMDA LR, {RO-R12, LR}
 - ; Subroutine instructions
 - LDMFA LR!, {RO-R12, PC}
 - C) STMEA LR!, {R0-R12, SP}
 - ; Subroutine instructions
 - LDMIA LR! , {R0-R12, PC}
 - D) STR SP, {R0-R12, LR}
 - ; Subroutine instructions
 - LDR SP!, {R0-R12, PC}

| 15. | Consider the below subroutine, If initially registe | r R0 has value 7 | , find the value o | n register R0 after |
|------------|-----------------------------------------------------|------------------|--------------------|---------------------|
| | executing the subroutine. | | | |

SUBROUTINE CMP R0, #0

MOVEQ R0, #1

MOVEQ PC, LR

MOV R3, R0

SUB R0, R0, #1

BL SUBROUTINE

MUL R0, R3, R0

MOV PC, LR

- A) 0x13B0
- B) 0x7
- C) 0x0
- D) Code fragment runs into an infinite loop

16. Replace XX in LDM and STM with appropriate suffix from IA, IB, DA and DB such that they execute the corresponding function?

| STMFD | STM{XX} |
|-------|---------|
| LDMFD | LDM{XX} |
| STMEA | STM{XX} |
| LDMEA | LDM{XX} |

17. What will be the content of R0 & SP after execution of program? Assume that the DATA is stored at 0x8000.

| CODE | R0 | SP |
|---------------------------------|----|----|
| LDR R0, =DATA | | |
| LDR SP, =0X4EFC | | |
| LDM R0!, {R2 - R9} | | |
| STM SP, {R7, R2, R6, R8} | | |
| STM SP!, {R9, R3-R5} | | |
| DATA DCD 1, 2, 3, 4, 5, 6, 7, 8 | | |

18. What will be the contents of register R1-R5 and SP after the execution of each instructions? Assume initial values of R1, R2, R3, R4, and R5 are 1, 2, 3, 4, and 5 respectively.

| | SP | R1 | R2 | R3 | R4 | R5 |
|-------------------|----|----|----|----|----|----|
| MOV SP,#0X4000 | | | | | | |
| STMED SP!,{R1-R5} | | | | | | |
| LDMFD SP!,{R1-R5} | | | | | | |
| STMFA SP!,{R1-R5} | | | | | | |
| LDMEA SP!,{R1-R5} | | | | | | |

| 19. | Which register will be stored at which memory location after executing program? What will be the | ne |
|-----|--------------------------------------------------------------------------------------------------|----|
| | value of SP at the end of program? | |

AREA PROGRAM, CODE, READONLY
ENTRY

LDR SP, =0X4000

PUSH {R2}

PUSH {R3}

PUSH {R7}

POP {R8}

POP {R8}

PUSH {R0}

PUSH {R8}

END

| 0X3FF0 | 0X3FF4 | 0X3FF8 | 0X3FFC | 0X4000 | 0X4004 | 0X4008 | 0X400C | 0X4010 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| | | | | | | | | |

20. What is significance of ^ in below instruction?

LDMFD SP!, {RO-R3, PC}^

- 21. The appropriate return addresses are obtained with the help of ______ in case of nested routines.
 - A) MAR
 - B) MDR
 - C) Buffers
 - D) Stack-pointers

| 22. | | ong statement/s regarding interrupts and subroutines among the following is/are | | | | |
|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|--|--|--|--|
| | i) The sub-routine and interrupts have a return statement ii) Both of them alter the content of the PC | | | | | |
| iii) Both are software oriented | | | | | | |
| iv) Both can be initiated by the user | | | | | | |
| | ., 500 | Total Se miliated S7 the aser | | | | |
| | A) i, ii | and iv | | | | |
| | B) ii ai | nd iii | | | | |
| | C) iv | | | | | |
| | D) iii a | nd iv | | | | |
| 23. | What is | the problem with this code? | | | | |
| | | AREA PROGRAM, CODE, READONLY | | | | |
| | CT 4 D T | ENTRY | | | | |
| | START | MOV R0, #1 MOV R1, #3 | | | | |
| | | BL SUB1 | | | | |
| | | ADD R0, R0, R1 | | | | |
| | SUB1 | ADD R0, R0, R1 | | | | |
| | | BL SUB2 | | | | |
| | | BX LR | | | | |
| | SUB2 | ADD R0, R0, R1 | | | | |
| | END | BX LR | | | | |
| | EIND | | | | | |
| 24. | Explain | pre-fetch abort in one sentence. | | | | |
| | | | | | | |
| 25. | Why th | e FIQ vector is the last entry in the vector table. Explain in 1-2 sentences. | | | | |
| _0. | , | | | | | |
| 26. | Which | of the following trigger an interrupt by executing a special operation which is known as a | | | | |
| _5. | system | | | | | |
| | A) Har | | | | | |
| | B) Sof | | | | | |
| | C) Ker | | | | | |
| | D) Noi | | | | | |
| | | | | | | |

| 27. | When the p | ocess is returned after an interrupt service should be loaded again. |
|-----|------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| | I. Regi | ster contents |
| | II. Cond | dition codes |
| | III. Stac | k contents |
| | IV. Retu | rn addresses |
| | A) i,iv | |
| | B) ii,iii and | iv |
| | C) iii,iv | |
| | D) i,ii | |
| | | |
| 28. | | ssembly code and you get error "Undefined Instruction at 80H". At what address code |
| | will jump? | |
| | | |
| | | |
| | | |
| 29. | Will followin | ng code go in infinite loop? Justify. |
| | | |
| | | AREA PROGRAM, CODE, READONLY |
| | | ENTRY |
| | | LDR R1, =0 |
| | | B MAIN |
| | | SWI_MAIN |
| | | STMFD SP!, {R0-R12, LR} |
| | | LDR R10, [LR, #-4] |
| | | |
| | | BIC R10, R10, #0XFF000000 |
| | | BIC R10, R10, #0XFF000000 CMP R10, #01 |
| | | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD |
| | | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 |
| | MAIN | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD |
| | MAIN | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL |
| | MAIN | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL LDR R0, =2 |
| | MAIN | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL LDR R0, =2 LDR R1, =2 |
| | MAIN | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL LDR R0, =2 LDR R1, =2 LDR R2, =2 |
| | | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL LDR R0, =2 LDR R1, =2 LDR R2, =2 SWI 02 |
| | MAIN SWI_ADD SWI_MUL | BIC R10, R10, #0XFF000000 CMP R10, #01 BLEQ SWI_ADD CMP R10, #02 BLEQ SWI_MUL LDR R0, =2 LDR R1, =2 LDR R2, =2 |

30. Execution is in which mode at the end of following code?

AREA PROGRAM, CODE, READONLY ENTRY LDR RO, =0X11 MRS R10, CPSR AND R10, R10, #0XFFFFFFE0 ORR R10, R10, R0 MSR CPSR_C, R0 END