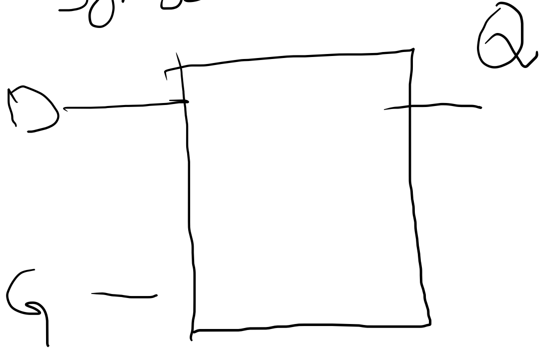
Transparent D Latch :

Symbol.



Q \ GD	00	01	11	10
0				
1				

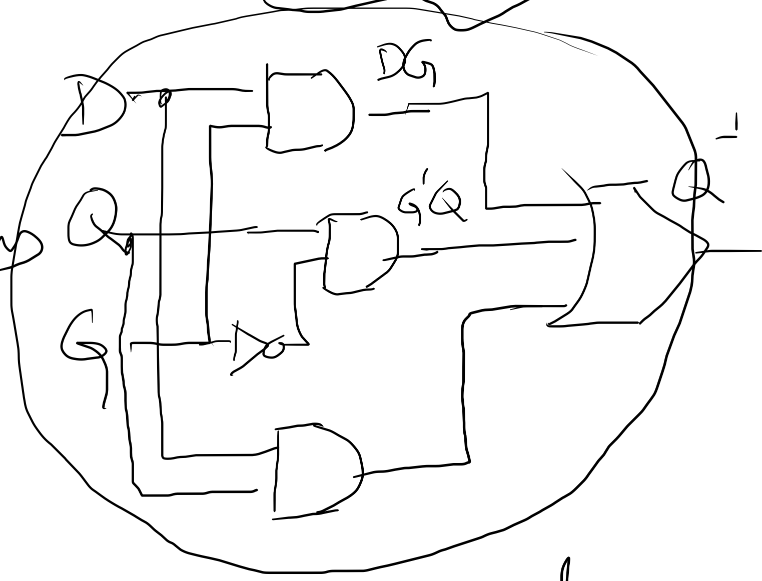
$Q^+ =$

G	D	Q	Q^+(NS)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

follows Q

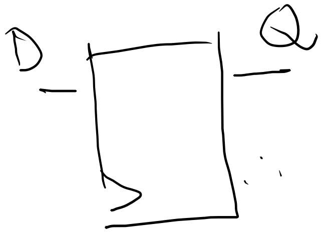
follows D

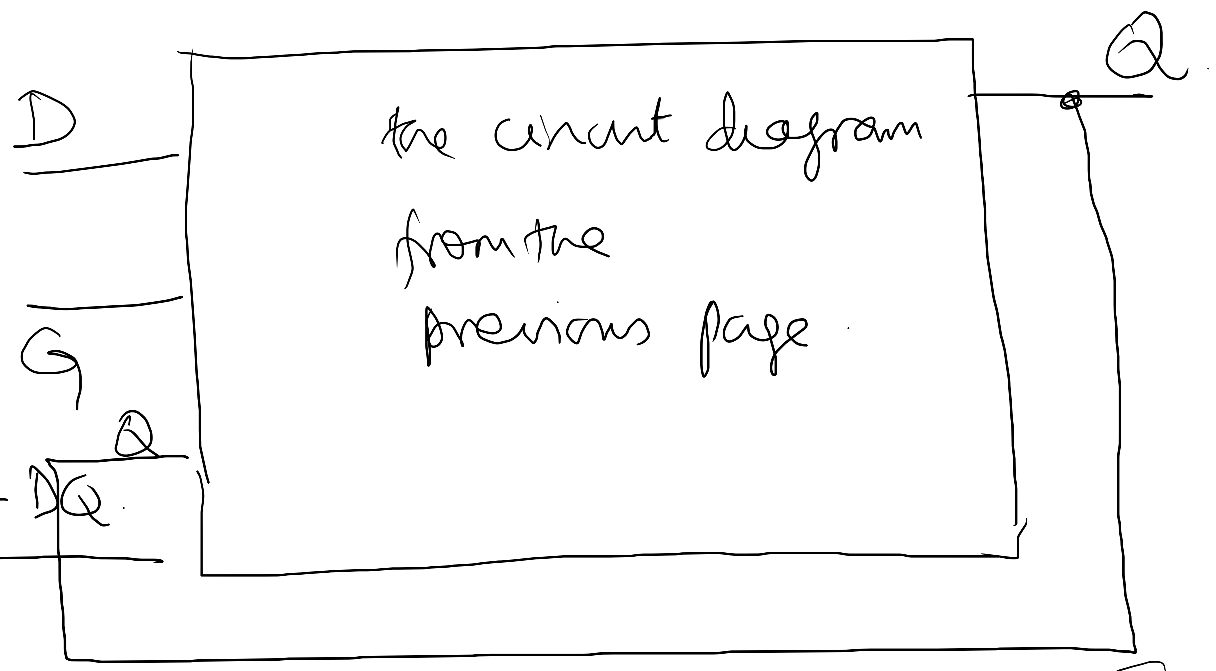
$$Q^+ = DG + G'Q + (DQ)$$



Q^+ Circuit diagram.

In terms of Q (as Q^+ is Next state)
and Q is available from the (D) flipflop output





$Q^+ = \underline{DG + G'Q + DQ}$

Implementation of a
transparent $\underline{\underline{D}}$ latch.

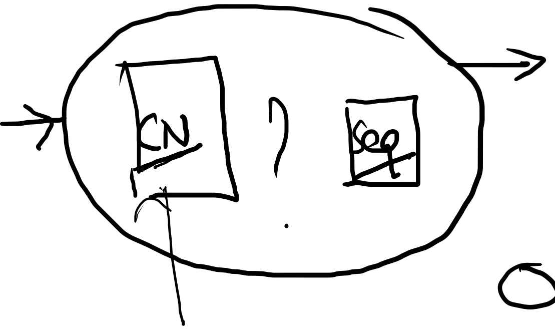
It can ~~have~~ be positive/
or negative transparent latch.

After Δt $\underbrace{Q \rightarrow \boxed{Q^+}}$

Q^+ = Next state
Q = Current State

State Machine :- Synchronons and Asynchronons

X



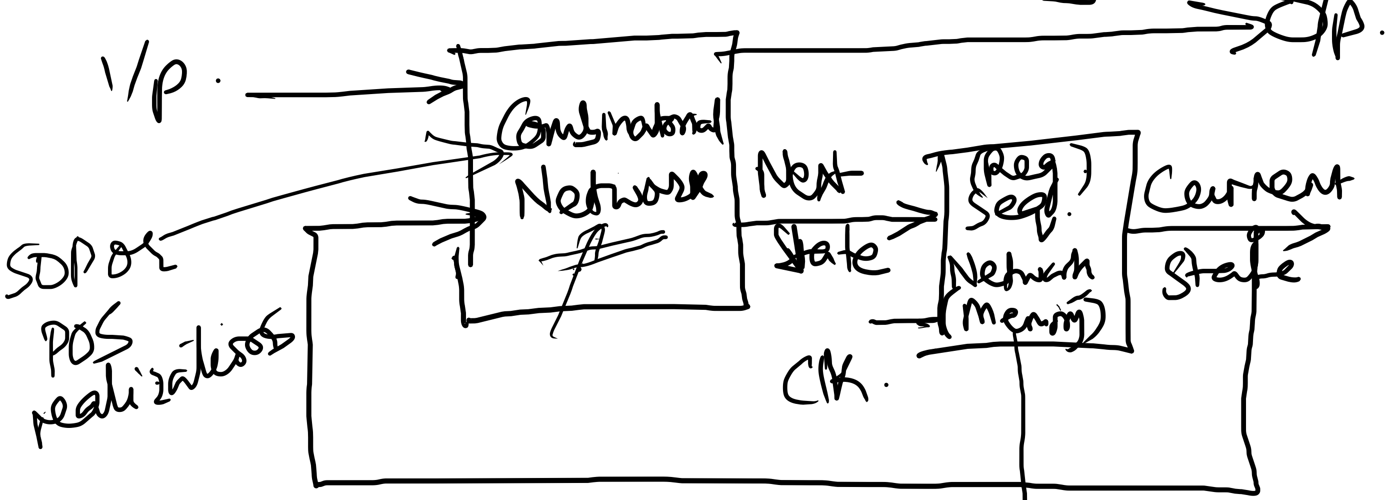
Mealy

Output = f [i/p + CS.]

Moore

Output = f [State]

no i/ps.



D Flip Flop or Register or Memory Element.

Design of a Code Converter:

BCD to Excess 3 (+3)

0 to 9

State Table

Design a Sequential State-Machine

Dec.	X INPUTS (BCD)				Excess 3			
	t3	t2	t1	t0	t3	t2	t1	t0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
	0	0	1	1	0	1	1	0
	0	1	0	0	1	1	1	1
	0	1	0	1	1	0	0	0
	0	1	1	0	1	0	0	1
	0	1	1	1	1	0	1	0
	1	0	0	0	1	0	1	1
	1	0	0	1	1	1	0	0

BCD no
+ 0011

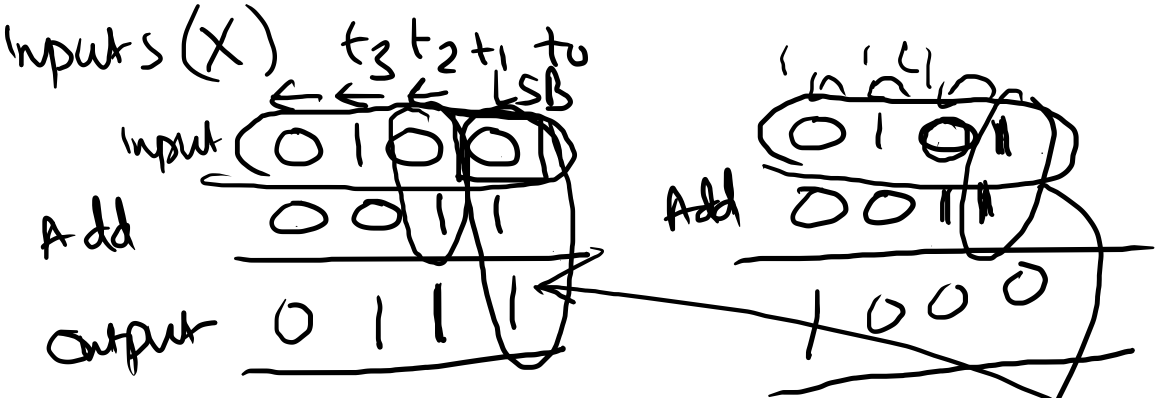
← States

S0 S1 S2 .... Sx.

1. ~~State~~ I/O Table
2. State Graph + State Table.
3. State Assignment
4. State Equations (K-maps)

From the Code Converter input-output table:

X is the input   Excess 3 ($t_3 \cdots t_0$) is the O/P.



Start State / Initial State S∅

First bit arrives: we need to add '1' to this bit ~~0011~~
0011

S∅

At t_0 we add 1 to the LSB:

if $X = 0$ (0+1) Output $Z = 1$ (no carry) ← State S1 (NC State)

$X = 1$ (1+1) output $Z = 0$ (Carry = 1) ← State S2 (Carry State)

At t_1: if there is no carry from first addition (S1)

State S1 . then $\underset{\text{input}}{X} = 0$ gives $Z = \underset{\text{nocarry}}{0} + 1 + 0 = 1$ (S3)

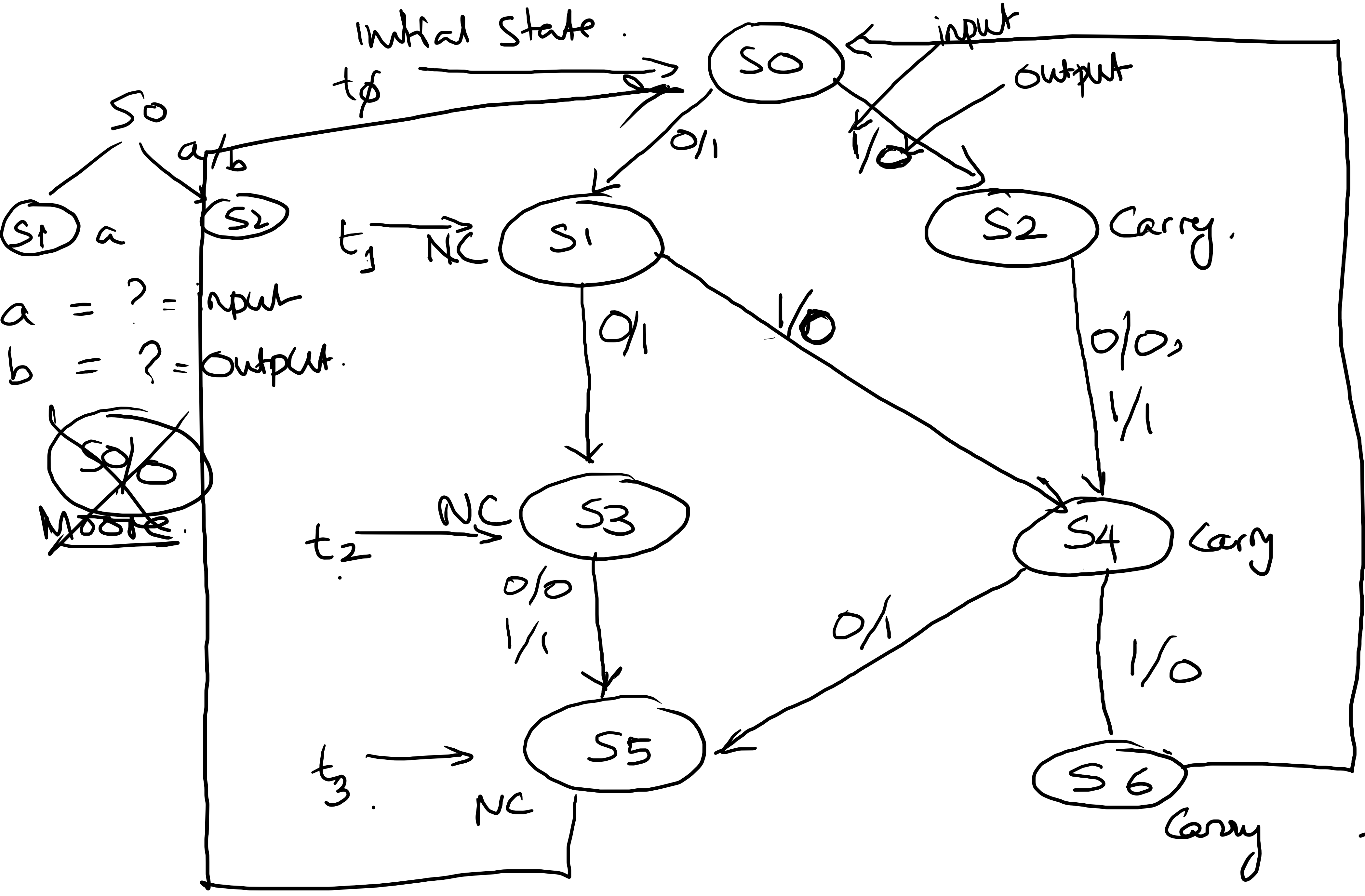
$\underset{\text{input}}{X = 1}$ gives $Z = \underset{\text{Carry}}{1} + \underset{\text{input}}{1} + 0 =$ carry State (S4)

if there is a carry state from first addition (State S2)

S2 then $X = 0$ gives $Z = 0 + 1 + 1 = 0$ carry S4

$X = 1$ gives $Z = 1 + 1 + 1 = 1$ and carry S4.

Similar


Initial State
tϕ
S0
input
output
0/1
1/0
S0
a/b
S1
a
S2
a = ? = input
b = ? = output
~~S0/0~~
~~Moore~~
t1
NC
S1
S2
Carry
0/1
1/0
0/0,
1/1
t2
NC
S3
S4
Carry
0/0
1/1
0/1
1/0
t3
S5
NC
S6
Carry

State Graph

from State diagram/Graph to State Table:

PS	Next State		Z	
	X = 0	X = 1	X = 0	X = 1
S0	S1	S2	1	0
S1	S3	S4	1	0
S2	S4	S4	0	1
S3	S5	S5	0	1
S4	S5	S6	1	0
S5	S0	S0	0	1
S6	S0	–	1	–

7 States

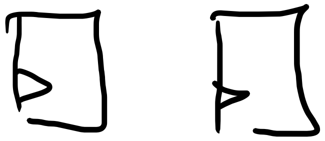
S0

3 ff's

[encode these states as 0 and 1

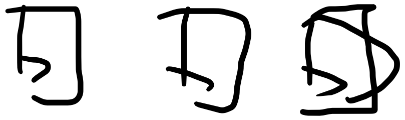
how many FF's if we use One-hot approach. 7

Each Flipflop/Register can save 2 State 0/1



0 0
0 1
1 0
1 1

3 ffs



0 0 0
0 1 1 1 } 8 States

State Graph → State Encoding or
State Assignment .

S0 = 000

S1 = 001

S2

⋮

S6 = 110

Binary Assignment