Chapter 1 Solutions

1.1

A	B	C	$A \oplus B$	$B' \oplus C$	$(A \oplus B) \cdot C$	$A' \cdot (B' \oplus C)$	F
0	0	0	0	1	0	1	1
0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	0	0	0	0
1	1	1	0	1	0	0	0

1.2

X	Y	B_{in}	$Diff$	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Sum of Products: $Diff = XY'B_{in}' + X'Y'B_{in} + XYB_{in} + X'YB_{in}'$

$B_{out} = X'B_{in} + X'Y + YB_{in}$

Product of Sums: $Diff = (X + Y + B_{in})(X + Y' + B_{in}')(X' + Y + B_{in}')(X' + Y' + B_{in})$

$B_{out} = (Y + B_{in})(X' + B_{in})(X' + Y)$

1.3

CD \ AB	00	01	11	10
00	0	X	S	0
01	X	E	E	X
11	1	0	F′	1
10	0	0	F′	0

S = G + H′

Set all map-entered variables to 0 to get MS_0=B'D. Set E, F', G, and H, to 1 one at a time and all 1's to X's to get MS_1=C'D(E), MS_2=ABC(F'), MS_3=BC'D'(G + H)

$Z = B'D + C'DE + ABCF' + BC'D'G + BC'D'H'$

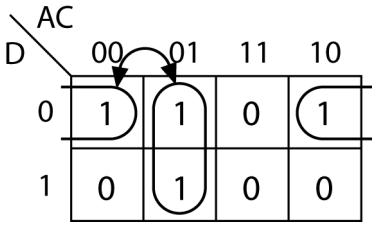
1.4 **(a)** $F = A'D' + AC'D + BCD' + A'B'C'E + BD'E$

(b) $Z = A'CD' + C'D + BC'E + B'DE + CD'F + A'C'G$

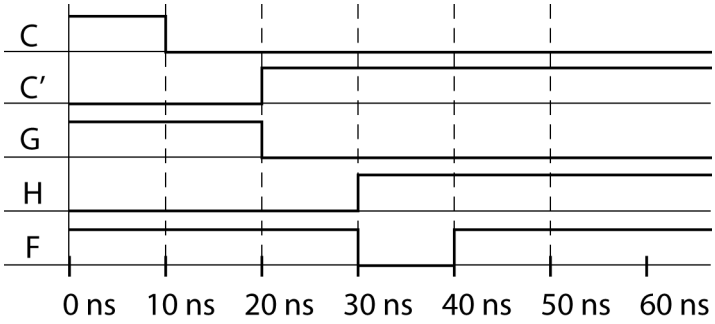
(c) $H = A'CD + A'B'CE + BCDF'$

(d) $G = C'E'F + DEF + AD'F'$

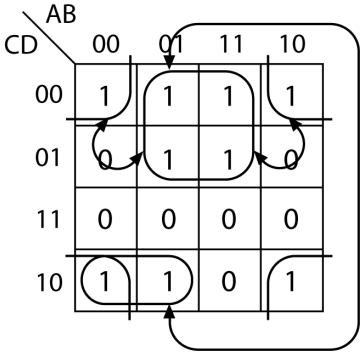
1.5



A static 1-hazard occurs when $A = 0$, $D = 0$, and C changes. When C changes from 1 to 0; $A'C$ also goes from 1 to 0. The hazard occurs because C' hasn't become 1 yet since it has to go through the inverter; therefore, F goes to 0 momentarily before going to 1. Gate delays are assumed to be 10ns in the timing diagram below.



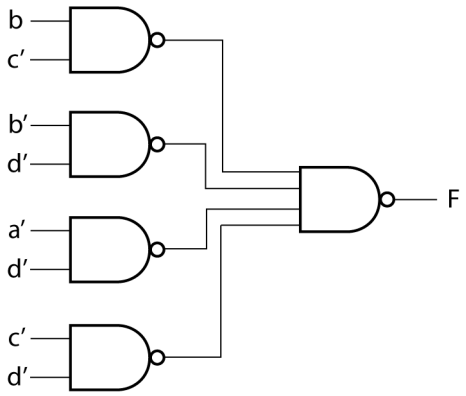
1.6



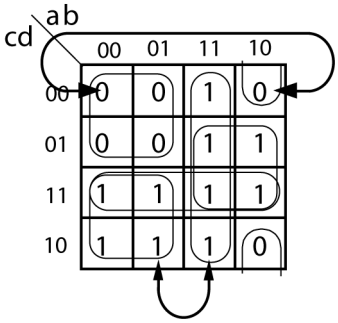
$F = bc' + b'd' + a'cd'$

3 hazards: A=0, C=0, D=0, B changes
A=1, C=0, D=0, B changes
A=0, B=1, D=0, C changes

To eliminate the hazards, add the term $c'd'$ (combining the four 1's in the top row) and replace $a'cd'$ with $a'd'$ (combining two 1's from the bottom left with two 1's from the top left.)



1.7 (a)

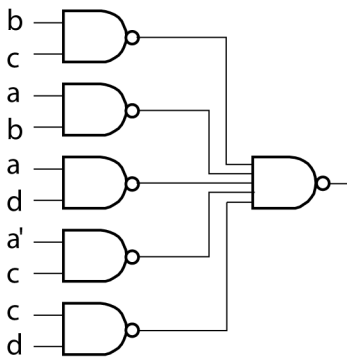


F = *((ab)'.(a+c)'+(a'+d)')'*
= *ab + ((a+c)'+(a'+d)')'*
= *ab* + (*a* + *c*)(*a*' + *d*)
= *ab* + *aa*' + *ad* + *a*'*c* + *cd*;
Circle all these terms on the K-map; arc shows nearby1's not in the same product term, indicating a 1 hazard.
1-hazard *bcd* = 110, a changing 1 => 0 gates 1,5,3,4,5,
0 => 1 gates 3,4,5,1,5

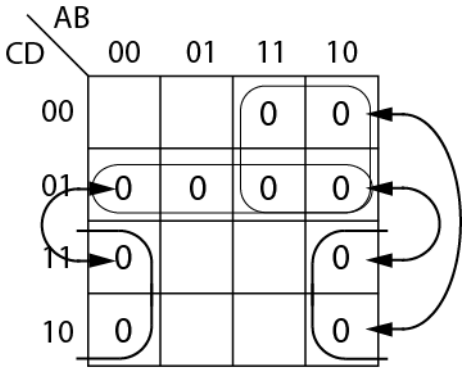
F = *ab* + *aa*' + *ad* + *a*'*c* + *cd*
= *ab* + *a*(*a*' + *d*) + *c*(*a*' + *d*)
= *ab* + (*a*+*c*) (*a*' + *d*)
= (*ab* + *a* +*c*)(*ab* + *a*' +*d*) --see Table 1-1 for Boolean laws
= (*a* + *c*)(*a* + *a*' + *d*)(*a*' + *b* + *d*) -- a+ab=a; a'+d+ab=(a'+d+a)(a'+d+b)
Circle all these terms of 0's in the K-map; arc shows 0's not in same term.

0-hazard *bcd* = 000, a changing 0 => 1 gates 3,4,5,3,5
1 => 0 gates 3,4,5,2,5

(b) We will design a 2-level sum of products circuit because a 2-level sum-of-products circuit has no 0-hazard as long as an input and its complement are not connected to the same AND gate. Avoid 1-hazard by adding product term bc. Use NAND gates as asked in the question.



1.8 (a)



H' = ((*A*'+*C*)(*C*+*D*')(*B*+*C* '))'
= (*A*'+*C*) ' + (*C* '+*D*') ' + (*B*+*C* ')'
= *AC* ' + *C* '*D* + *B*'*C*

H = (A'+C)(C+D')(B+C')

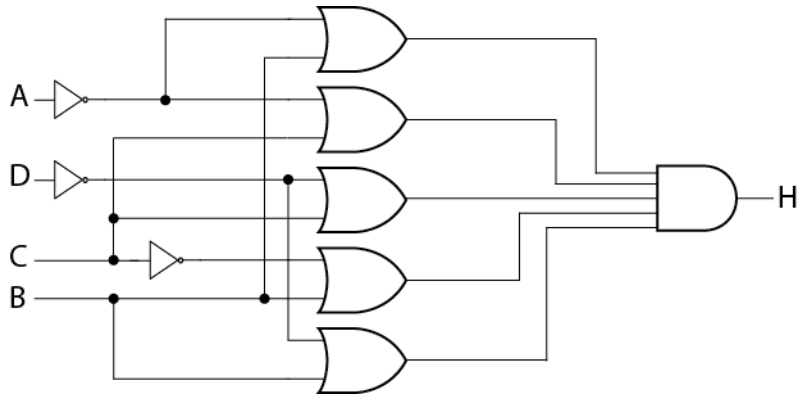
The circuit is in the Product-of-Sums form, and thus we only need to consider the static 0-hazards.

Circle all these terms of 0's in the K-map; arc shows 0's not in same term.

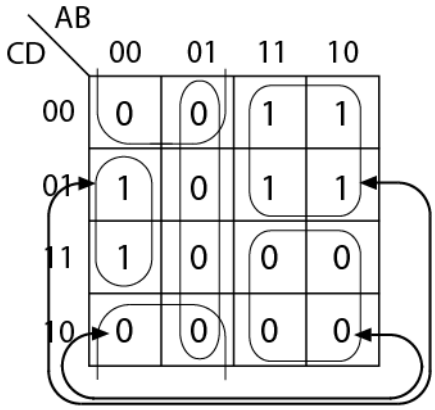
3 hazards:
ABCD = 0001, C changes to 1
ABCD = 1001, C changes to 1
ABCD = 1000, C changes to 1

Adding the terms: (*A*'+*B*)(*B*+*D*') will eliminate the hazards.

(b)



1.9 (a)



f = AC' + A'B'D

Circle all these terms on the K-map; arc shows nearby1's not in the same product term, indicating a 1 hazard.

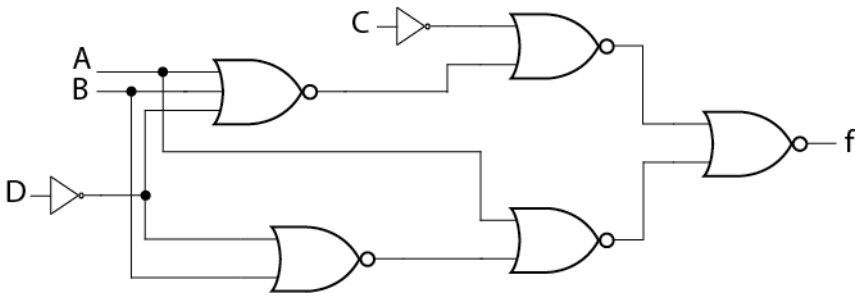
Static 1-hazard:
ABCD = 0001, A changes to 1

f ' = A'B + AC + A'D'
f = (A+B')(A'+C')(A+D)

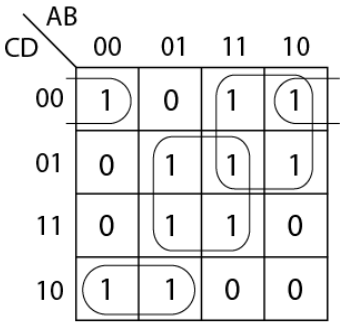
Circle all these terms of 0's in the K-map; arc shows 0's not in same term.

Static 0-hazard:
ABCD = 0010, A changes to 1

(b)

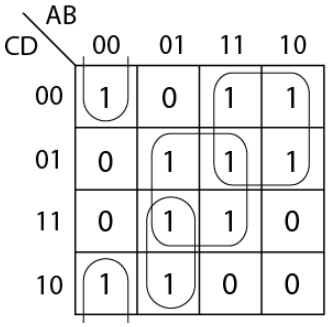


1.10 **(a)** Any two of the three solutions will suffice.



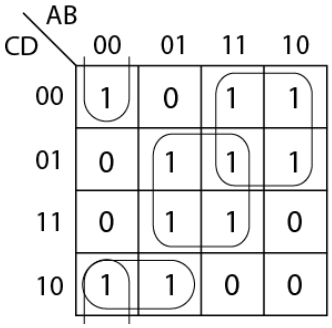
F = AC' + BD + A'CD' + B'C'D'

Static 1-hazard:
Between ABCD = 0000 and 0010
Between 0110 and 0111



F = AC' + BD + A'BC + A'B'D'

Static 1-hazard:
Between ABCD = 0000 and 1000
Between 0010 and 0110

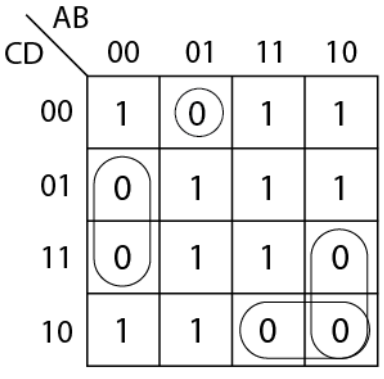


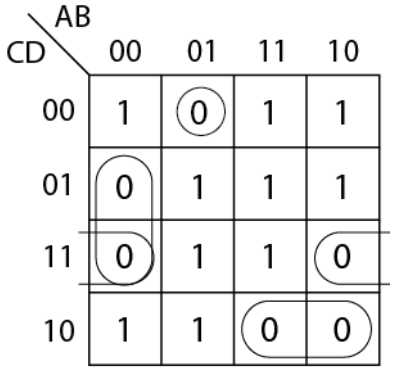
F = AC' + BD + A'B'D' + A'CD'

Static 1-hazard:
Between ABCD = 0000 and 1000
Between 0110 and 0111

Hazard free circuit:
F = AC' + BD + A'BC + A'B'D' + A'CD' + B'C'D'

(b)





F = (A+B'+C+D)(A+B+D')(A'+B+C')(A'+C'+D)

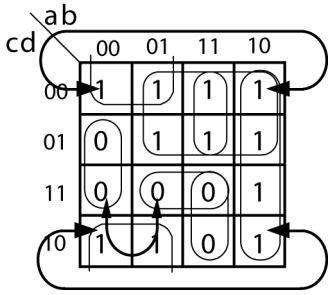
Static 0-hazard:
Between ABCD = 0011 and 1011

F = (A+B'+C+D)(A+B+D')(B+C'+D')(A'+C'+D)

Static 0-hazard:
Between ABCD = 1010 and 1011

Hazard free circuit:
F = (A+B'+C+D)(A+B+D')(A'+B+C')(A'+C'+D) (B+C'+D')

1.11

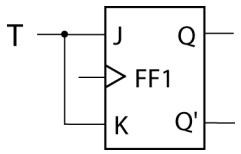


(a) $Z = A'D' + (A + B)(B' + C')$
$= A'D' + AB' + AC' + BB' + BC'$
Static 1 hazard (see the arcs between nearby 1's not in the same product term.)
$ABCD$ = 0000 to 1000
$ABCD$ = 0010 to 1010

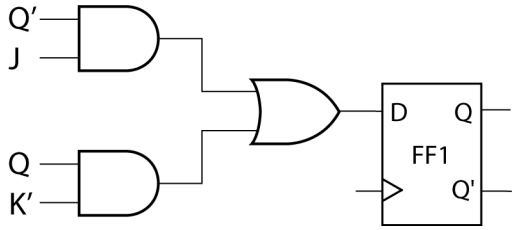
$Z = (A'D' + A + B)(A'D' + B' + C')$
$= (A' + A + B)(D' + A + B)(A' + B' + C')(D' + B' + C')$
Static 0 hazard (see the arcs between nearby 0's not in the same term)
$ABCD$ = 0111 to 0011

(b) One can design a hazard-free sum of products circuit as in the previous question. Or, one can design a product of sums (POS) circuit with no hazards. A properly designed 2-level POS circuit has no 1-hazards. Static 0-hazards can be avoided by including loops for all 0's that are adjacent. 4 terms here including the arc:
$Z = (A + B + D')(A' + B' + C')(D' + B' + C')(C' + D' + A)$
$= (D' + A + BC')(A' + B' + C')(D' + B' + C')$ combining 1st and 4th terms
$= (D' + A + BC')(B' + C' + A'D')$ combining 2nd and 3rd terms

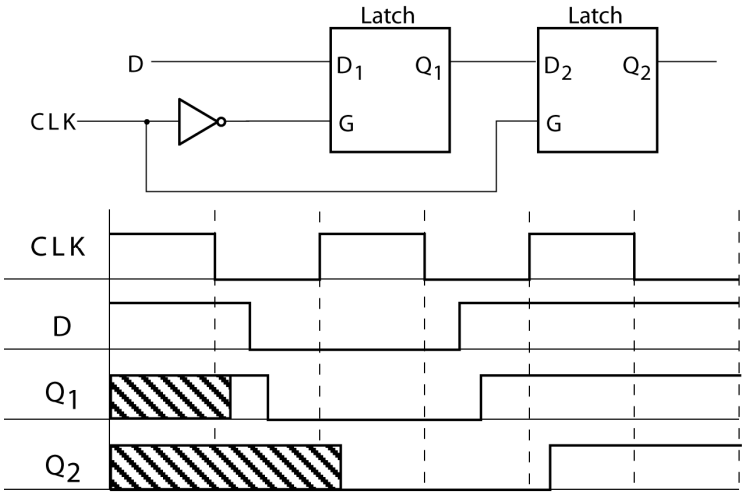
1.12 (a)



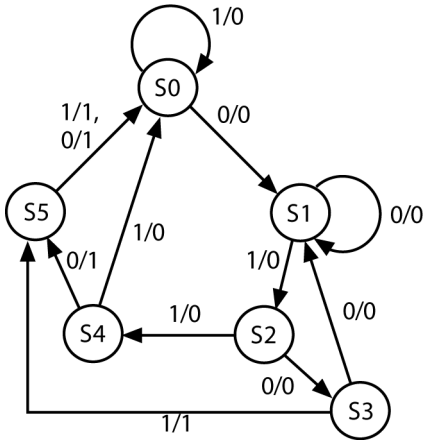
(b) From the characteristic equation for a J-K flip-flop ($Q^+ = JQ' + K'Q$):



1.13



1.14 (a)



Present State		Next State $X=0$	Next State 1	Output $X=0$	Output 1
Reset	S0	S1	S0	0	0
0	S1	S1	S2	0	0
01	S2	S3	S4	0	0
010	S3	S1	S5	0	1
011	S4	S5	S0	1	0
0101 or 0110	S5	S0	S0	1	1

(b) Guidelines:

I. (0,1,3),(0,4,5)
II. (0,1),(1,2),(3,4),(1,5),(0,5)
III. (0,1,2,3),(4,5),(3,5)

For state assignment:

S0 = 000 S1 = 001 S2 = 010 S3 = 011 S4 = 100 S5 = 101

Equations for NAND gate network:

$J_1 = XQ_2$ $K_1 = X + Q_3$

$J_2 = XQ_1'Q_3$ $K_2 = X + Q_3$

$J_3 = X'$ $K_3 = XQ_2' + Q_1$

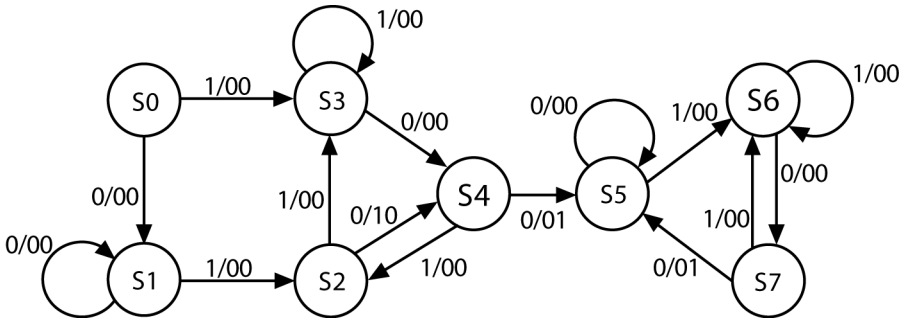
$Z = XQ_2Q_3 + X'Q_1 + Q_1Q_3$

For NOR gate network, use product of sums form:

$K_3 = (X + Q_1)(Q_2')$

$Z = (Q_1 + Q_2)(X' + Q_3)(X + Q_2')$

1.15 (a)



Present State	Next State $X = 0$	Next State 1	Output $X = 0$	Output 1
S0	S1	S3	00	00
S1	S1	S2	00	00
S2	S4	S3	10	00
S3	S4	S3	00	00
S4	S5	S2	01	00
S5	S5	S6	00	00
S6	S7	S6	00	00
S7	S5	S6	01	00

(b) Guidelines:

I. (0,1),(2,3),(4,5,7),(0,2,3),(1,4),(5,6,7)
II. (1,3),(1,2),2x(3,4),(2,5),2x(5,6),(6,7)
III. (0,1,3,5,6),(4,7)

For state assignment:

S0 = 000 S1 = 100 S2 = 001 S3 = 101
S4 = 111 S5 = 011 S6 = 010 S7 = 110

Equations for NAND gate network:

$J_1 = Q_2' + X'Q_3'$ $K_1 = XQ_3' + Q_2$

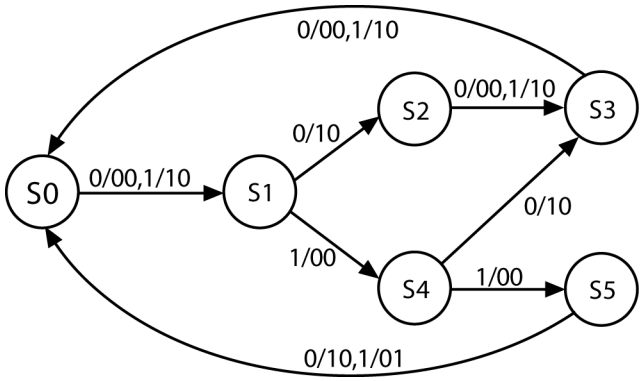
$J_2 = X'Q_3$ $K_2 = XQ_1Q_3$

$J_3 = XQ_2' + X'Q_1Q_2$ $K_3 = XQ_1'Q_2$

$Z_1 = X'Q_1'Q_2'Q_3$
$Z_2 = X'Q_1Q_2$

For NOR gate network, use product of sums form:
$J_1 = (Q_2' + Q_3')(X' + Q_2')$ $K_1 = (X + Q_2)(Q_2 + Q_3')$
$J_3 = (X + Q_2)(X' + Q_2')(X + Q_1)$

1.16 (a)



Present State	Next State X = 0	Next State 1	Output X = 0	Output 1
S0	S1	S1	00	10
S1	S2	S4	10	00
S2	S3	S3	00	10
S3	S0	S0	00	10
S4	S3	S5	10	00
S5	S0	S0	10	01

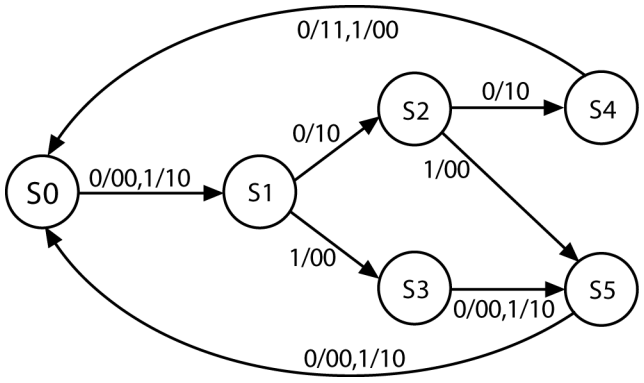
(b) Guidelines:
I. (2,4),2x(3,5)
II. (2,4),(3,5)
III. (0,2,3),(1,4,5)

For state assignment:
S0 = 000 S1 = 010 S2 = 001 S3 = 101 S4 = 011 S5 = 111

Equations for NAND gate network:
$D_1 = Q_1'Q_3$
$D_2 = Q_2'Q_3' + XQ_1'Q_2$
$D_3 = Q_1'Q_3 + Q_2Q_3'$ or $Q_1'Q_3 + Q_1'Q_2$
$S = XQ_2' + X'Q_2$
$V = XQ_1Q_2$

For NOR gate network, use product of sums form:
$S = (X + Q_2)(X' + Q_2')$
$D_2 = Q_1'(Q_2 + Q_3')(X + Q_2')$
$D_3 = Q_1'(Q_2 + Q_3)$

1.17 (a)



Present State	Next State X = 0	1	Output X = 0	1
S0	S1	S1	00	10
S1	S2	S3	10	00
S2	S4	S5	10	00
S3	S5	S5	00	10
S4	S0	S0	11	00
S5	S0	S0	00	10

(b) Guidelines:
I. (4,5),(2,3)
II. (2,3),(4,5)
III. (0,3,5),(1,2,4)

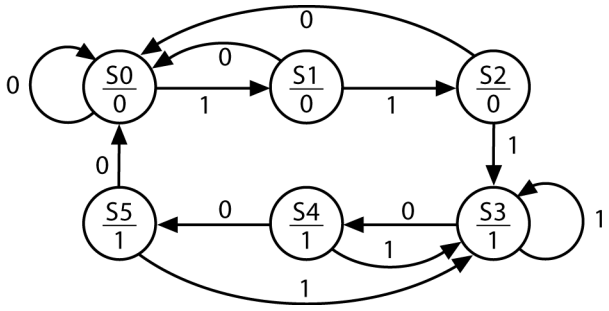
For state assignment:
S0 = 000 S1 = 100 S2 = 101 S3 = 001 S4 = 111 S5 = 011

Equations for NAND gate network:

$J_1 = Q_3'$ $K_1 = X + Q_2$
$J_2 = Q_3$ $K_2 = 1$
$J_3 = Q_1$ $K_3 = Q_2$
$D = X'Q_1 + XQ_1'Q_3$
$B = X'Q_1Q_2$

For NOR gate network, use product of sums form:
$D = (X' + Q_1')(X + Q_1)(Q_1 + Q_3)$

1.18



Present State	Next State X = 0	1	Output
S0	S0	S1	0
S1	S0	S2	0
S2	S0	S3	0
S3	S4	S3	1
S4	S5	S3	1
S5	S0	S3	1

1.19

Present State ($Q_2Q_1Q_0$)	Next State ($Q_2^+Q_1^+Q_0^+$)
000	001
001	010
010	011
011	100
100	101
101	000

$J_2 = Q_1Q_0$ $K_2 = Q_0$
$J_1 = Q_2'Q_0$ $K_1 = Q_0$
$J_0 = 1$ $K_0 = 1$

1.20

Present State ($Q_2Q_1Q_0$)	Next State ($Q_2^+Q_1^+Q_0^+$)
001	010
010	011
011	100
100	101
101	110
110	001

$D_2 = Q_1Q_0 + Q_2Q_1'$
$D_1 = Q_2'Q_0' + Q_1'Q_0$
$D_0 = Q_0'$

1.21

Present State ($Q_2Q_1Q_0$)	Next State ($Q_2^+Q_1^+Q_0^+$)
000	001
001	010
010	011
011	100
100	101
101	110
110	000

$J_2 = Q_1Q_0$ $K_2 = Q_1$
$J_1 = Q_0$ $K_1 = Q_2 + Q_0$
$J_0 = Q_2' + Q_1'$ $K_0 = 1$

1.22

Present State ($Q_2Q_1Q_0$)	Next State ($Q_2^+Q_1^+Q_0^+$)
001	010
010	011
011	100
100	101
101	110
110	111
111	001

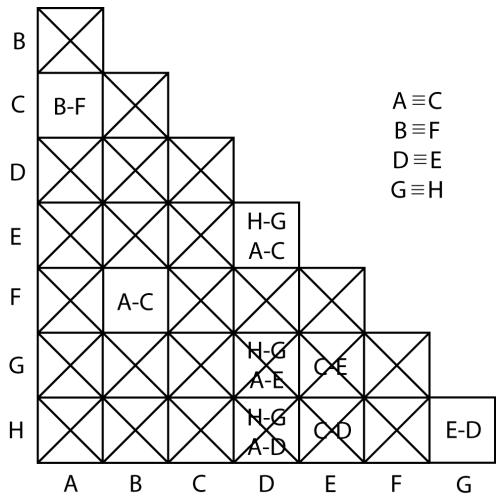
$D_2 = Q_2'Q_1Q_0 + Q_2Q_1' + Q_2Q_0'$
$D_1 = Q_1Q_0' + Q_1'Q_0$
$D_0 = Q_2Q_1 + Q_0'$

1.23

Present State ($Q_2Q_1Q_0$)	Next State ($Q_2^+Q_1^+Q_0^+$)
000	001
001	011
010	XXX
011	101
100	XXX
101	111
110	XXX
111	000

$D_2 = Q_2'Q_1 + Q_2Q_1'$
$D_1 = Q_1'Q_0$
$D_0 = Q_2' + Q_1'$

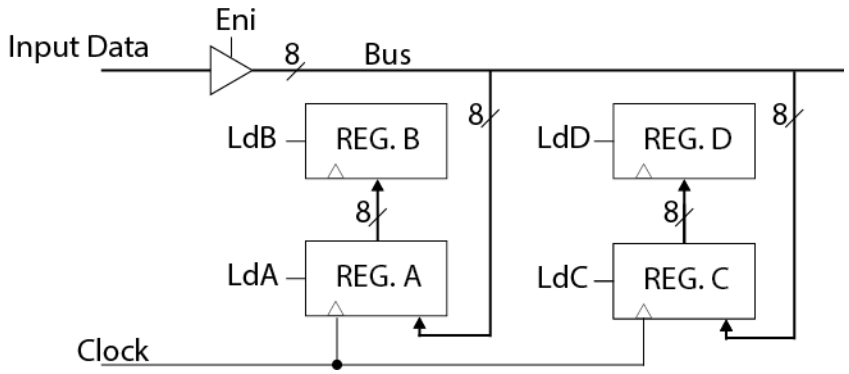
1.24



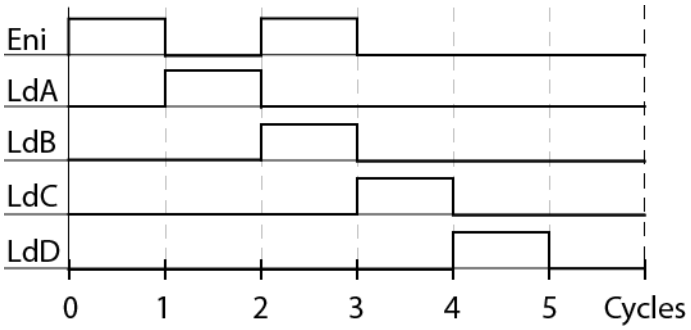
present state	next state $X=0$	next state $X=1$	output $X=0$	output $X=1$
A	B	G	0	1
B	A	D	1	1
~~C~~	~~F~~	~~G~~	~~0~~	~~1~~
D	~~H~~ G	A	0	0
~~E~~	~~G~~	~~C~~	~~0~~	~~0~~
~~F~~	~~C~~	~~D~~	~~1~~	~~1~~
G	G	~~E~~ D	0	0
~~H~~	~~G~~	~~D~~	~~0~~	~~0~~

1.25 *Eni* = 0 *Ena*= 0 *Enb* = 0 *Enc* = 1 *Lda* = 1 *Ldb*= 1 *Ldc*= 0

1.26

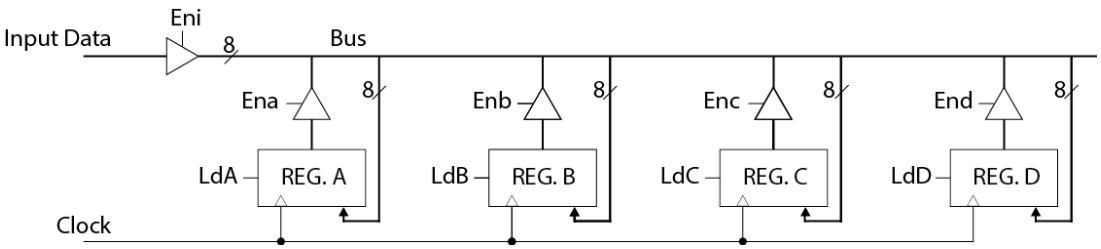


The circuit requires one tri-state gate.

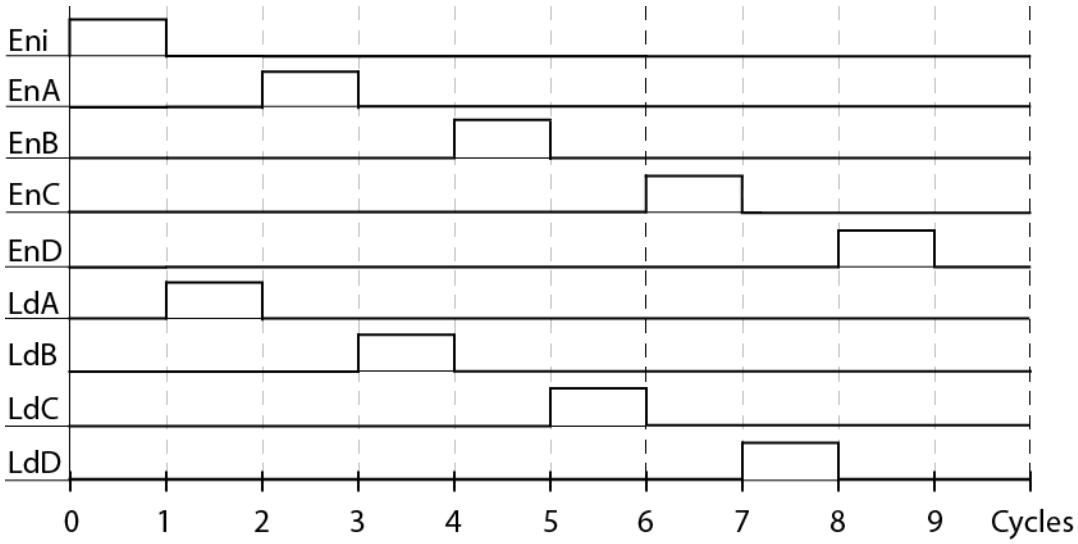


Minimum of 5 cycles for the transfer.

1.27



The circuit requires five tri-state gates.



Minimum of 10 cycles for the transfer.