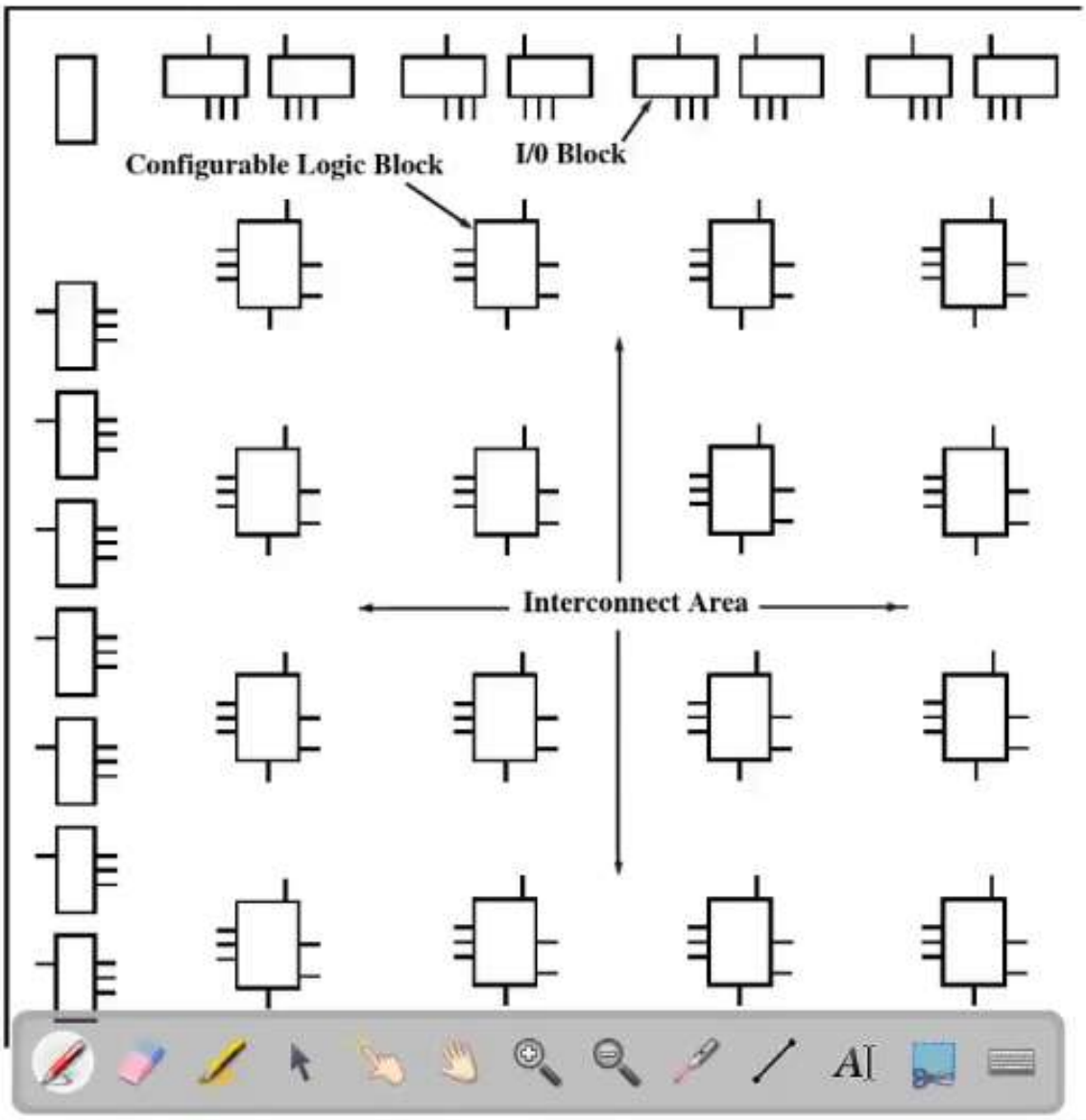
Figure 6-1 Layout of Part of a Programmable Logic Cell Array



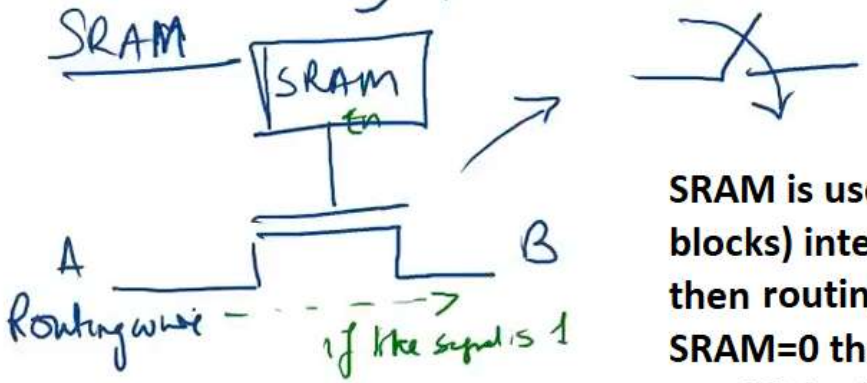
FPGA

Xilinx, Altera, Lattice, Actel, Quick logic, Atmel.

- Matrix based
- Row based
- Hierarchical PLD based
- Sea of Gates. State of the ART

fundamental technology of FPGA is

SRAM



SRAM is used in CLBs (Configurable Logic blocks) interconnection and if SRAM = 1 then routing in CLBs is on and if SRAM=0 then routing is not established.

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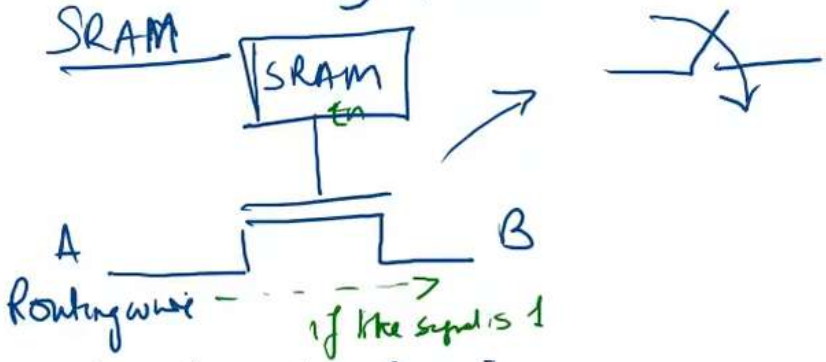
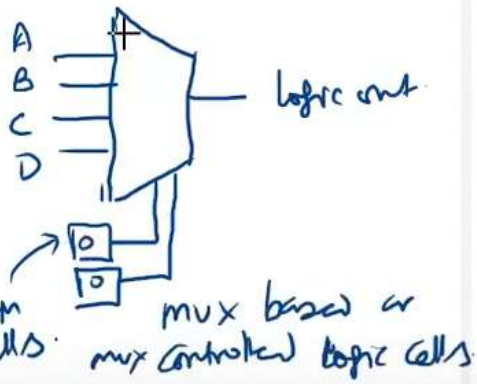
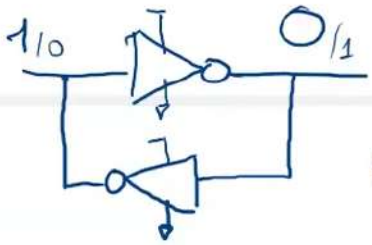
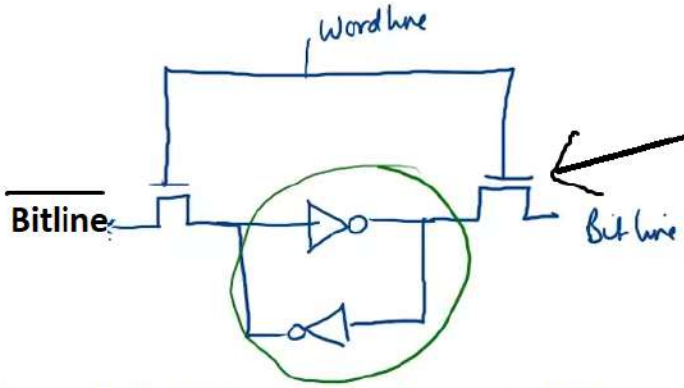






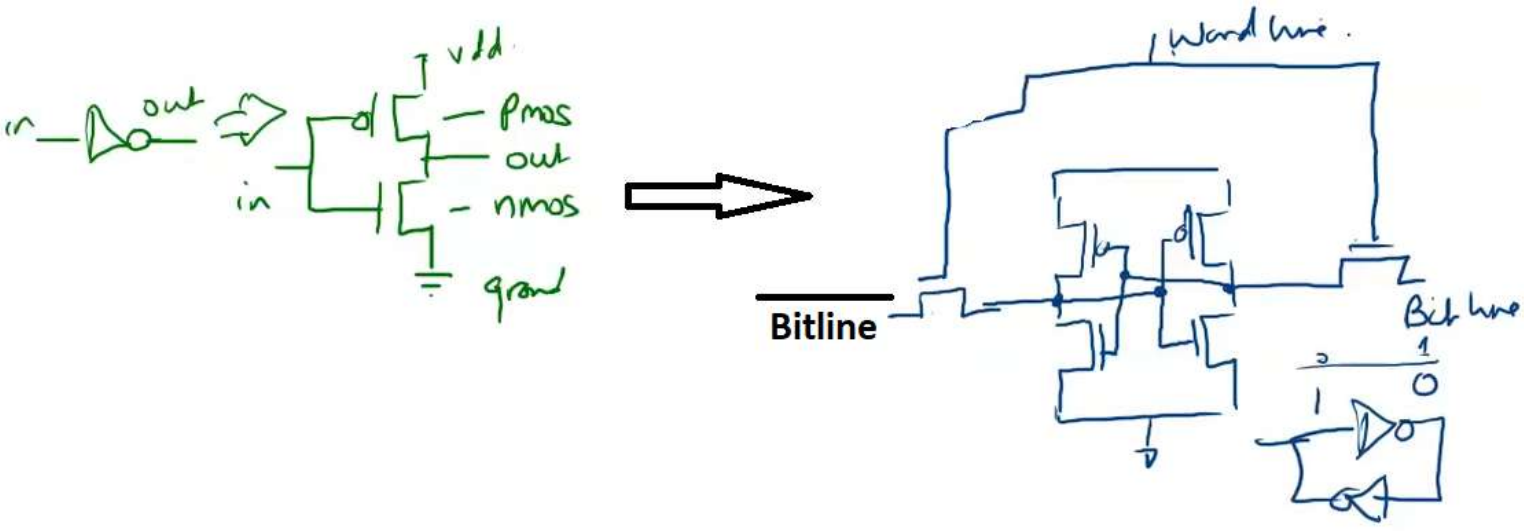
Basic SRAM cell.

SO this ckt doesn't change its o/p i.e., if i/p =1 then o/p=0 and if i/p=0 then o/p=1. This is called Basic SRAM. Then where is the i/p port?



Six 1xtor SRAM cell.

The variant of this ckt is in the next slide.



Basically there two types of operation:
1)write
2)read

For Write Operation: Ward line is set, then load the value on the bit line
For Read Operation: Precharge the bitline and bitline_bar, then set the ward line high and then contents(state) will apper on bitline

19-12-2020

EL Notes (After Midsem)

⊙ FPGA (Feild Programmable Gate Arrays)

⟹ 3 major programmable elements in FPGA:
(1) Logic block (2) Interconnect (3) i/p - o/p block

⟹ 4 different architecture of FPGA:
(1) Matrix-based (symmetrical array) architectures:
- These architecture typically contains 8×8 arrays in the smaller chips & 100×100 or larger arrays in the bigger chips
- routing in this architecture is often called 2D channel routing.

(2) Row based architecture:
- routing in this architecture is often called 1D channel routing

(3) Hierarchical Architecture:
- These FPGAs containt clusters of logic blocks with localized resources for interconnection. The global interconnection network is used for the interconnections between the clusters of logic blocks in these FPGAs.

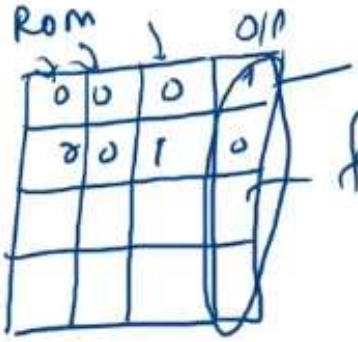
(4) Sea-of Gates Architecture:
- These FPGA consists of a large #gates and then there is interconnect superimposed on the see of gates.

⟹ 3 Programming Technologies of FPGA:
(1.) Static RAM (SRAM)
(2.) EPROM / EEPROM / flash
(3.) Antifuse
} Programming Technology

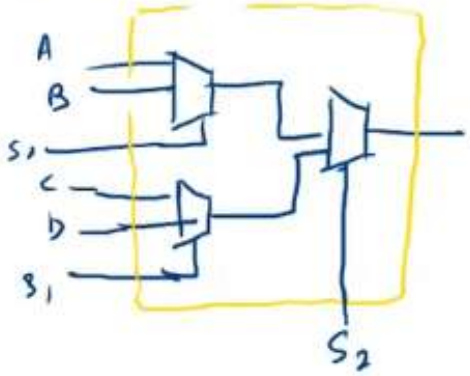
→ founded by Xilinx, Altera
→ founded by Actel, Quicklogic

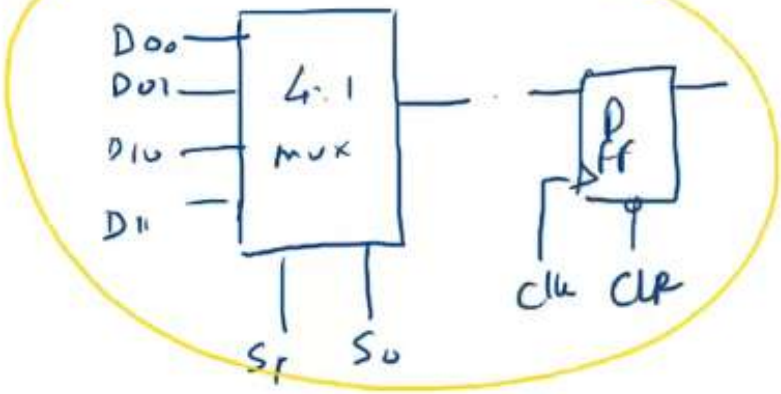
CLB – Configurable Logic Blocks

LUT – Logic Blocks can be made from LUT.



Logic Blocks based on multiplexers + and Gates:





SRAM

(i) using extra space

(ii) not violating the rule of FPGA that is device is programmable.

(iii) High delay

Antifuse

(i) using less area than SRAM

(ii) violatinge Rule of FPGA

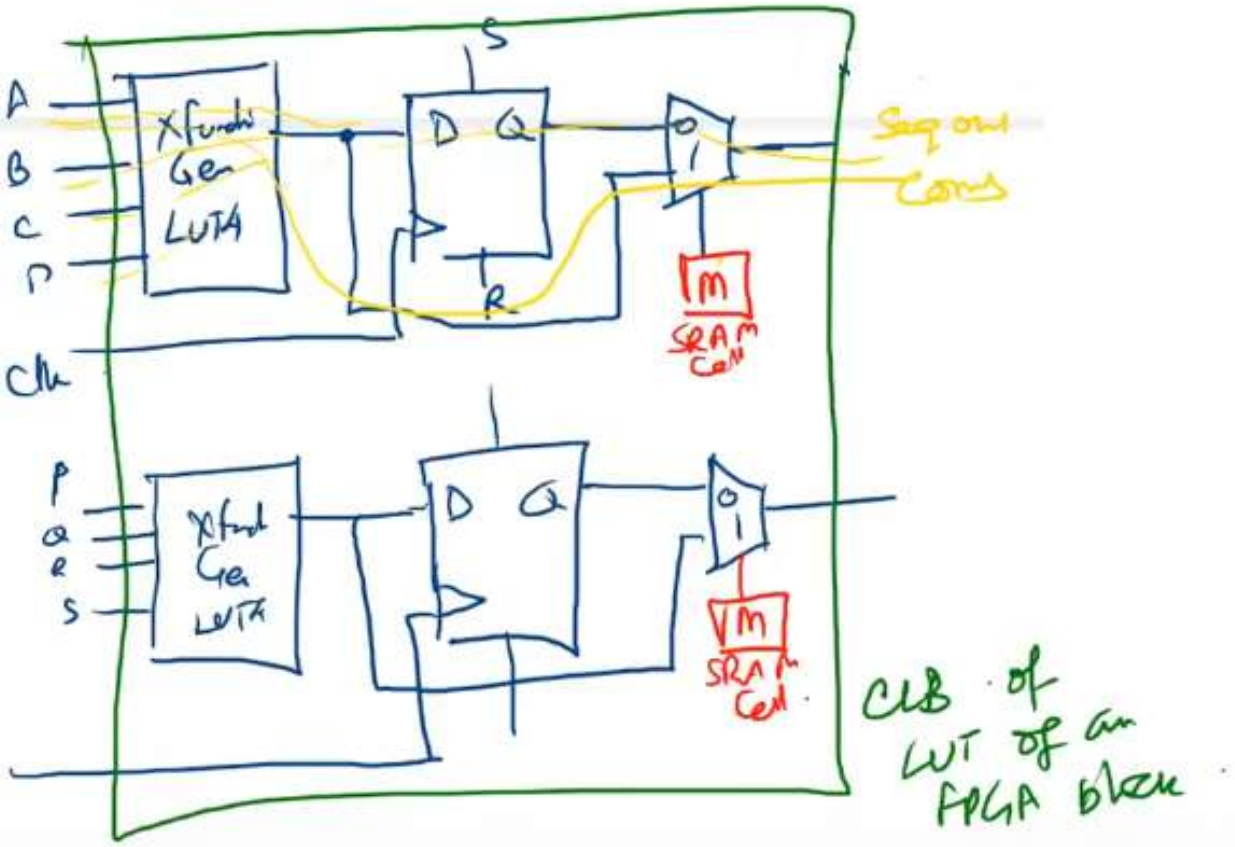
(iii) High speed

ex. used in synchronization

Programming Tech	Volatility	Program-mability	Area Overhead	Resistance	Capacitance
SRAM	Volatile	in-ckt reprogrammable	Large	Medium to high	high
EEPROM	Non-volatile	"	Medium to high	High	High
EPROM	"	out-of-ckt reprogrammable	small	"	"
Antifuse	"	Not reprogrammable	"	small	small

- Programmable Logic block (PLB) =
  Configurable logic block (CLB) =
  Logic Elements (LE) =
  Logic Array Blocks (LABs)

LUT = Lookup table



CLB of LUT of an FPGA block

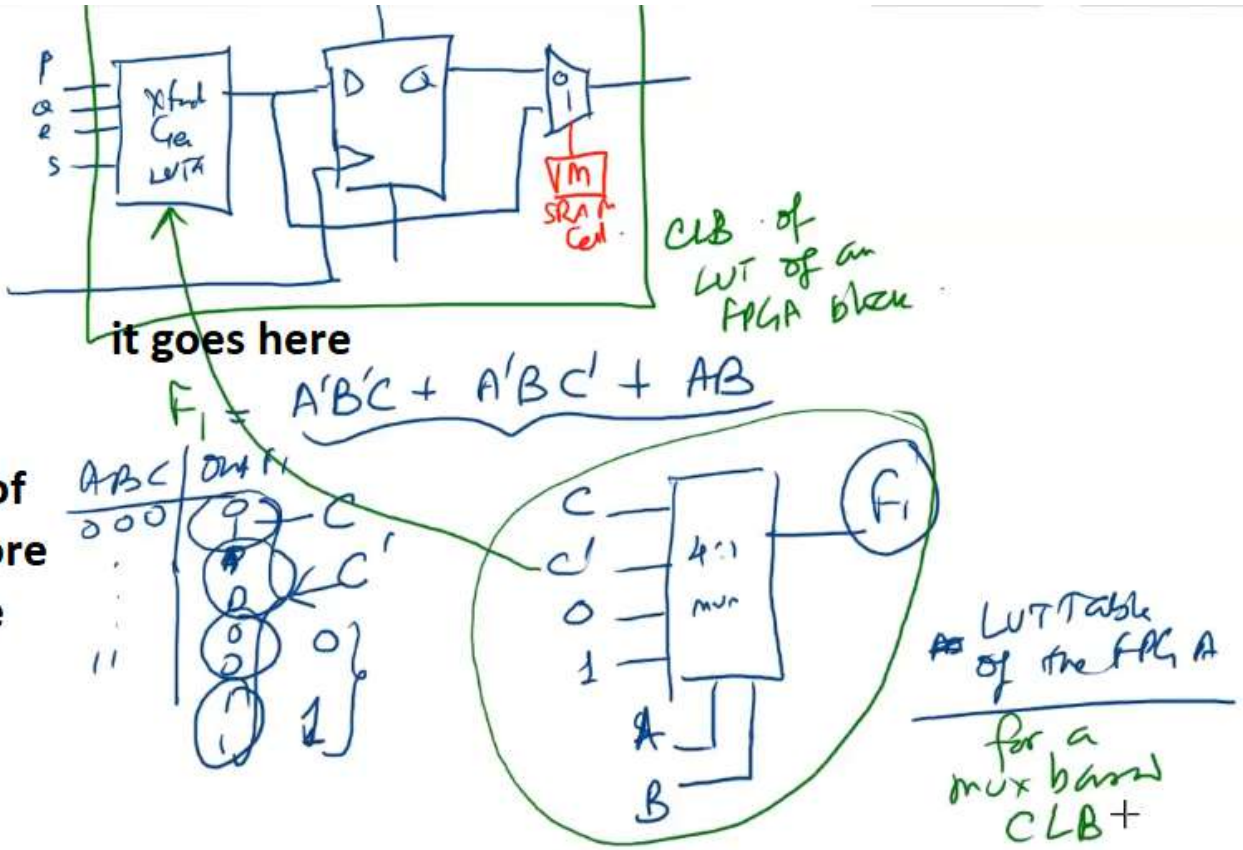

CLB of LUT of an FPGA block
it goes here
$F_1 = A'B'C + A'BC' + AB$
Ex. of before slide
ABC
C
C'
4:1 mux
A
B
F_1
LUT Table of the FPGA for a mux based CLB+

Figure 6-2 Configuration Memory Cell

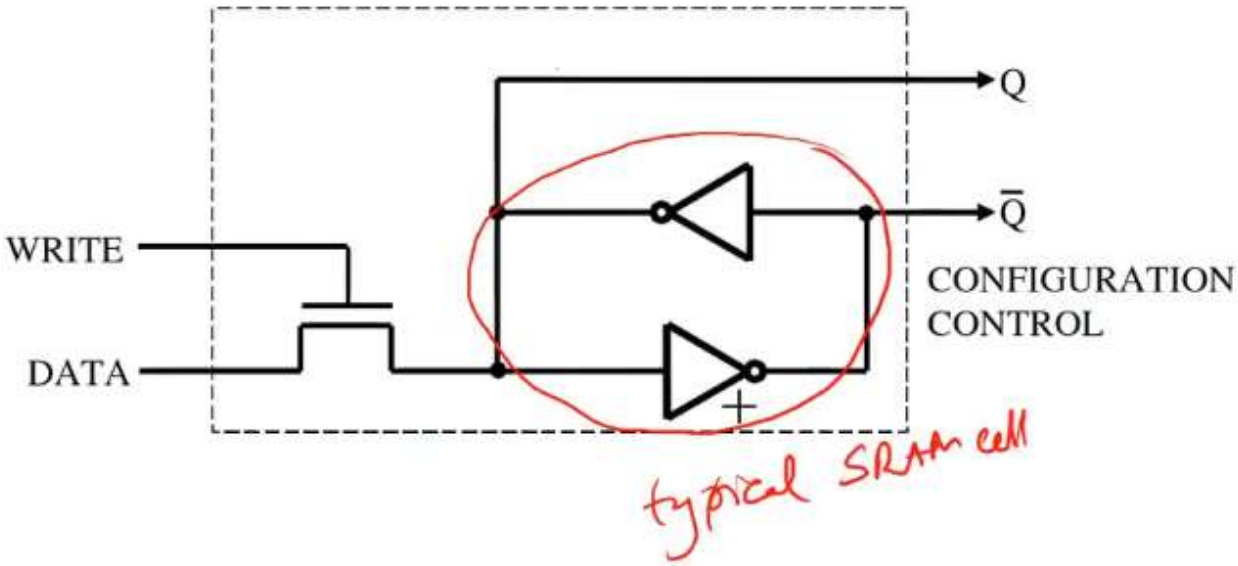


Figure 6-3 Xilinx 3000 Series Logic Cell