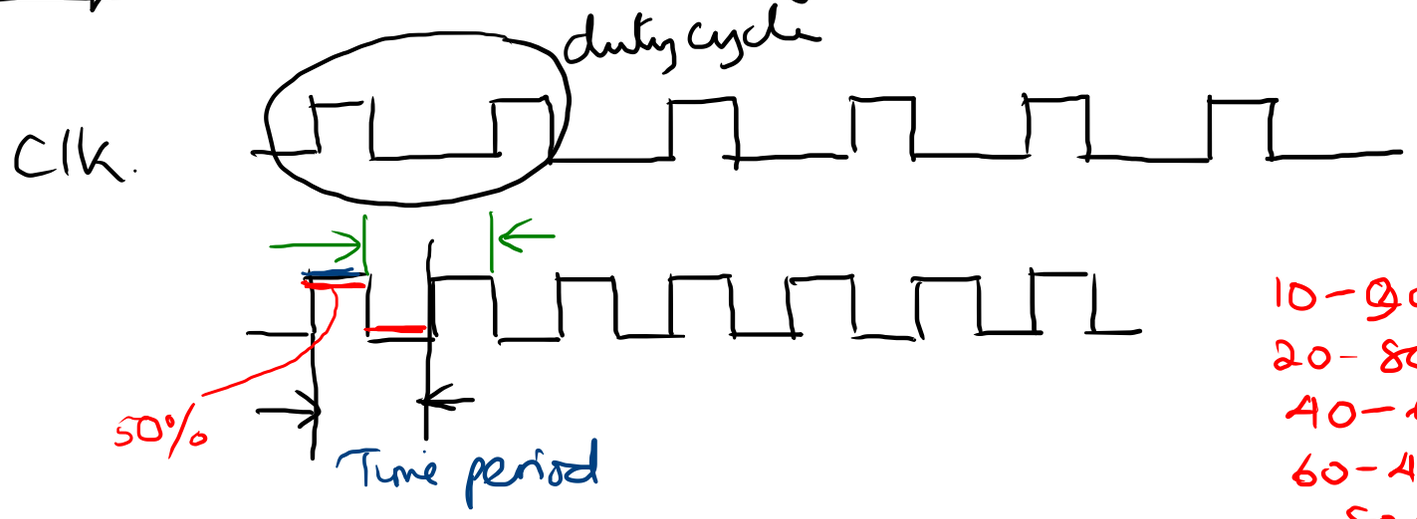
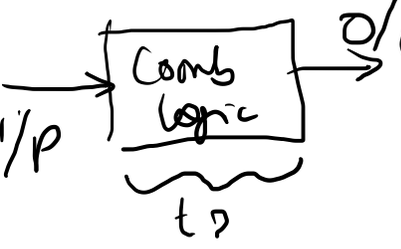
Sequential Circuit Timing :

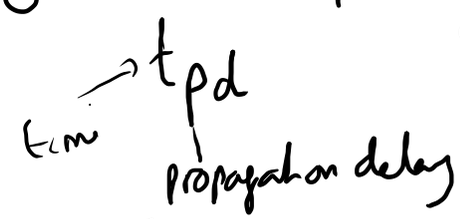


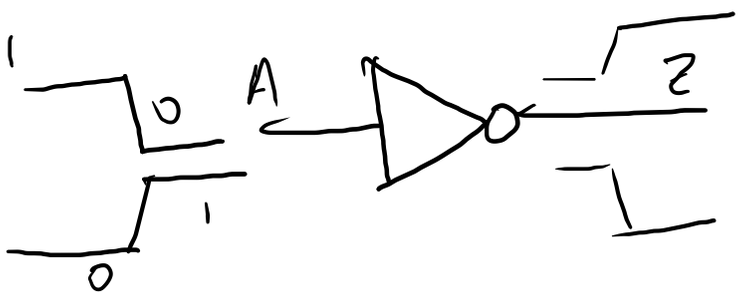
10-90
20-80
40-60
60-40
so on. -

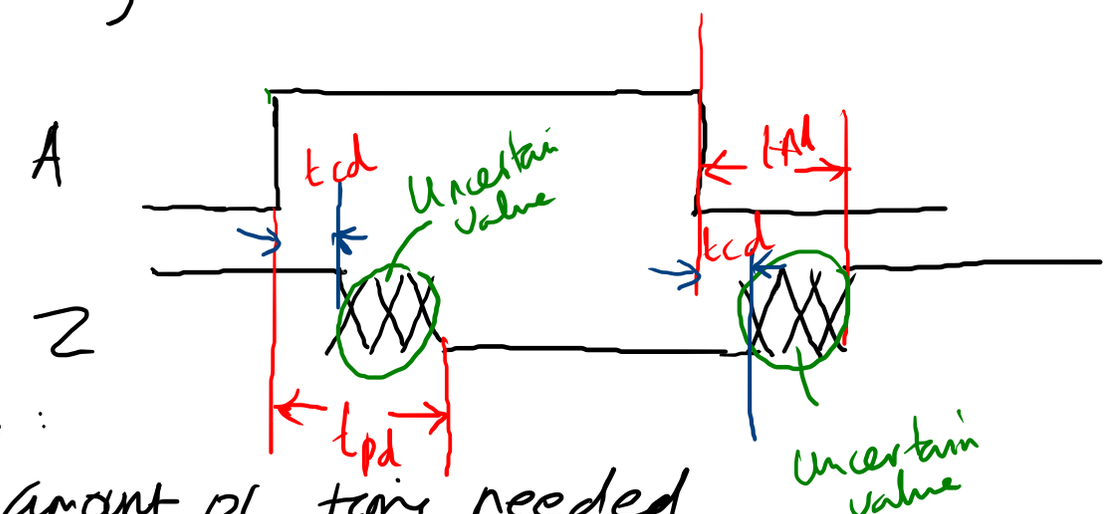
Timing parameters of the combinational logic :



propagation delay : Indicates the time needed for a change in an input to result in a permanent change at the output.

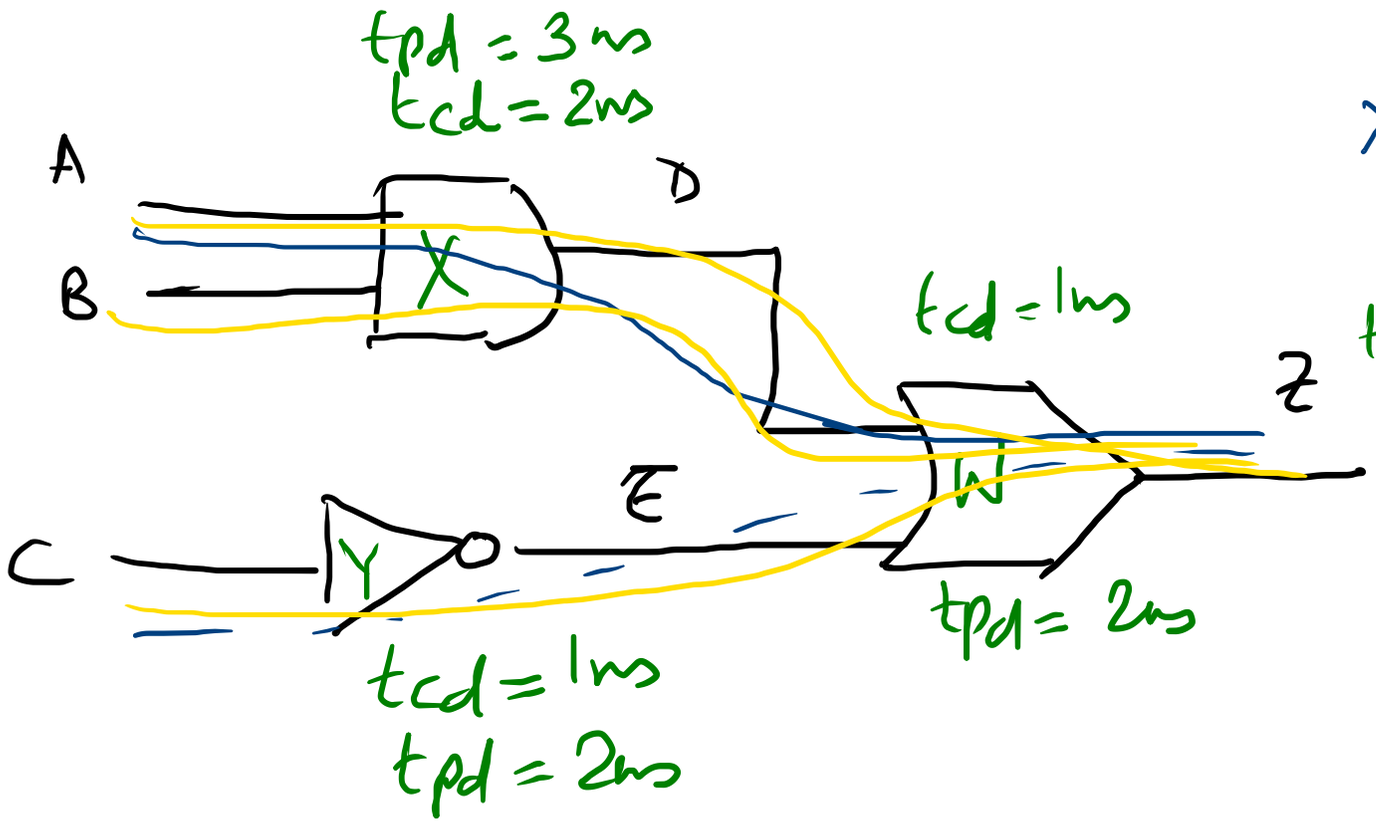






tcd = contamination delay :
Time or delay indicates the amount of time needed for a change in a logic input to result in an initial change at an output.. That means $t_{cd} < t_{pd}$

Combinational logic delays ⇒ always additive



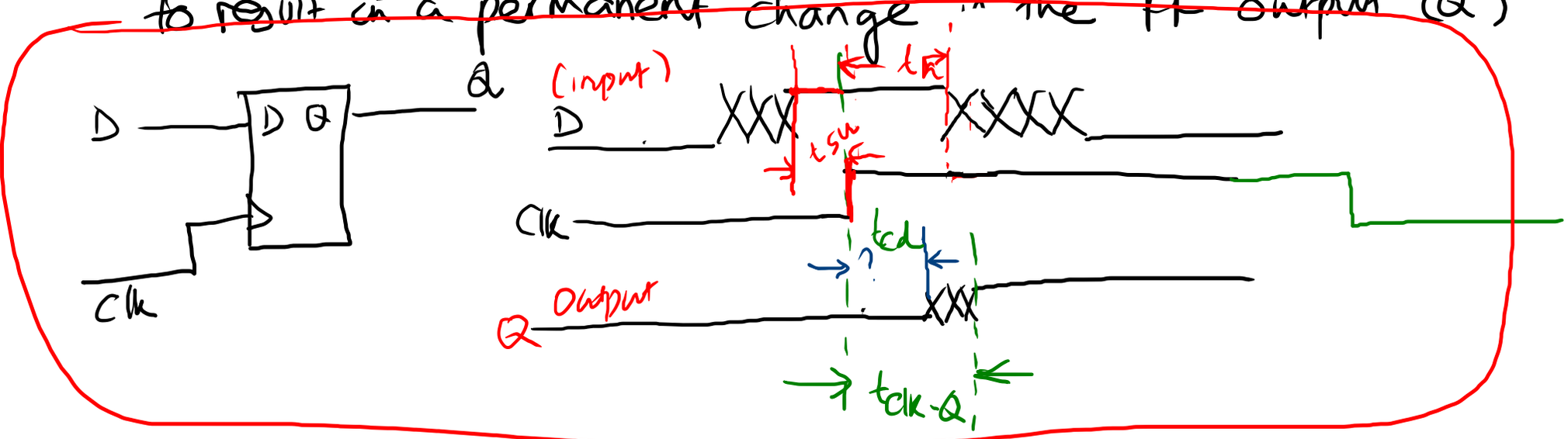
X-W = ~~3ns+~~
tpd of X + tpd W
3ns + 2ns = 5ns
tcd = 2+1 = 3ns

Y-W = tpd_y and tpd W
= 2ns + 2ns = 4ns
r+1 = 2ns

Sequential Circuit :

Propagation delay :- t_{clk-Q}

Time or value indicates the time needed for a change in the ff clk (clk) input (rising or falling edge) to result in a permanent change in the ff output (Q)

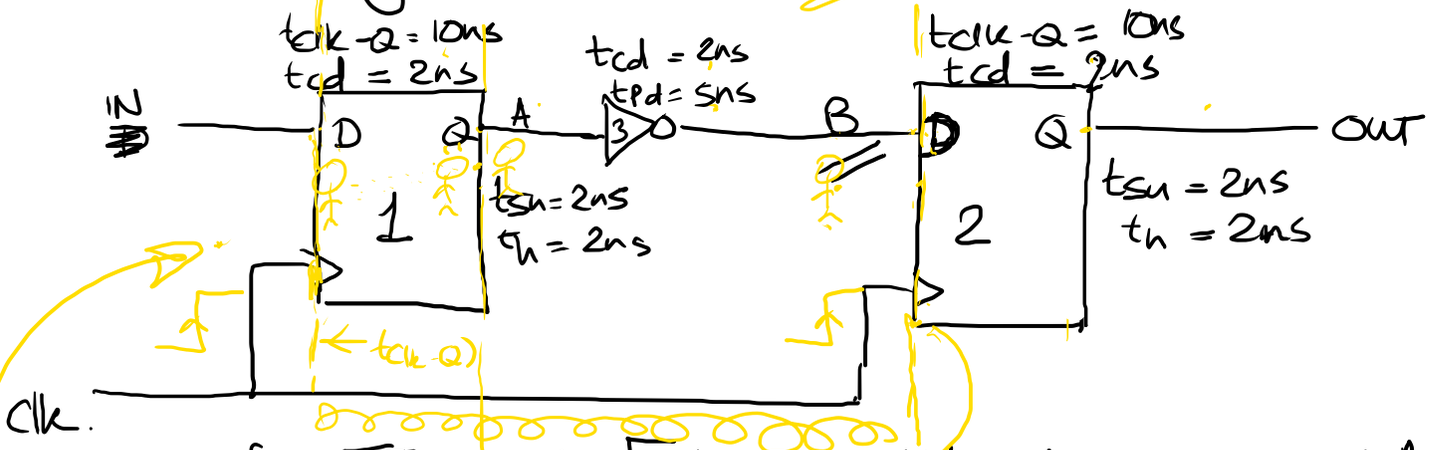


Contamination delay :- Value indicates the amount of time needed for a change in the ff clk input to result in the initial change at the ff output Q.

Setup time :- t_{su} (time, set up) value indicates the amount of time before the clock edge that data input D must be "STABLE".

Hold time : t_h (time, HOLD) value indicates the amount of time after the clock edge the data input D must be stable.

Determining maximum clock frequency:

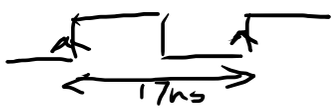


1. For FF_1 at ↑ clk a valid output appears at A after t_{clk-Q}. (10ns)
2. (For INV) A valid output appears at B after t_{pd} = 5ns
3. Signal B is clocked on the ↑ clk.

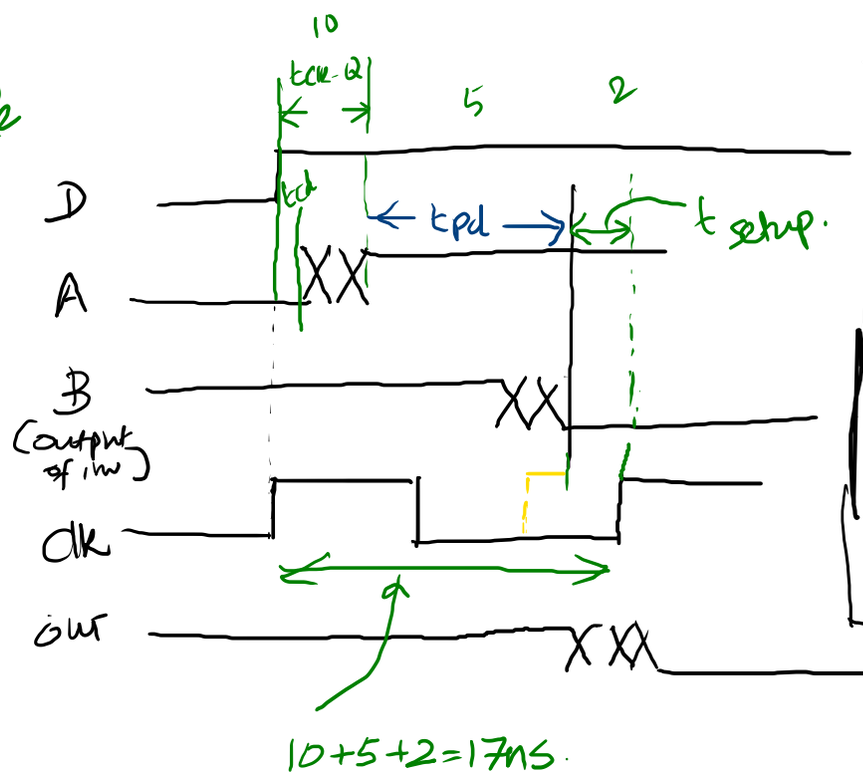
   Condn: signal must arrive at least t_{su}=2ns before the ↑ clk.

What is the max. clk period T_{min} for the ckt:

IB. $T_{min} = t_{clk-Q}(1) + t_{pd}(INV) + t_{su}(2) = 10 + 5 + 2\,ns$
$= 17\,ns.$



not exactly to the scale



$T_{FF1-FF2} = t_{clk-Q(FF1)} + t_{su(FF2)} = 10+2 = 12\,ns$

$= t_{clk-Q(FF1)} + t_{pd(INV)} + t_{su(FF2)}$

$= 10 + 5 + 2$

$= 17\,ns.$