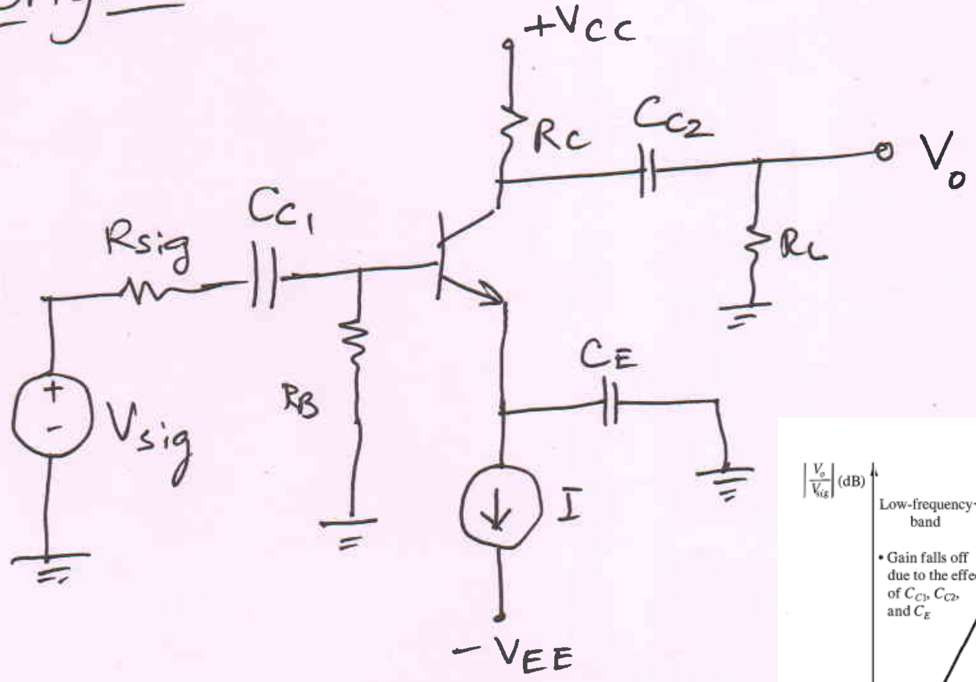
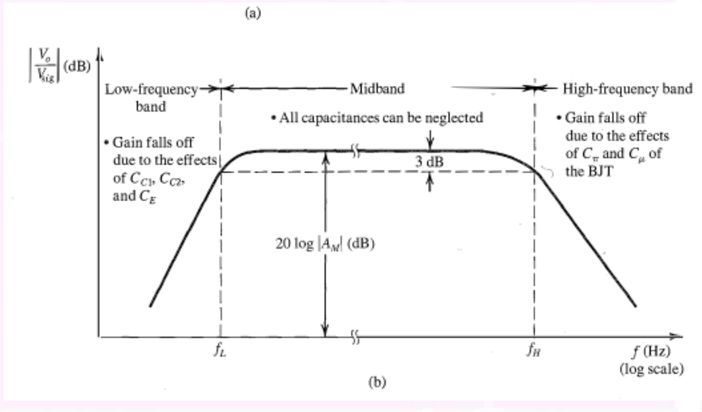
LOW FREQUENCY RESPONSE OF A CE AMPLIFIER

We will now draw small signal model at low frequencies where C_{C1}, C_{C2} and C_E will not be perfect short circuits (as we assumed before in Mid Band & High Frequency Band) but will show significant reactance (or impedance). Similarly at such low frequencies the effect of C_π and C_μ will be negligible & we will not consider them. We will neglect r_o also assumed to be too high compared to R_C and R_L. Lastly we will neglect r_x which is in series with much larger quantity r_π.

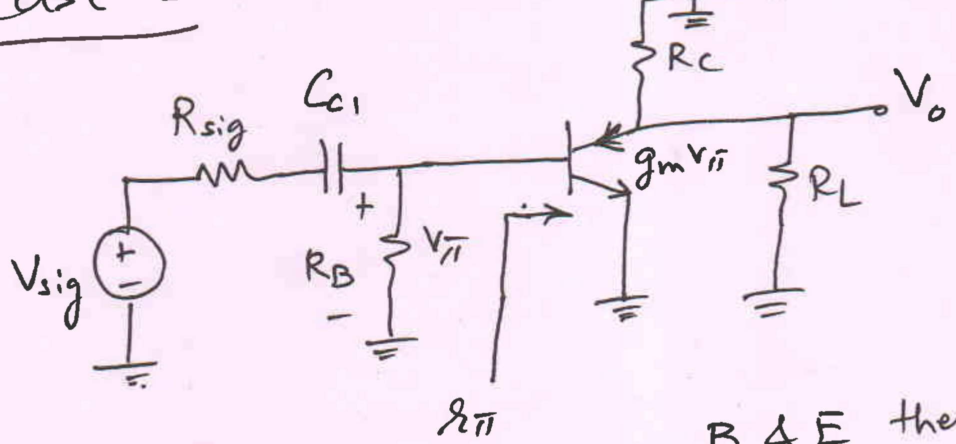
Original Circuit with biasing.





We will solve this circuit to find out effect of C_{C1}, C_{C2} and C_E by considering effect of each ~~of~~ one of them separately assuming that when one is considered, other two are perfect short circuit. So while evaluating effect of C_{C1}, we will assume C_{C2} and C_E to be SC.

Case I : Consider only C_{C1}.



We can see that between B & E there are R_B & r_π in $\|$.
V_{sig} sees three elements in series — R_{sig}, C_{C1} & $(R_B \| r_\pi)$.

$$\therefore V_\pi = \frac{R_B \| r_\pi}{(R_B \| r_\pi) + R_{sig} + \frac{1}{sC_{c1}}} \cdot V_{sig}$$

Output Voltage

$$V_o = -g_m \cdot V_\pi (R_C \| R_L)$$

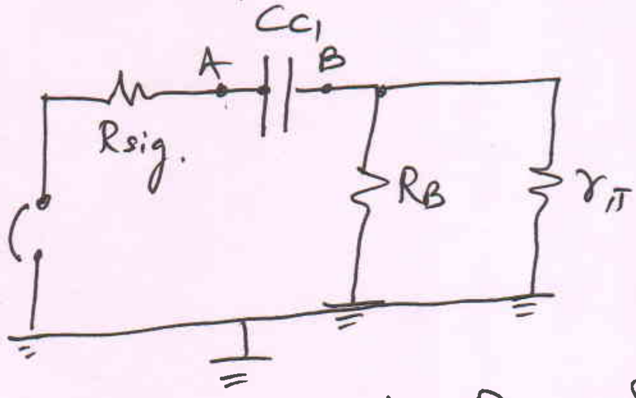
$\therefore$ Overall Voltage Gain

$$\frac{V_o}{V_{sig}} = -g_m (R_C \| R_L) \left\{ \frac{(R_B \| r_\pi)}{(R_B \| r_\pi + R_{sig})} \right\} \left[\frac{s}{s + \frac{1}{C_{c1}[R_B \| r_\pi + R_{sig}]}} \right]$$

The right side part is frequency sensitive (3)
and represents a STC zero or High Pass
type circuit with a corner frequency ω_{P1}

$$\omega_{P_1} = \frac{1}{C_{C_1}\left[\left(R_B \| r_\pi\right) + R_{sig}\right]}$$

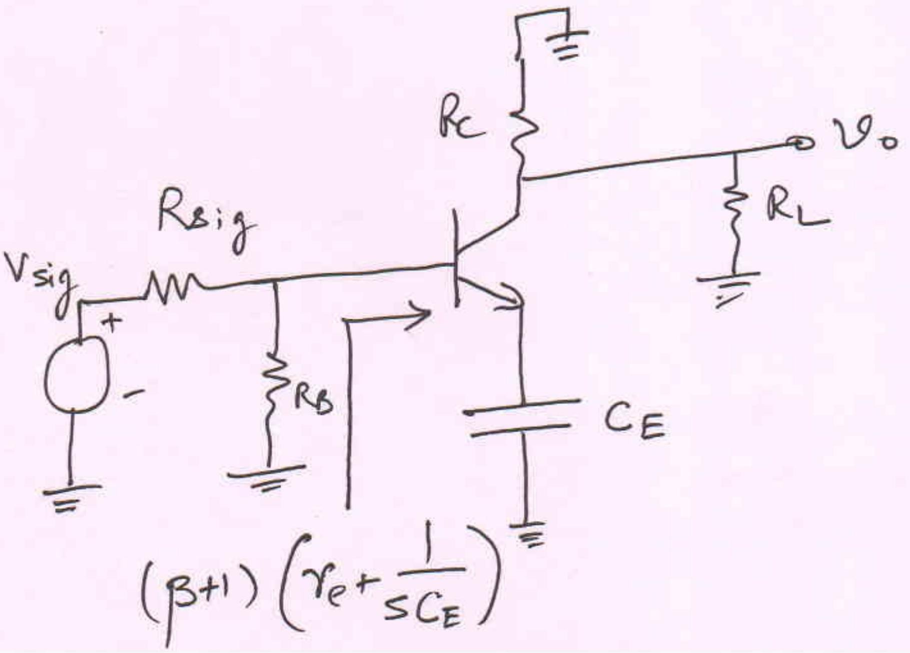
The part in [ ] brackets is Req as seen across the terminals of CC_1 when Vsig is set to 0.



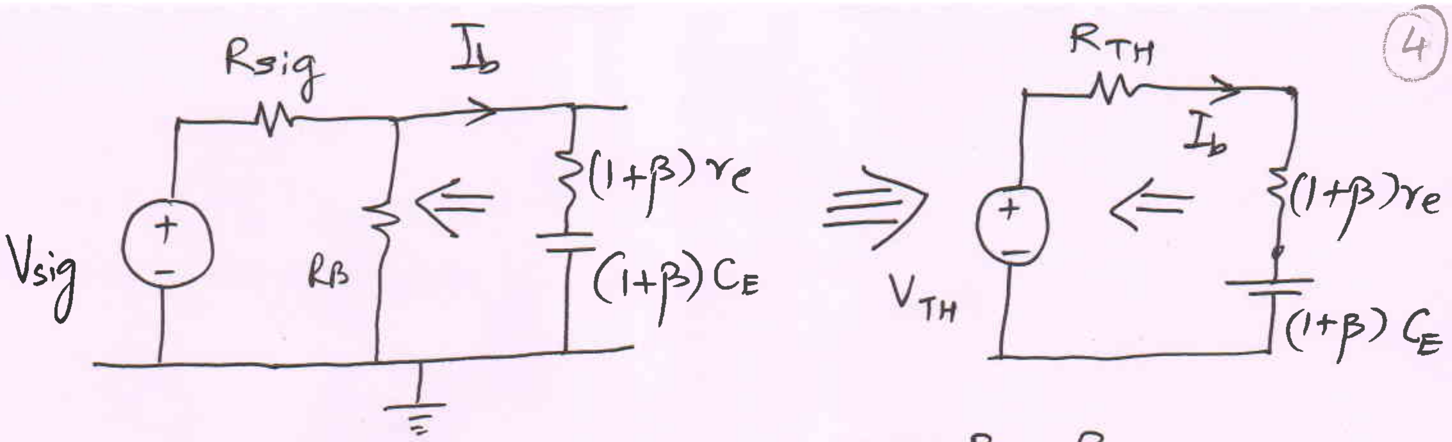
Req is between A & B
$= R_{sig} + R_B \| r_\pi$.

We have obtained Req & ω_{P1} connected with C_{C1}.

Case II : Consider only C_E
CC_1 & CC_2 are perfect short circuits.



We reflect r_e and C_E into base circuit.



$$R_{TH} = \frac{R_B \cdot R_{sig}}{R_B + R_{sig}}$$

$$\Rightarrow \quad V_{TH} = \frac{R_B}{R_B + R_{sig}} \cdot V_{sig}.$$

Hence I_b will be

$$I_b = \frac{\cancel{V_{sig}}.V_{TH}}{R_{TH} + (1+\beta) r_e + (1+\beta)\frac{1}{sC_E}}$$

$$= \frac{R_B}{R_B + R_{sig}} \left\{ \frac{1}{(R_B \| R_{sig}) + (1+\beta)\left(r_e + \frac{1}{sC_E}\right)} \right\} . V_{sig}$$

The output current source $= \beta I_b$

and output Voltage $V_o = -\beta \cdot I_b \cdot (R_C \| R_L)$

$\therefore$ Overall Voltage Gain $= \dfrac{V_o}{V_{sig}}$

$$= -\left(\frac{R_B}{R_B + R_{sig}}\right) \left\{ \frac{\beta (R_C \| R_L)}{(R_B \| R_{sig}) + (1+\beta) r_e} \right\} \frac{s}{s + \dfrac{1}{C_E\left(r_e + \dfrac{R_B \| R_{sig}}{\beta+1}\right)}}$$

The extreme right side factor gives STC high pass filter with 3 db corner frequency ω_{P_2} as

$$\omega_{P_2} = \frac{1}{C_E\left[r_e + \frac{R_B \| R_{sig}}{(1+\beta)}\right]}$$

Note that the resistor component or Req. can be given as

$$R_{eq} = r_e + \frac{R_B \| R_{sig}}{1+\beta}$$

= resist~~or~~ance seen by C_E looking into Emitter when Vsig is grounded. The base resistance to ground $R_B \| R_{sig}$ is reflected $1/(\beta+1)$ when transferred from base to emitter and put in series with r_e.

$$f_{P_2} = \frac{1}{2\pi C_E\left[r_e + \frac{R_B \| R_{sig}}{1+\beta}\right]}$$

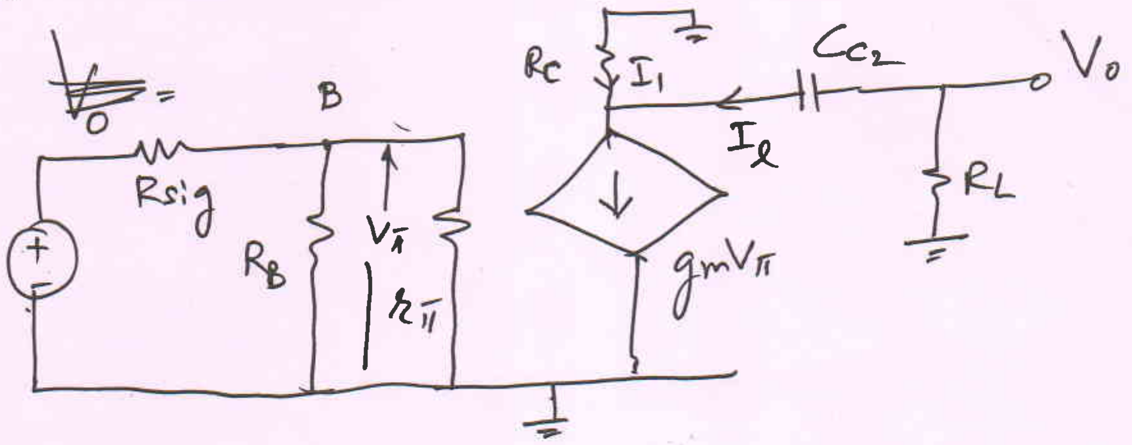
Note that r_e is small and $(R_B \| R_{sig})$ get divided by $(1+\beta)$ which is large so they also contribute small. Thus f_{P_2} will be higher than f_{P_1} (and possibly than f_{P_3} also).

Case III Consider Only C_{C2}.

Since C_{C1} and C_{E} are perfect short circuit, we can write V_π as in mid band —

$$V_\pi = V_{sig} \frac{R_B \parallel r_\pi}{(R_B \parallel r_\pi) + R_{sig}}$$

~~and~~ Now see the output in model :



$$V_o = I_l \cdot R_L \quad \text{—(1)} \qquad g_m V_\pi = I_1 + I_l \quad \text{—(2)}$$

$$\frac{I_l}{I_1} = \frac{Y_l}{Y_{RC}} = \frac{Z_{RC}}{Z_l} = \frac{R_C}{R_L + \frac{1}{C_{C2} \cdot s}}$$

$$\therefore \; I_l = I_1 \cdot \frac{R_C}{R_L + \frac{1}{C_{C2} \cdot s}} \quad \text{—(3)}$$

Therefore,

$$\frac{V_o}{V_{sig}} = \left\{ - \frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{sig}} \right\} g_m (R_C \parallel R_L) \left[\frac{s}{s + \frac{1}{C_{C2}(R_C + R_L)}} \right]$$

The part in rectangular bracket is frequency sensitive STC part and gives us corner frequency ω_{P_3} as

$$\omega_{P_3} = \frac{1}{C_{C_2}(R_C + R_L)}$$

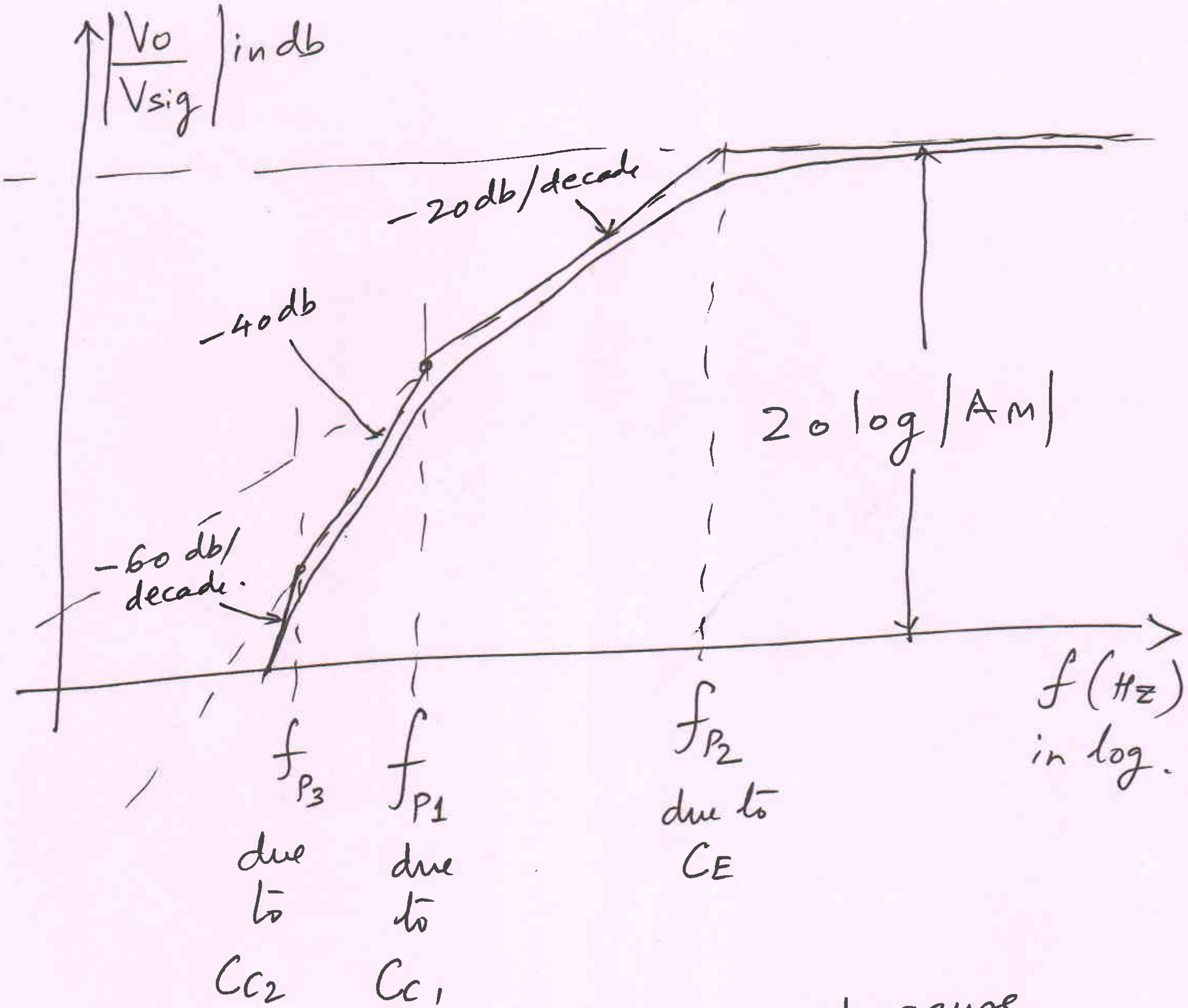
where $(R_C + R_L)$ is resistance as seen by C_{C_2} when $V_{sig} = 0$ and current source is opened.

— x —

We have estimated effect of each capacitor when contributing alone. Now if we assume that all 3 affect simultaneously but without interacting with each other. In other words, if they are widely separeted in their f values then we can write transfer fn. as

$$\frac{V_o}{V_{sig}} = -A_M\left(\frac{s}{(s+\omega_{P_1})}\right)\left(\frac{s}{s+\omega_{P_2}}\right)\left(\frac{s}{s+\omega_{P_3}}\right)$$

Each one will contribute a 20 db/decade slope as shown.



Usually f_{P2} is dominant one because

f_L is largest of f_{P1}, f_{P2} and f_{P3}

and that is usually f_{P2}.

If the 3 frequencies are close to each other and they interact then calculations become complex. ~~As~~ a first approx. we can assume

$$f_L = f_{P1} + f_{P2} + f_{P3}.$$

Each corner frequency pushes lower cutoff freq f_L, up and above & reduces Bandwidth.

How to select values of C_{C_1}, C_{C_2} & C_E?

The design objective is to place lower cutoff frequency f_L of the amplifier at a desired value or location. Since C_E sees a very small resistance, it is usually the dominent freq. and we should use C_E to affect f_{P2} which is close to f_L. Then select f_{P1} and f_{P3} far lower than f_{P2}. This method gives minimum sum total of 3 capacitors & saves cost & space.

For example in equation $f_L = f_{P_1} + f_{P_2} + f_{P_3}$
if we set $f_{P_2} = 0.8 f_L$ and rest both as $0.1 f_L$ then
we will select C_E such that

$$f_{P_2} = 0.8 f_L = \frac{1}{2\pi (R_E)\, C_E}$$

Calculate resistors seen by each capacitor

by C_{C1}, let us call it R_{C1}

$$R_{C_1} = (R_B \parallel r_\pi) + R_{sig} \qquad 0.1 f_L = \frac{1}{2\pi R_{C_1} \cdot C_{C_1}}$$

by C_E, let us call it R_E

$$R_E = r_e + \frac{R_B \parallel R_{sig}}{(1+\beta)} \qquad 0.8 f_L = \frac{1}{2\pi R_E \cdot C_E}$$

by C_{C2}, let us call it R_{C2}

$$R_{C2} = R_C + R_L \qquad f_{P_3} = 0.1 f_L = \frac{1}{2\pi R_{C2} \cdot C_{C2}}$$

Get exact value of C_{C1}, C_{C2} & C_E from above and then put standard commercially available capacitor values, just next higher e.g. if you get $C_{C1} = 1.8\,\mu F$, $C_E = 27\,\mu F$ and $C_{C2} = 2.7\,\mu F$ then use $C_{C1} = 2.2\,\mu F$ or $3.3\,\mu F$ and $C_{C2} = 3.3\,\mu F$ or $4.7\,\mu F$. $C_E =$ ~~47~~ $33\,\mu F$ or $47\,\mu F$

Putting slightly higher value of Commercial value available will ensure that your design lower cutoff frequency will be slightly lower than what you wish to achieve and give you slightly better or more bandwidth.

Solve problems Example 3.19, Exercise 3.52

Solve unsolved problems 3.159, 3.160, 3.161 also at home.