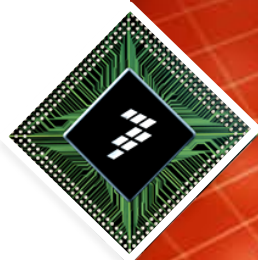




ARM Cortex-M0+ Core *Technical Introduction*

hitex: ARM – The New Standard Across The Board?



May 2012

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Mark Dunnett
Senior Field Applications Engineer



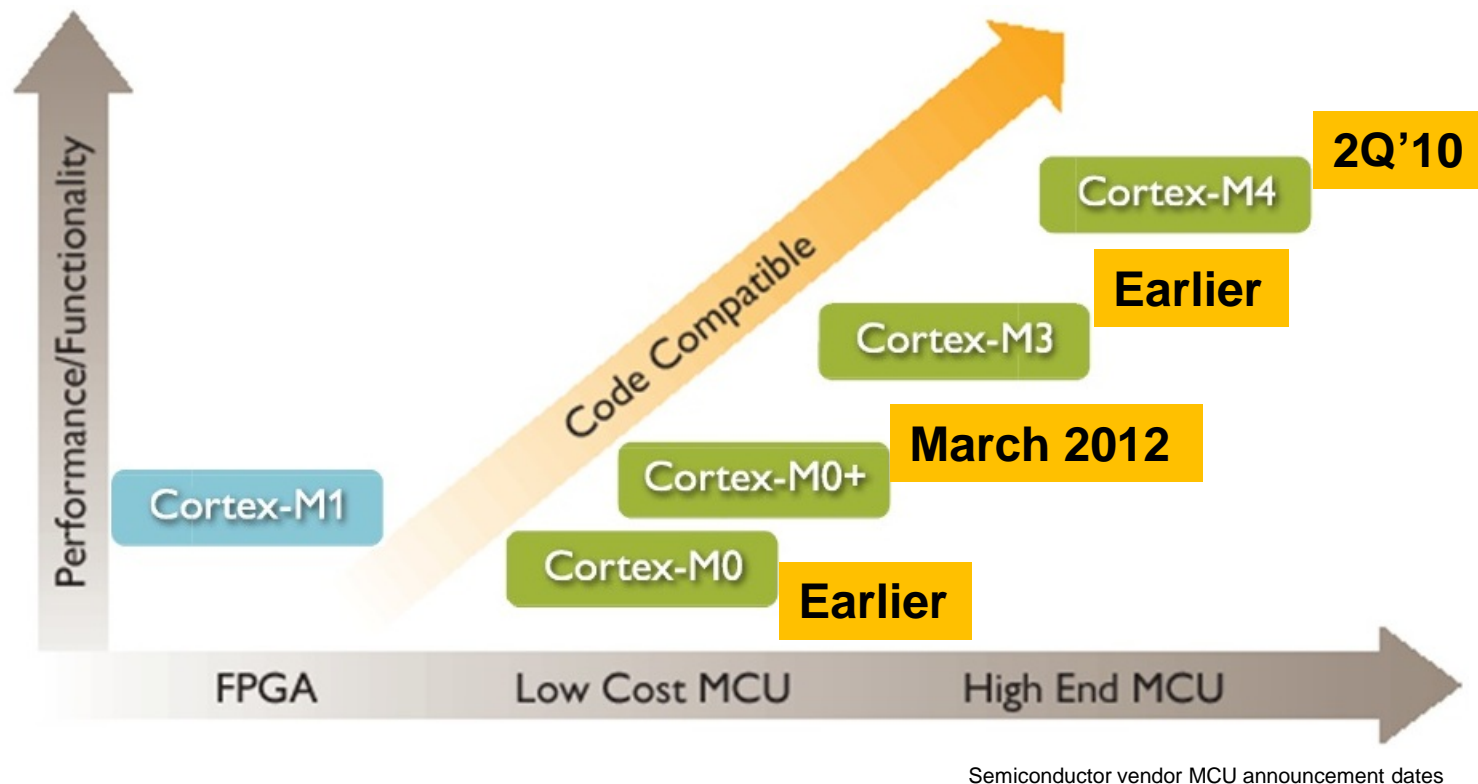
The ARM Cortex-M0+ core: a technical introduction

ARM continue to invest in cost-effective cores suited to the low-end microcontroller space. In this technical presentation, Mark will introduce the differences between the well-known Cortex™ M3/M4 cores, and the recently-announced **M0+ core** suited to 8-bit replacement. The ARM Cortex-M0+ core offers **improved performance**, **energy efficiency** and **ease-of-use** in comparison to the Cortex-M0, but retains full compatibility with all other Cortex-M class cores enabling reuse of existing compiler and debug tools. The material will cover improvements in the **GPIO handling capability**, increases in **performance** over the existing M0 core, and the sophisticated **Micro Trace Buffer** trace capability. All this is achieved whilst extending ARM's **industry leading low power** performance with a quoted dynamic power of 11uW/MHz.

ARM



Cortex-M Processor Series



Cortex-M Processor Series: *compared*

ARM Cortex-M	SysTick	Bit Banding	MPU	Pipeline
M0	Optional	No	No	3
M0+	Yes	No	Optional	2
M3	Yes	Optional	Optional	3
M4	Yes	Optional*	Optional*	3

ARM Cortex-M	Thumb	Thumb 2	Mul (Cycle)	Div	Sat.	DSP	FPU
M0	Most	Subset	1/32	No	No	No	No
M0+	Most	Subset	1*/32	No	No	No	No
M3	All	All	1	Yes	Yes	No	No
M4	All	All	1	Yes	Yes	Yes	Optional*

*Semiconductor vendor Freescale: Yes

Cortex-M Processor Series: *compared*

Cortex-M0+

- 56 Instructions
- Mostly 16-bit
- Operate on 32-bit registers
- Optional fast MUL (32x32 in 1 cycle)

VABS	VADD	VCMP	VCMP	VCMP	VCMP	VCMP	VCMP
VLDR	VMLA	VMLS	VMOV	VMSR	VMSR	VMUL	VNEG
VNMLA	VMMLS	VNMUL	VPOP	VPUSH	VSQRT	VSTM	VSTR
VSUB	VFMA	VFMS	VFNMA	VFNMS			

Cortex-M4 FPU

PKH	QADD	QADD16	QADD8	QASX	QDADD	QDSUB	QSAX
QSUB	QSUB16	QSUB8	SADD16	SADD8	SASX	SEL	SHADD16
SHADD8	SHASX	SHSAX	SHSUB16	SHSUB8	SMLABB	SMLABT	SMLATB
SMLATT	SMLAD	SMLALBB	SMLALBT	SMLALTB	SMLALTT	SMLALD	SMLAWB
SMLAWT	SMLSD	SMLSDD	SMMLA	SMMLS	SMMUL	SMUAD	SMULBB
						SMULBT	SMULTT
						SMULTB	SMULWT
						SMULWB	SMUSD
						SSAT16	SSAX
						SSUB16	SSUB8
						SXTAB	SXTAB16
						SXTAH	SXTB16
						UADD16	UADD8
						UASX	UHADD16
						UHADD8	UHASX
						UHSAX	UHSUB16
						UHSUB8	UMAAL
						UQADD16	UQADD8
						UQASX	UQSAX
						UQSUB16	UQSUB8
						USAD8	USADA8
						USAT16	USAX
						USUB16	USUB8
						UXTAB	UXTAB16
						UXTAH	UXTB16

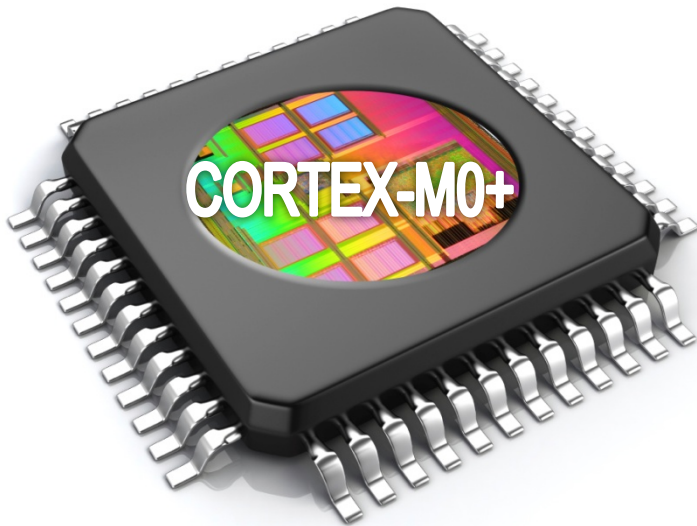
ADC	ADD	ADR	AND	ASR	B
CLZ	BFC	BFI	BIC	CDP	CLREX
CBNZ	CBZ	CMN	CMP	DBG	EOR
LDMIA	LDMDDB	LDR	LDRB	LDRBT	LDRD
LDREX	LDREXB	LDREXH	LDRH	LDRHT	LDRSB
LDRSBT	LDRSHT	LDRSH	LDRT	MCR	LSL
LSR	MCRR	MLS	MLA	MOV	MOVT
MRC	MRRC	MUL	MVN	NOP	ORN
ORR	PLD	PLDW	PLI	POP	PUSH
RBIT	REV	REV16	REVSH	ROR	RRX
			RSB	SBC	SBC
			SDIV	SEV	SMLAL
			SMULL	SSAT	STC
			STMIA	STMDB	STR
			STRB	STRBT	STRD
			STREX	STREXB	STREXH
			STRH	STRHT	STRT
			SUB	SXTB	SXTH
			TBB	TBH	TEQ
			TST	UBFX	UDIV
			UMLAL	UMULL	USAT
			UXTB	UXTH	WFE
			WFI	YIELD	IT

Cortex-M3

BKPT	BLX	ADC	ADD	ADR
BX	CPS	AND	ASR	B
DMB		BL		BIC
DSB	CMN	CMP	EOR	
ISB	LDR	LDRB	LDM	
MRS	LDRH	LDRSB	LDRSH	
MSR	LSL	LSR	MOV	
NOP	REV	MUL	MYN	ORR
REV16	REVSH	POP	PUSH	ROR
SEV	SXTB	RSB	SBC	STM
SXTH	UXTB	STR	STRB	STRH
UXTH	WFE	SUB	SVC	TST
WFI	YIELD			

Cortex-M0/M0+/M1

Cortex-M0+ *The solution for entry-level 32-bit*



EASE OF USE

ENERGY EFFICIENCY

LOW COST

PERFORMANCE

ECOSYSTEM

SCALABILITY

Simple Set of Program Registers

E
A
S
E

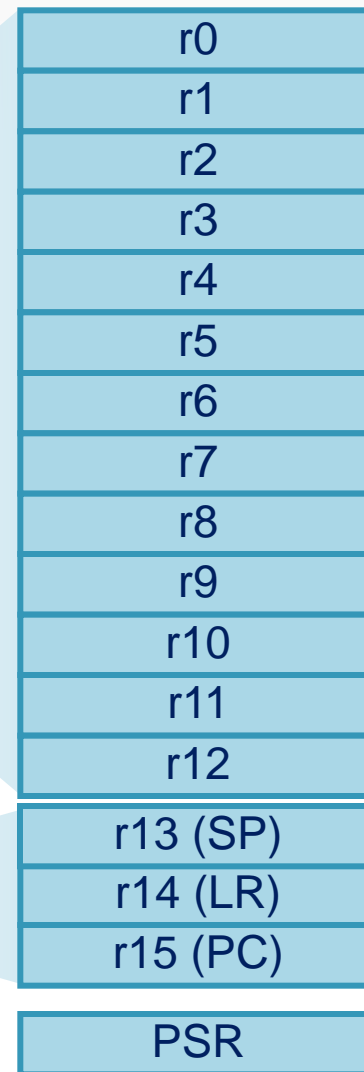
O
F

U
S
E

- All registers are 32-bit wide
- 13 general purpose registers
- Only 3 special registers
- Program Status Register

Compared with 8-bit:

- Less stacking
- Faster function calls
- Globals optimisation



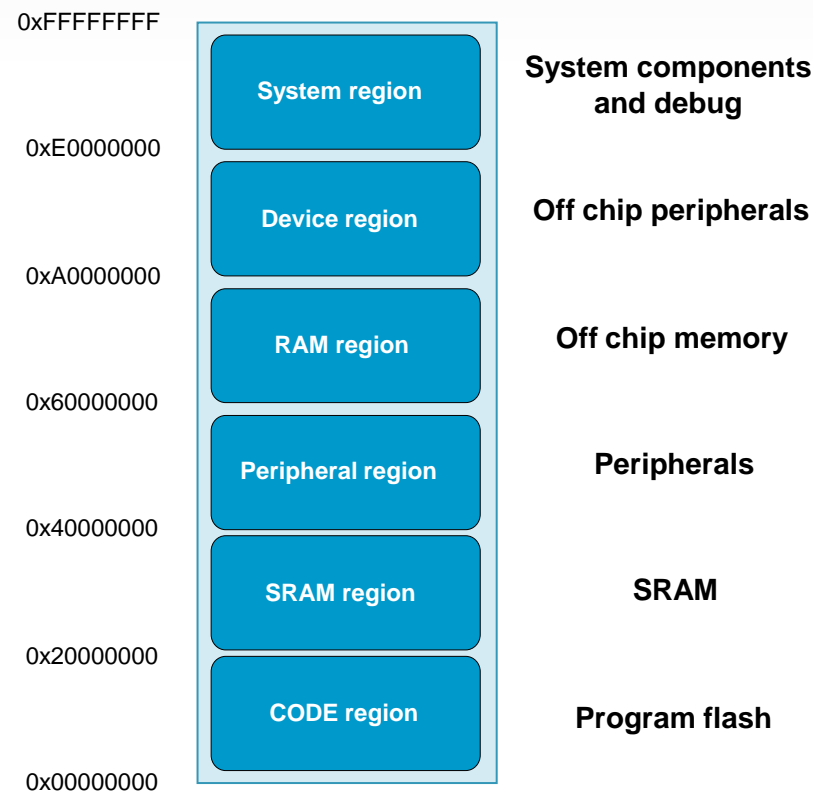
Straightforward Memory Map

E
A
S
E

O
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U
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E

- 4GB linear memory
- No paging/banking
- All locations always accessible by the SW



- Standard across all Cortex-M implementations
- Cortex-M0+ offers an optional MPU

Straightforward Memory Map

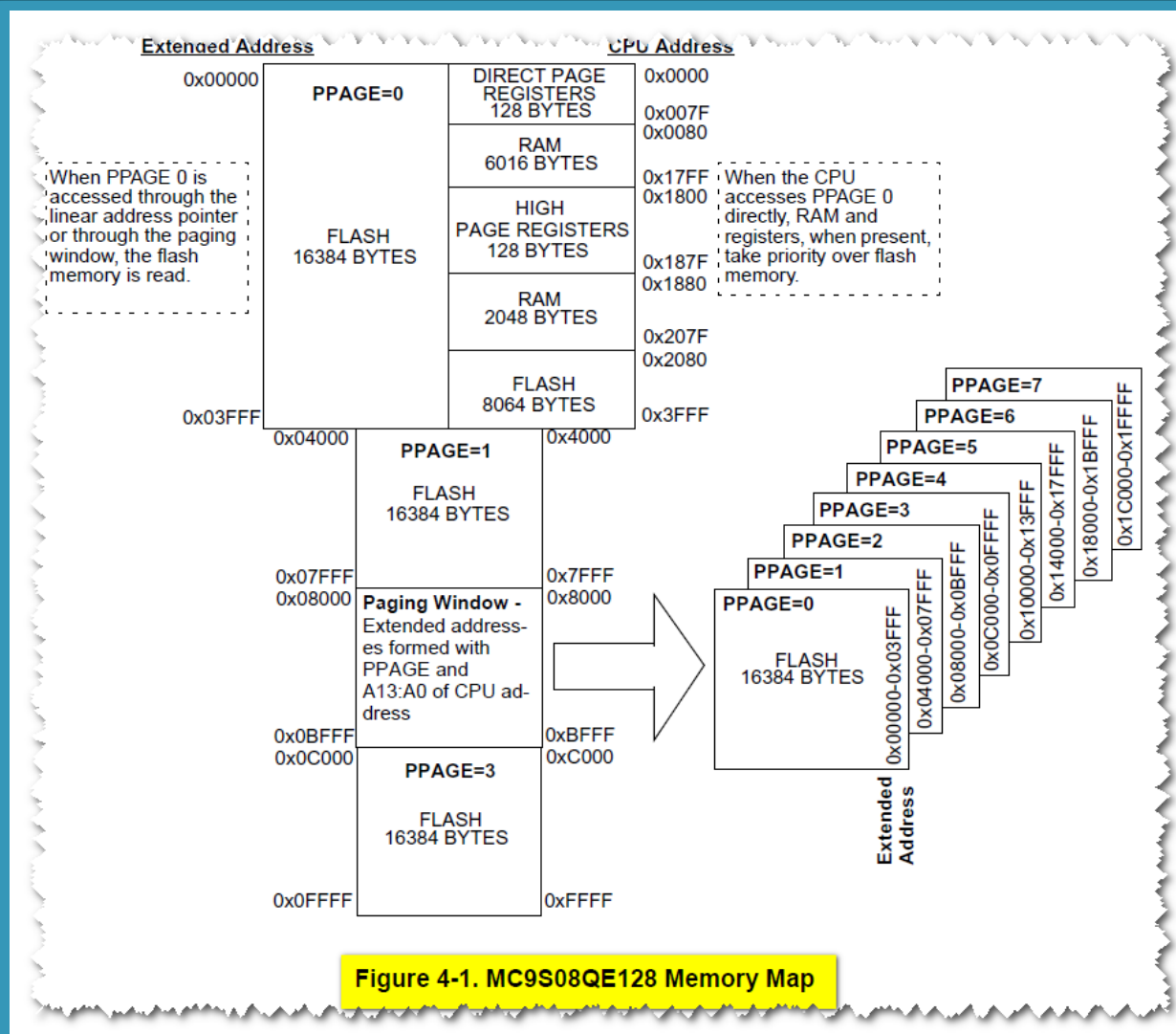


Figure 4-1. MC9S08QE128 Memory Map

32-bit?? What about code density??

- 32-bit *data*
- 16-bit *instructions*

- Example - MOV

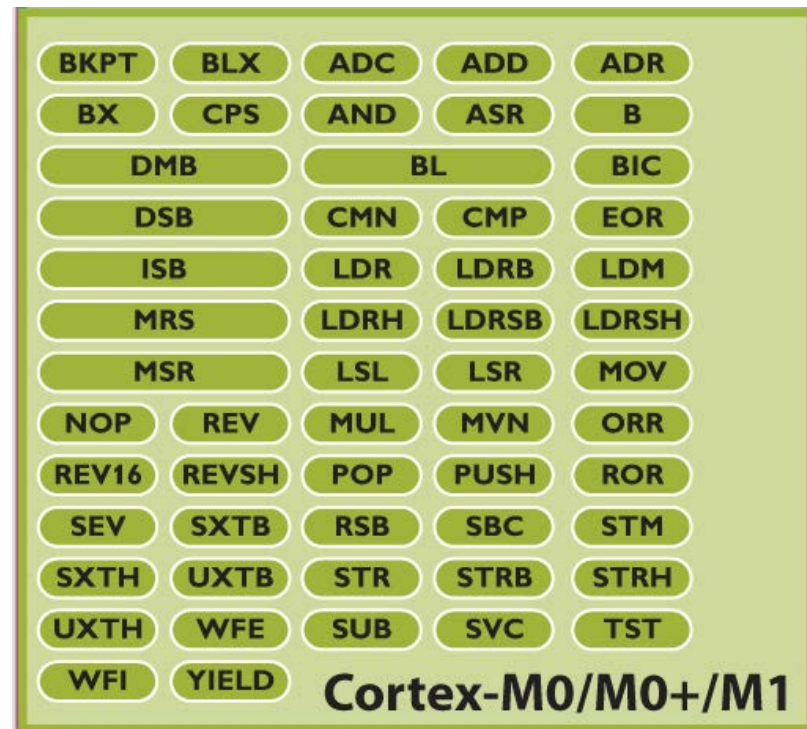
- HCS08 Architecture (3)

Source Form	Addr. Mode	Machine Code		HCS08 Cycles
		Opcode	Operand(s)	
MOV <i>opr8a,opr8a</i>	DIR/DIR	4E	dd dd	5

- Cortex-M0+ (2)

MOV<C> <Rd>, <Rm>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	0	D			Rm				Rd



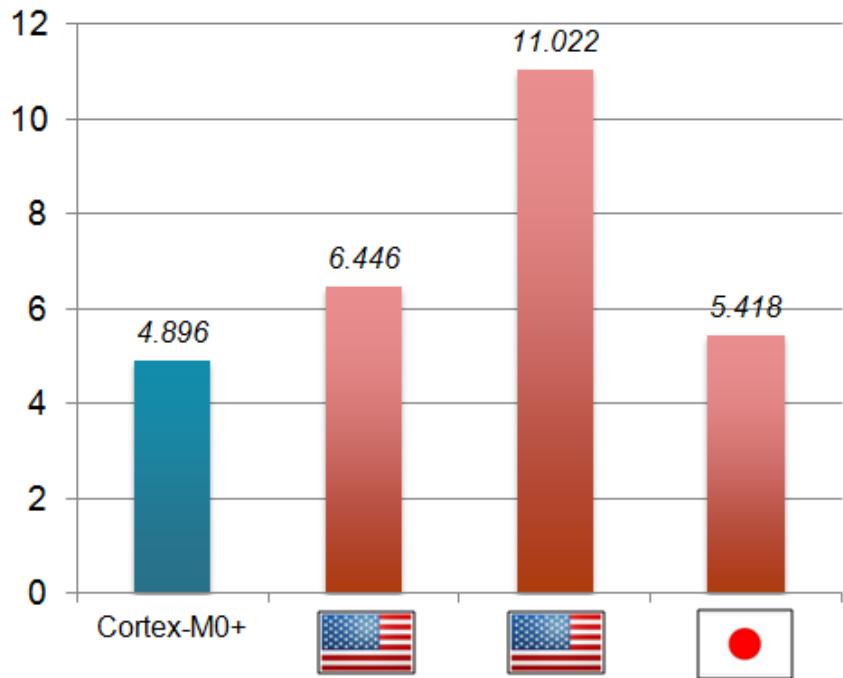
Size optimized solution

L
O
W

C
O
S
T

- **Best in class code density, reducing flash size needed**
- **Smaller flash size:**
 - Optimized cost
 - Lower MCU power consumption

CoreMark Code in kB



*CoreMark code compiled optimized for size
A, B, C & D - low power MCU from global vendors
Smaller number is better*

Embedded Systems are all about Interrupts

- **Nested Vectored Interrupt Controller (NVIC)**

- Interrupt prioritisation (4*)
- Interrupt masking
- Nested interrupt handling

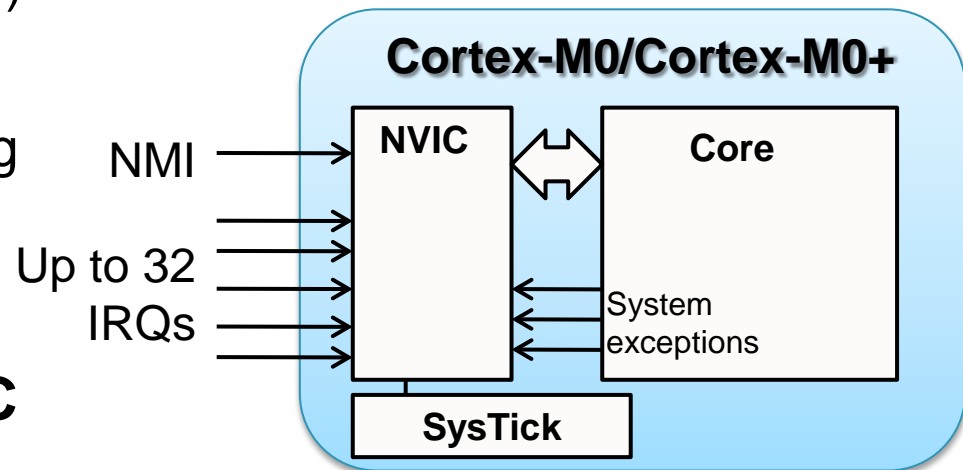
- **Interrupt handlers in C**

- **Processor handles stacking**

- r0-r3, r12 Registers
- Program Counter, Link-Register and PSR

Interrupt Service Routine starts after 15/16 cycles

Optimizations: tail-chaining & late arrival



*Semiconductor vendor Freescale

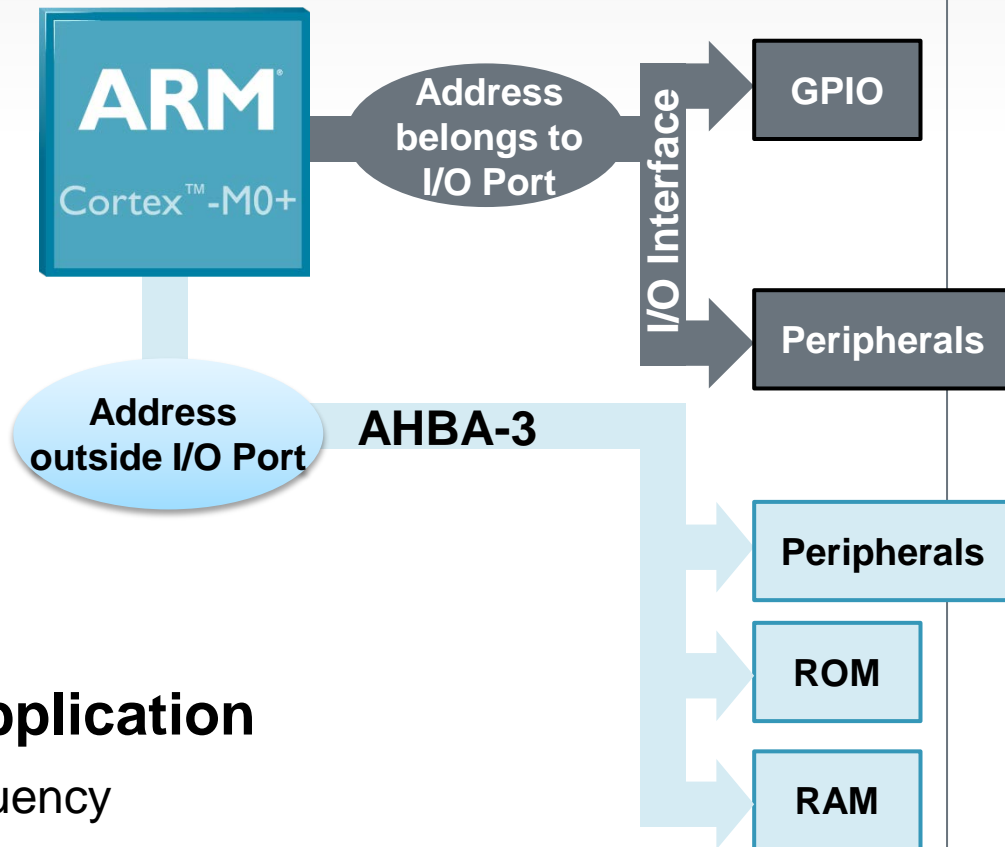
Easy and fast I/O control

- **I/O Port**

- 32-bit wide
- *Single cycle access*
- Best suited for accessing
 - GPIO
 - Peripheral registers
- Optional Feature

- **Advantages for the application**

- Higher GPIO toggling frequency
- Bit-bang the I/O as on a 8-bit!
- Save precious cycles, e.g. set faster peripherals for low-power
- “Harvard-like”: access GPIO while processor fetches next instruction



CoreSight™ Micro Trace Buffer (MTB)

E
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E

- How to bring Trace capability to low-end devices??

Cortex-M3 / ETM Debug Interface
20-pin Connector

VTref	1	<input type="checkbox"/>	<input type="checkbox"/>	2	SDWIO / TMS
GND	3	<input type="checkbox"/>	<input type="checkbox"/>	4	SWDCLK / TCK
GND	5	<input type="checkbox"/>	<input type="checkbox"/>	6	SWO/EXTa/TRACECTL / TDO
KEY	7	<input type="checkbox"/>	<input type="checkbox"/>	8	NC/EXTb / TDI
GNDDetect	9	<input type="checkbox"/>	<input type="checkbox"/>	10	EXTc
GND/TgtPwr+Cap	11	<input type="checkbox"/>	<input type="checkbox"/>	12	TRACECLK
GND/TgtPwr+Cap	13	<input type="checkbox"/>	<input type="checkbox"/>	14	TRACEDATA[0]
GND	15	<input type="checkbox"/>	<input type="checkbox"/>	16	TRACEDATA[1]
GND	17	<input type="checkbox"/>	<input type="checkbox"/>	18	TRACEDATA[2]
GND	19	<input type="checkbox"/>	<input type="checkbox"/>	20	TRACEDATA[3]

5-pin synchronous mode



QFN24 (4x4mm)*



•2-pin Serial Wire Debug (SWD)

- SWD_CLK (available on JTAG_CLK pin)
- SWD_DIO (available on JTAG_MS pin)

•2-pin cJTAG

- JTAG_CLK
- JTAG_MS

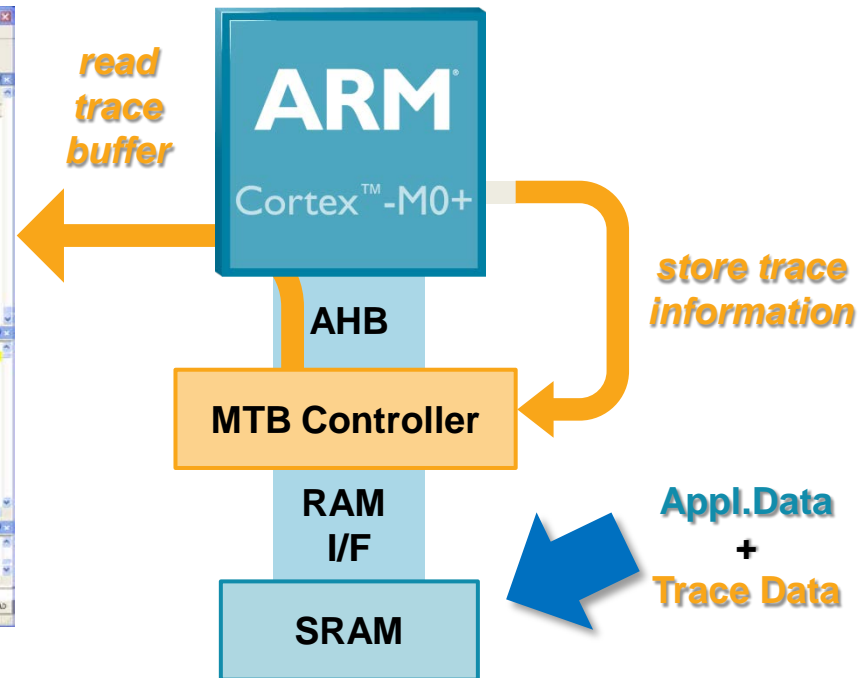
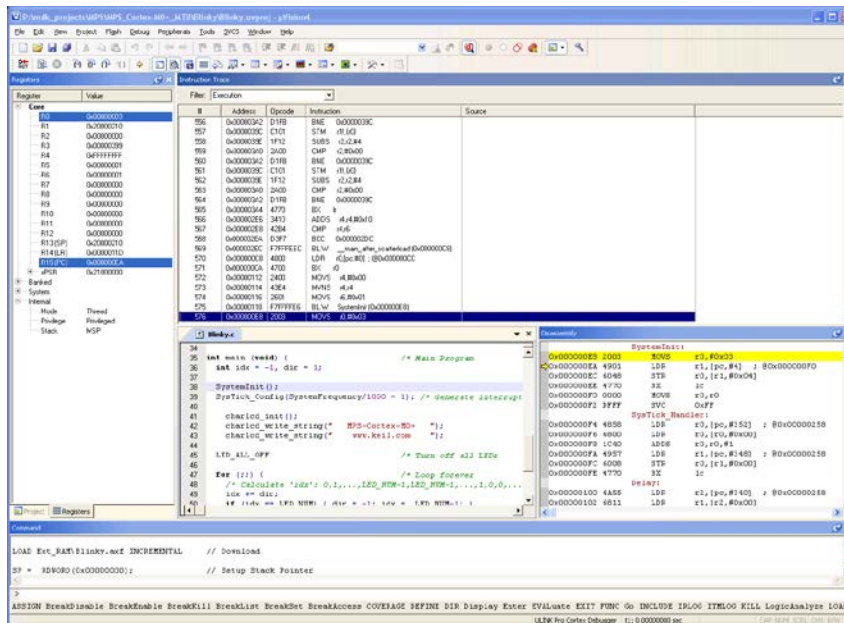
*Semiconductor vendor Freescale

CoreSight™ Micro Trace Buffer (MTB)

- Only 1.5kGate additional
- Trace stored in RAM (non intrusive)
- Read over Serial Wire Debug* (CPU stopped)



E
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- Bring fast debug advantages of trace to low-end devices

*Semiconductor vendor Freescale

Dynamic Power Consumption



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Cortex-M0+ Processor

The ARM Cortex™-M0+ processor is the most energy efficient ARM processor available. It builds on the very successful [Cortex-M0](#) processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Along with the Cortex-M0 processor, the exceptionally small silicon area, low power and minimal code footprint of these processors enable developers to achieve 32-bit performance at an 8-bit price point, bypassing the step to 16-bit devices. The Cortex-M0+ processor comes with a wide selection of options to provide flexible development.

[Request More Information](#)



[\(View Larger Cortex-M0+ Processor Image\)](#)

[Why Cortex-M0+?](#)

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[Technology](#)

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» The most energy efficient ARM processor

An optimized architecture with a core pipeline of just two stages, enables the Cortex-M0+ processor to achieve a power consumption of just **11.2uW/MHz** (90LP process, minimal configuration), while raising the performance to 1.77 CoreMark/MHz.

» Simplicity

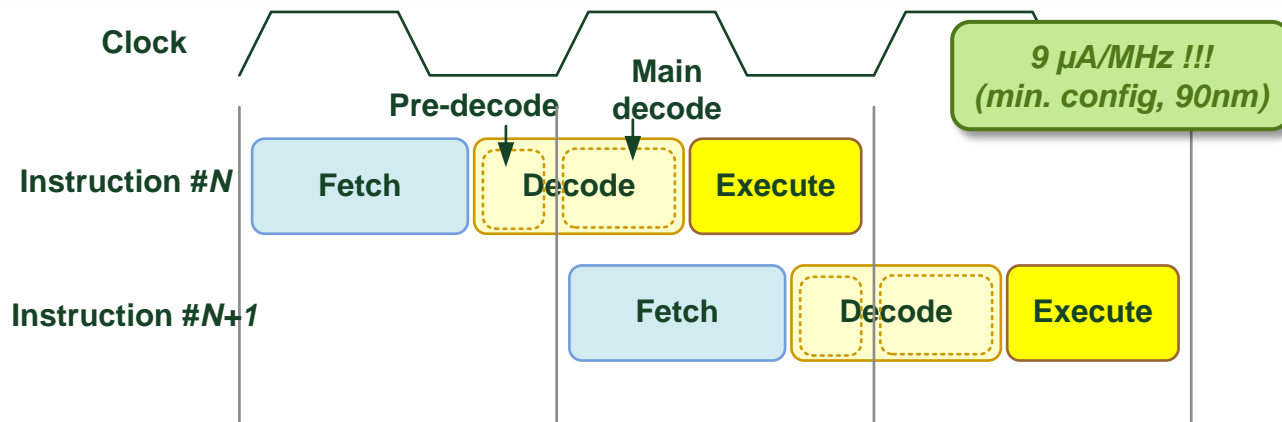
The Cortex-M0+ processor keeps the same 56 instructions of the [Cortex-M0](#) processor, enabling simple and quick development. The [Thumb® instruction set](#) offers an unrivaled code-density while providing access to 32-bit computation performance. The combination of these features make the Cortex-M0+ processor a natural and cost effective successor to 8/16-bit devices in a wide variety of applications, while retaining tool and binary upwards compatibility with the feature-rich [Cortex-M3](#) and [Cortex-M4](#).



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How?? By Cortex-M0+ design

- 2-stage pipeline von Neumann processor (1st time!)



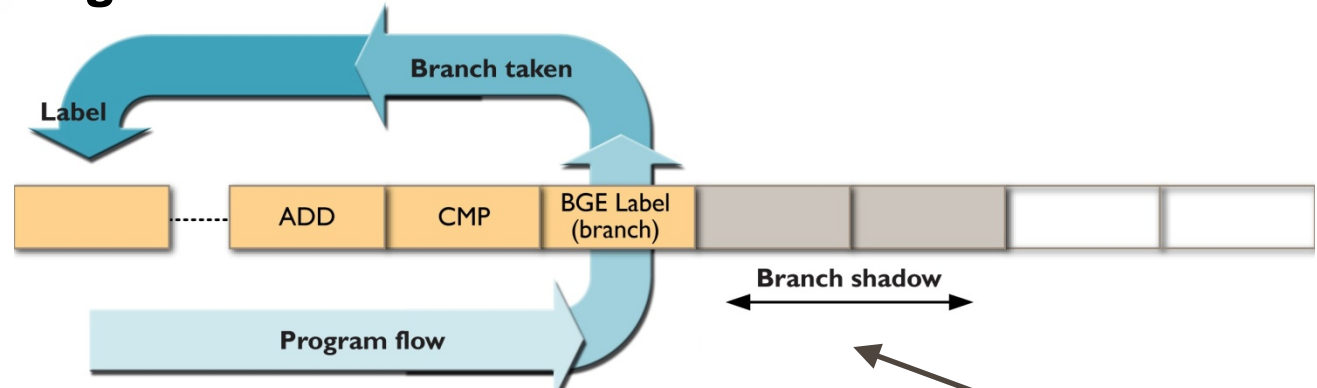
- Chasing the last μ A
 - Extensive gating of the processor
 - Minimizing flash accesses
- Save precious run cycles
 - Faster interrupt entry, faster Branch
 - Faster GPIO & peripheral access



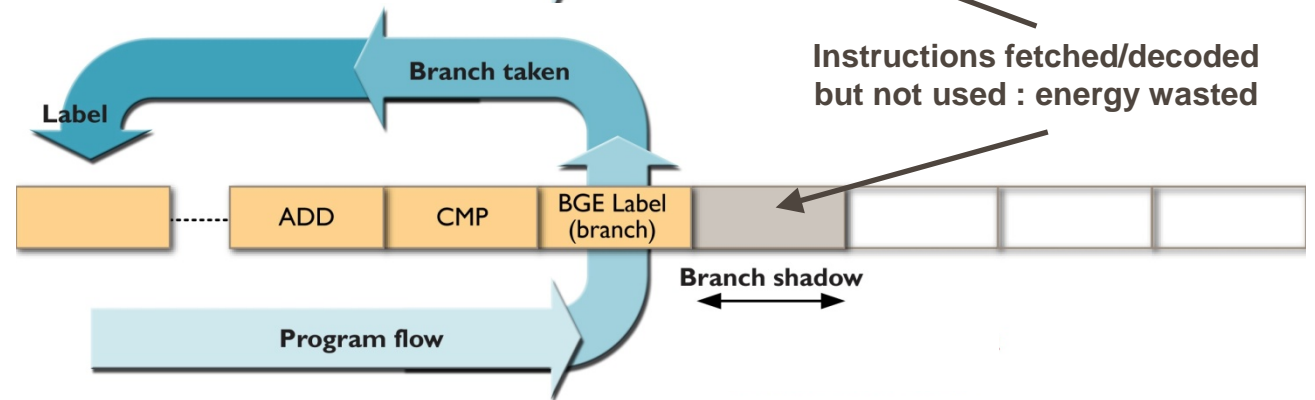
How? Higher efficiency on branch

- In pipelined processors, subsequent instructions are fetched while executing current instructions

3-stage pipeline



2-stage pipeline

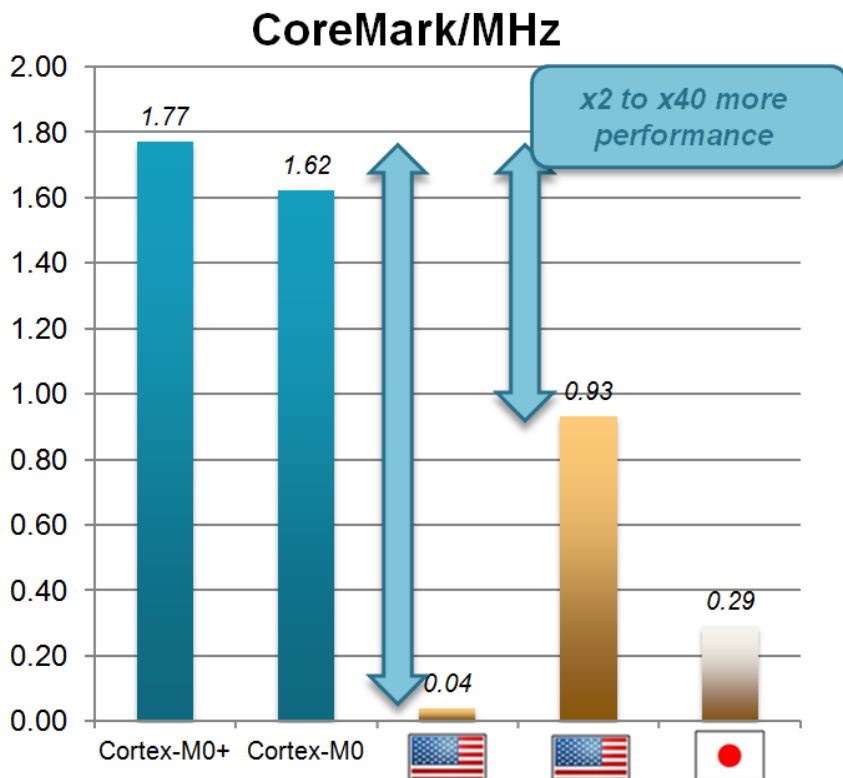
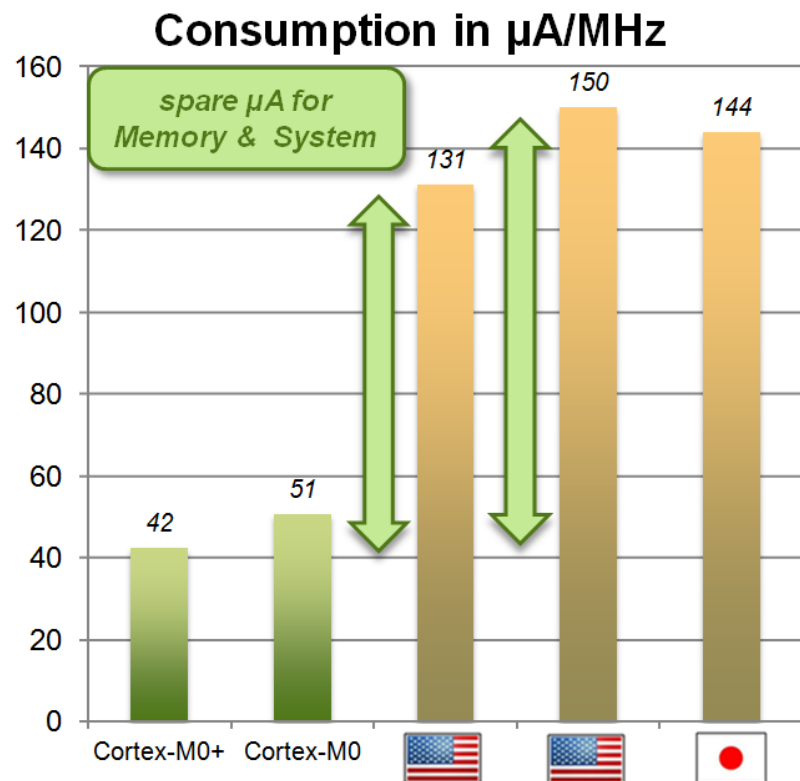


- In 2-stage pipeline:
 - Branch shadow is reduced and energy is saved!
 - Branch turn-around is 1 cycle faster!

Dynamic consumption at 8-/16-bit level

- **Enabling to design state-of-the art MCUs**

- Competitive ultra-low-power: $\geq 90\mu\text{A}/\text{MHz}$ to supply memory and system
- Quantum leap in performance: at least 2x more performance



Cortex-M0+: 1.8V, 25C, std configuration, TSMC180ULL, running CoreMark
A, B, C & D: current generation of low-power Flash MCUs, running from Flash in most favourable conditions, ~1.8-2.2V, values from Datasheet/public numbers

Kinetis MCUs with Cortex-M0+

Kinetis X Series
512K SRAM, 4MB Flash

K7x Family 120/150MHz,
512KB-1MB, Graphics LCD, Ethernet,
USB (FS/HS) Encryption, Tamper, DRAM

K6x Family 100-150MHz, 256KB-1MB,
Ethernet, USB OTG (FS/HS), Encryption, Tamper Detect, DRAM

K5x Family 72-100MHz, 28-512KB,
Analogue, USB OTG (FS), E'net, SLCD, Encryption

K4x Family
72-100MHz, 64-512KB, USB OTG (FS), SLCD

KL4x Family

K3x Family
72-100MHz, 64-512KB, Segment LCD

KL3x Family

K2x Family
50-120MHz, 32KB-1MB, USB OTG (FS/HS)

KL2x Family

K1x Family
50-120MHz, 32KB-1MB, Low Power, Mixed Signal

KL1x Family

KL0x Family

Cortex-M0+

Kinetis MCUs
Design Potential. Realized.

