ARM Cortex-M0+ Core

Technical Introduction

hitex: ARM – The New Standard Across The Board?

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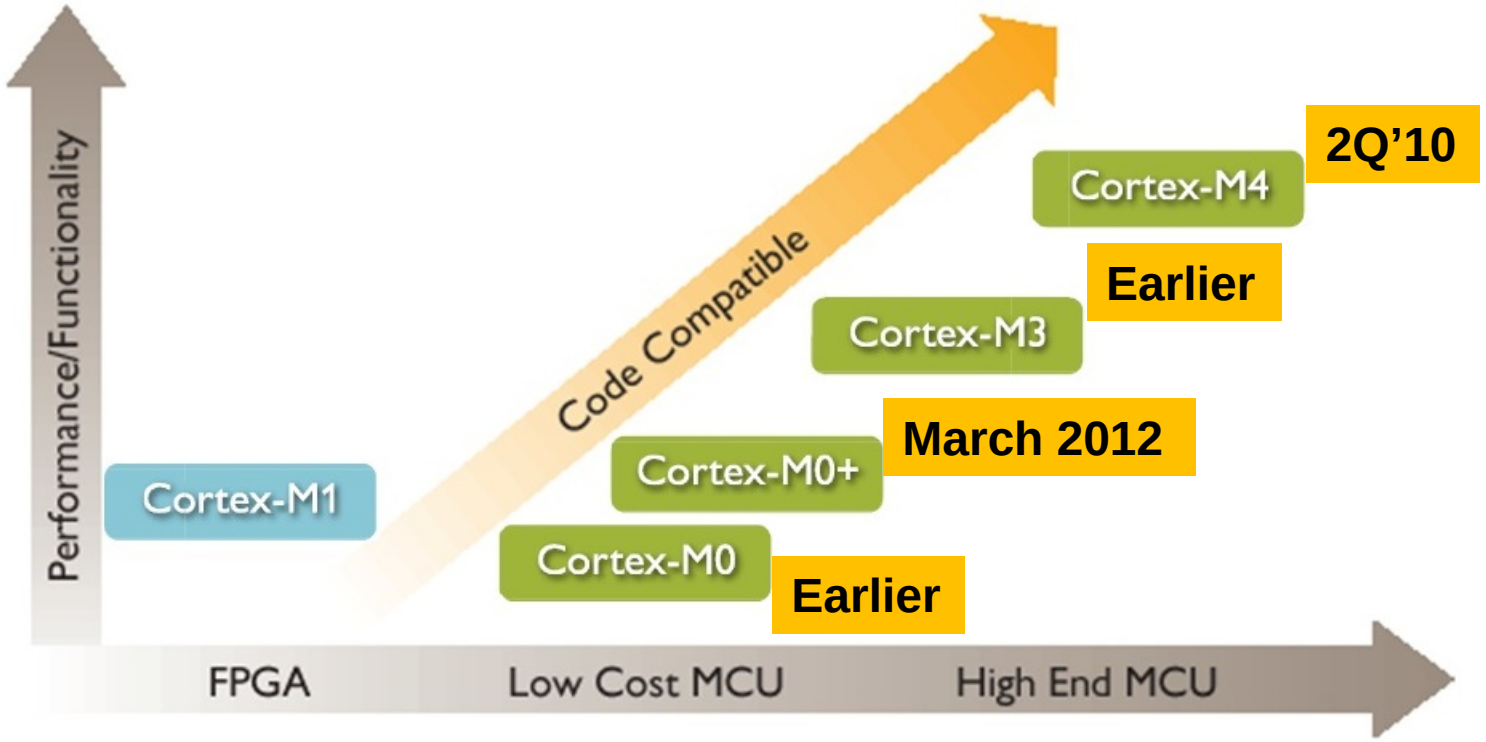
The ARM Cortex-M0+ core: a technical introduction

ARM continue to invest in cost-effective cores suited to the low-end microcontroller space. In this technical presentation, Mark will introduce the differences between the well-known Cortex™ M3/M4 cores, and the recently-announced **M0+ core** suited to 8-bit replacement. The ARM Cortex-M0+ core offers **improved performance**, **energy efficiency** and **ease-of-use** in comparison to the Cortex-M0, but retains full compatibility with all other Cortex-M class cores enabling reuse of existing compiler and debug tools. The material will cover improvements in the **GPIO handling capability**, increases in **performance** over the existing M0 core, and the sophisticated **Micro Trace Buffer** trace capability. All this is achieved whilst extending ARM's **industry leading low power** performance with a quoted dynamic power of 11uW/MHz.

ARM

Cortex-M Processor Series



Semiconductor vendor MCU announcement dates

Cortex-M Processor Series: *compared*

ARM Cortex-M	SysTick	Bit Banding	MPU	Pipeline
M0	Optional	No	No	3
M0+	**Yes**	**No**	**Optional**	**2**
M3	Yes	Optional	Optional	3
M4	**Yes**	**Optional***	**Optional***	**3**

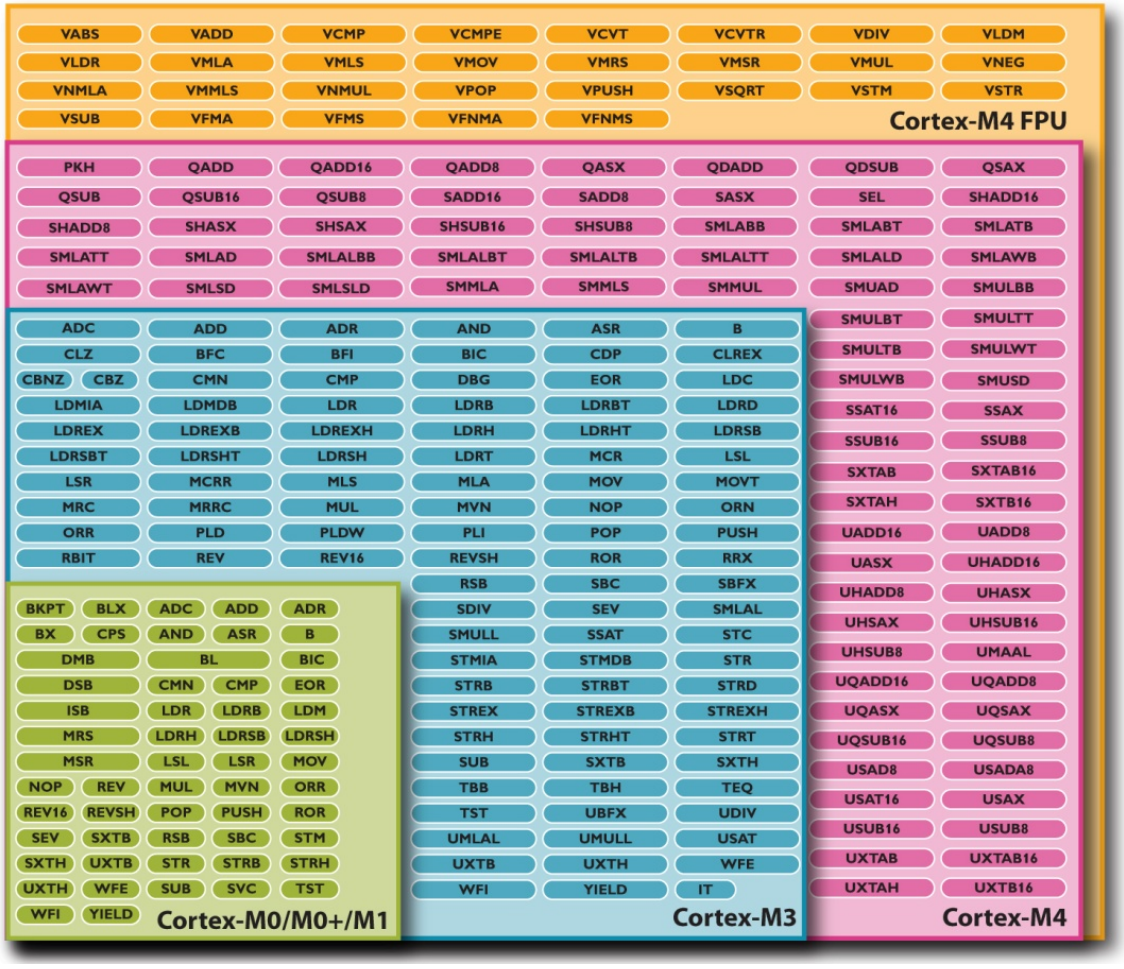
ARM Cortex-M	Thumb	Thumb 2	Mul (Cycle)	Div	Sat.	DSP	FPU
M0	Most	Subset	1/32	No	No	No	No
M0+	**Most**	**Subset**	**1*/32**	**No**	**No**	**No**	**No**
M3	All	All	1	Yes	Yes	No	No
M4	**All**	**All**	**1**	**Yes**	**Yes**	**Yes**	**Optional***

*Semiconductor vendor Freescale: Yes

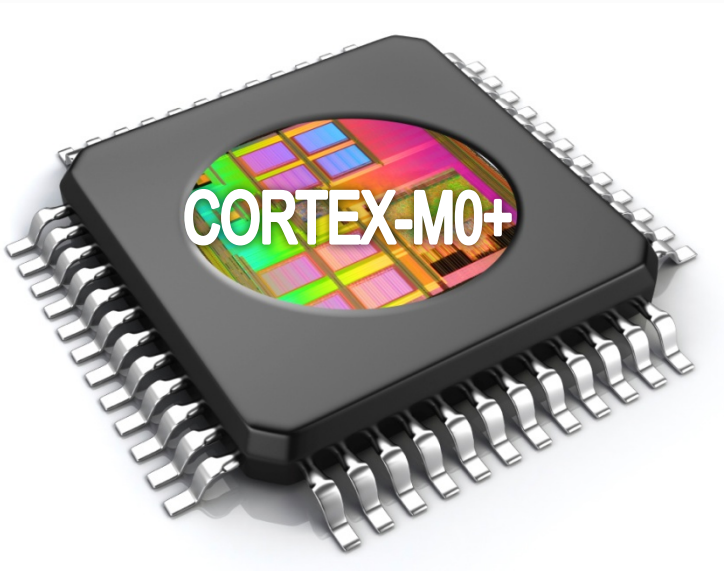
Cortex-M Processor Series: *compared*

Cortex-M0+

- 56 Instructions
- Mostly 16-bit
- Operate on 32-bit registers
- Optional fast MUL (32x32 in 1 cycle)



Cortex-M0+ *The solution for entry-level 32-bit*



EASE OF USE

ENERGY EFFICIENCY

LOW COST

PERFORMANCE

ECOSYSTEM

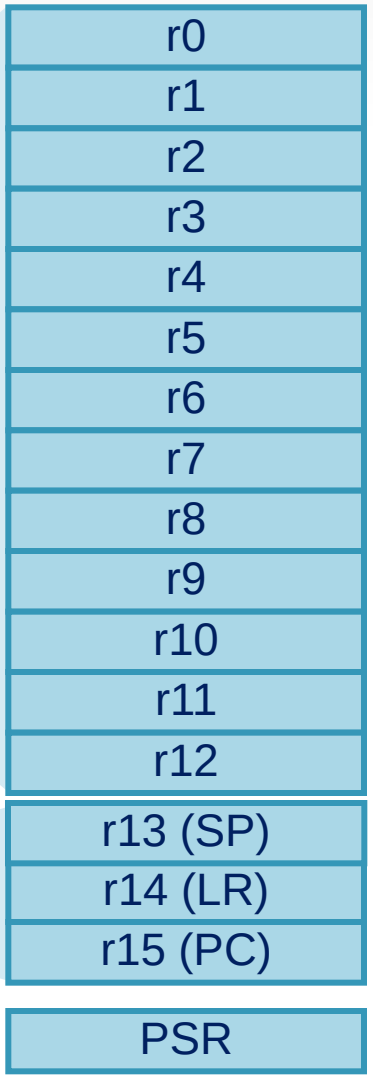
SCALABILITY

Simple Set of Program Registers

EASE OF USE

- **All registers are 32-bit wide**
- **13 general purpose registers**
- **Only 3 special registers**
- **Program Status Register**

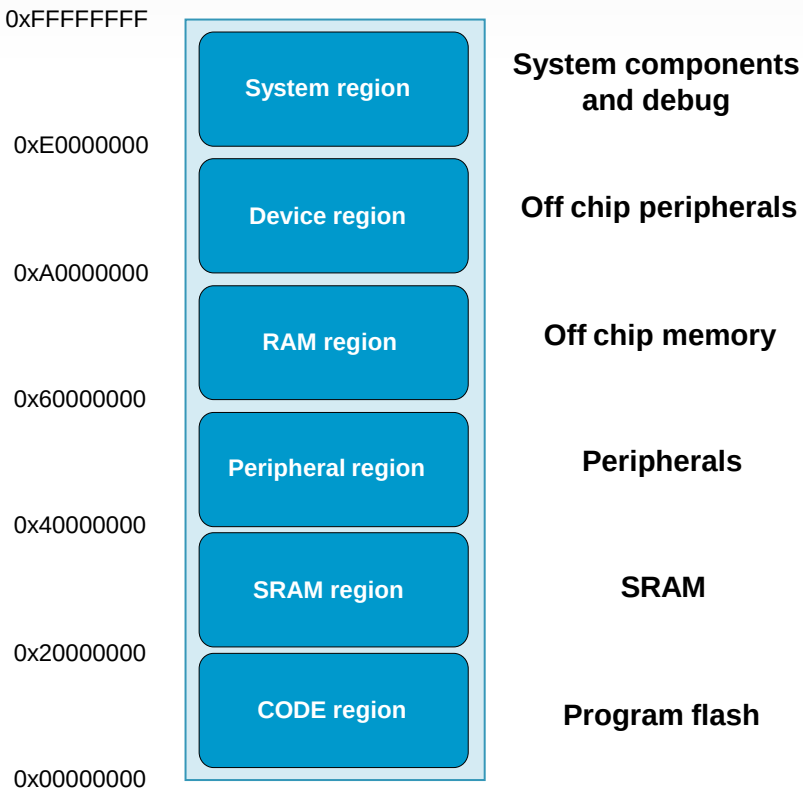
Compared with 8-bit:
- Less stacking
- Faster function calls
- Globals optimisation



Straightforward Memory Map

EASE OF USE

- 4GB linear memory
- No paging/banking
- All locations always accessible by the SW



- Standard across all Cortex-M implementations
- Cortex-M0+ offers an optional MPU

Straightforward Memory Map

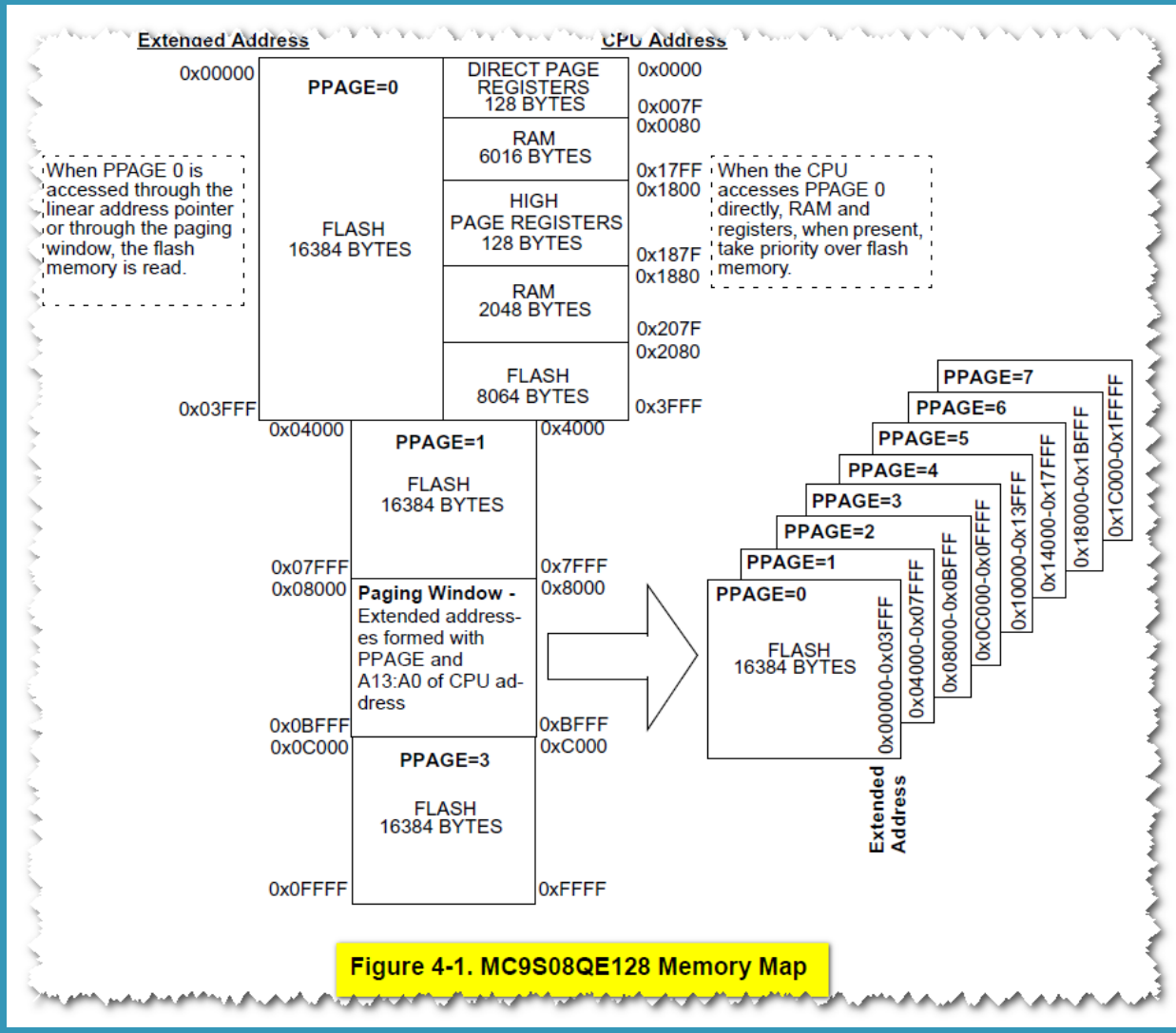


Figure 4-1. MC9S08QE128 Memory Map

32-bit?? What about code density??

EASE OF USE

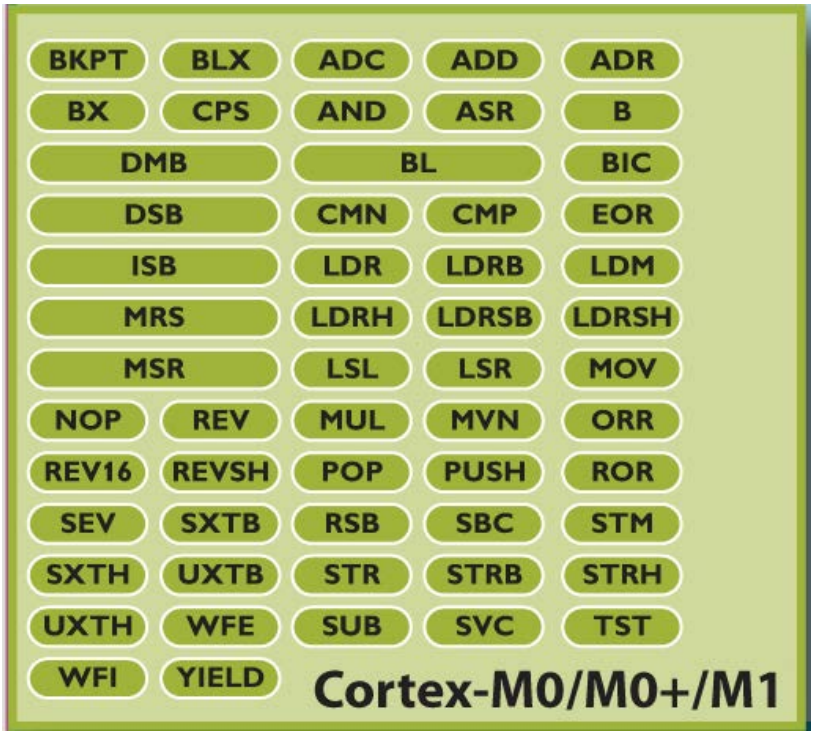
- 32-bit *data*
- 16-bit ***instructions***
- Example - MOV
- HCS08 Architecture (3)

Source Form		Addr. Mode	Machine Code		HCS08 Cycles
			Opcode	Operand(s)	
MOV	*oprr8a,oprr8a*	DIR/DIR	4E	dd dd	5

- Cortex-M0+ (2)

MOV<c> <Rd>,<Rm>

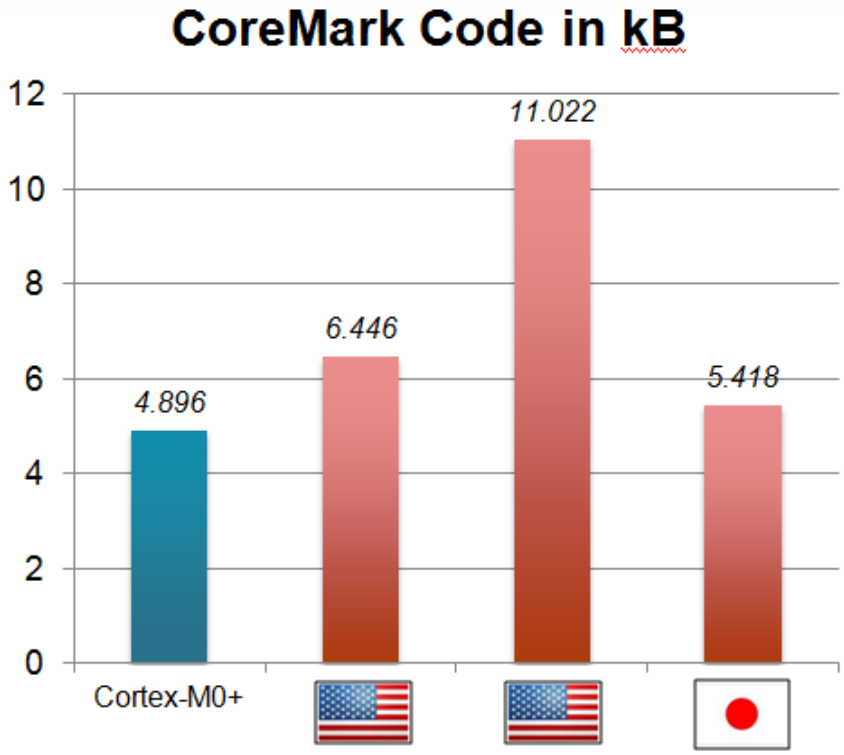
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	0	D	Rm				Rd		



Size optimized solution

LOW COST

- **Best in class code density, reducing flash size needed**
- **Smaller flash size:**
  - Optimized cost
  - Lower MCU power consumption

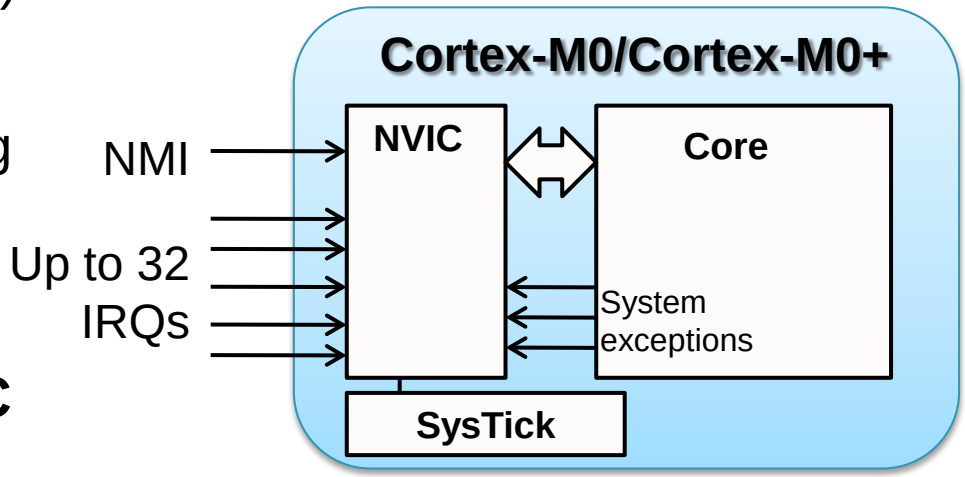


CoreMark code compiled optimized for size
A, B, C & D - low power MCU from global vendors
Smaller number is better

Embedded Systems are all about Interrupts

EASE OF USE

- **Nested Vectored Interrupt Controller (NVIC)**
  - Interrupt prioritisation (4*)
  - Interrupt masking
  - Nested interrupt handling



- **Interrupt handlers in C**
- **Processor handles stacking**
  - r0-r3, r12 Registers
  - Program Counter, Link-Register and PSR

Interrupt Service Routine starts after 15/16 cycles

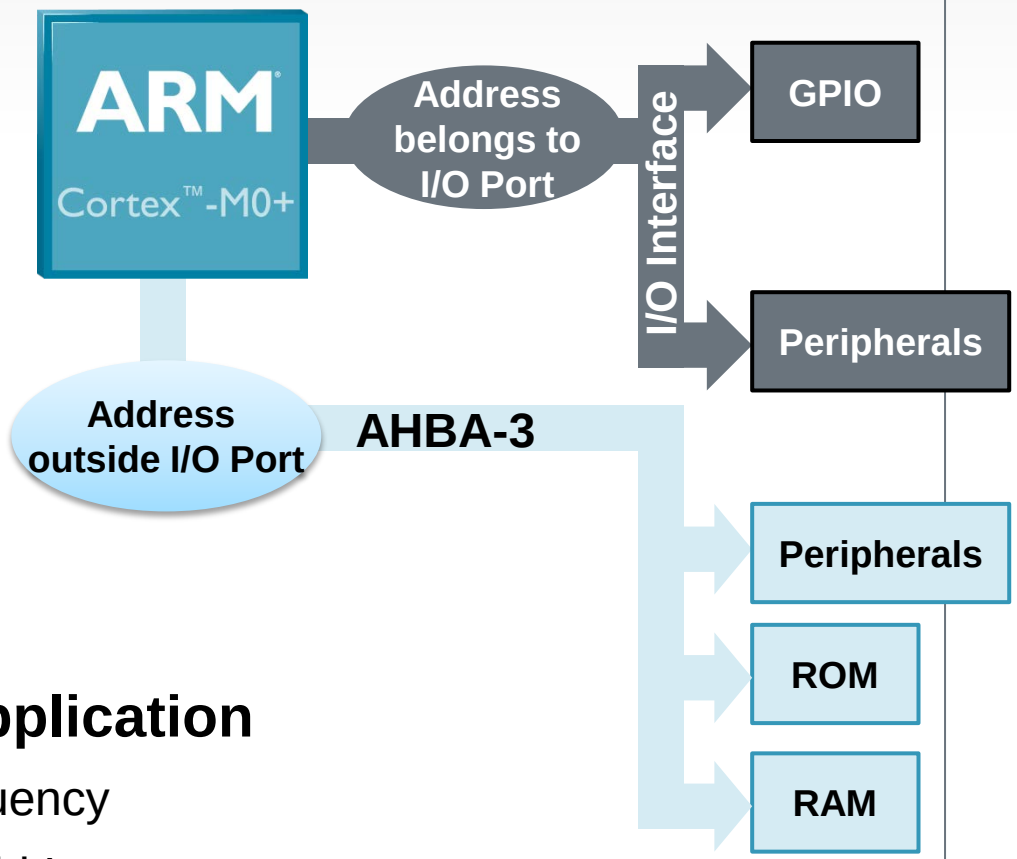
Optimizations: tail-chaining & late arrival

*Semiconductor vendor Freescale

Easy and fast I/O control

EASE OF USE

- **I/O Port**
  - 32-bit wide
  - ***Single cycle access***
  - Best suited for accessing
    - GPIO
    - Peripheral registers
  - Optional Feature

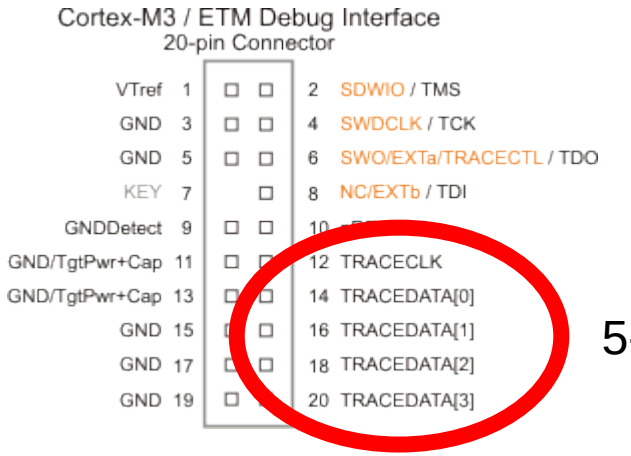


- **Advantages for the application**
  - Higher GPIO toggling frequency
  - Bit-bang the I/O as on a 8-bit!
  - Save precious cycles, e.g. set faster peripherals for low-power
  - “Harvard-like”: access GPIO while processor fetches next instruction

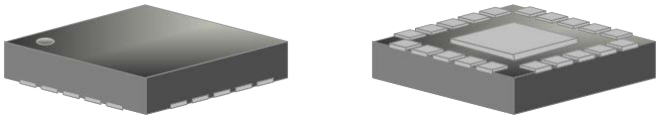
CoreSight™ Micro Trace Buffer (MTB)

EASE OF USE

- **How to bring Trace capability to low-end devices??**



5-pin synchronous mode



*QFN24 (4x4mm)**

- **2-pin Serial Wire Debug (SWD)**
  - SWD_CLK (available on JTAG_CLK pin)
  - SWD_DIO (available on JTAG_MS pin)
- **2-pin cJTAG**
  - JTAG_CLK
  - JTAG_MS

CoreSight™ Debug & Trace IP by ARM

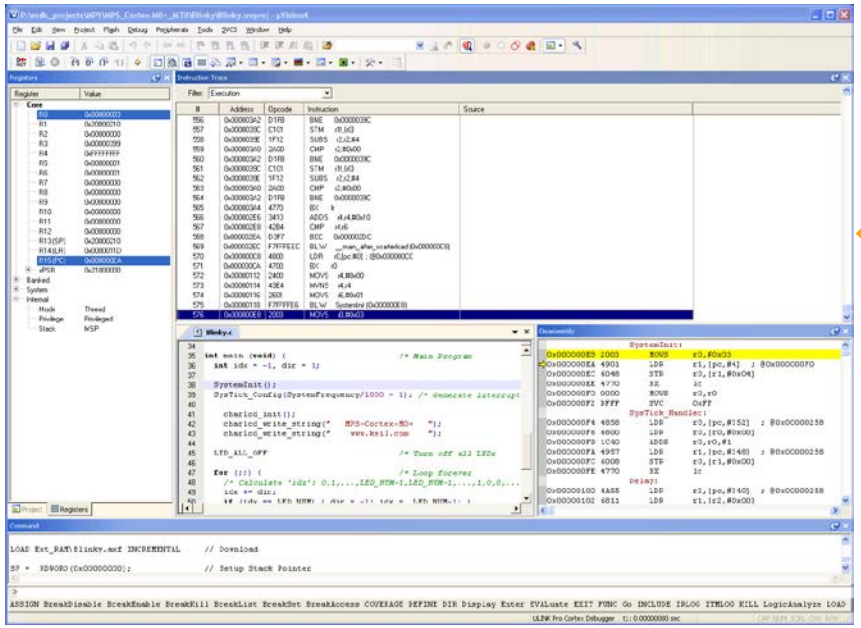
*Semiconductor vendor Freescale

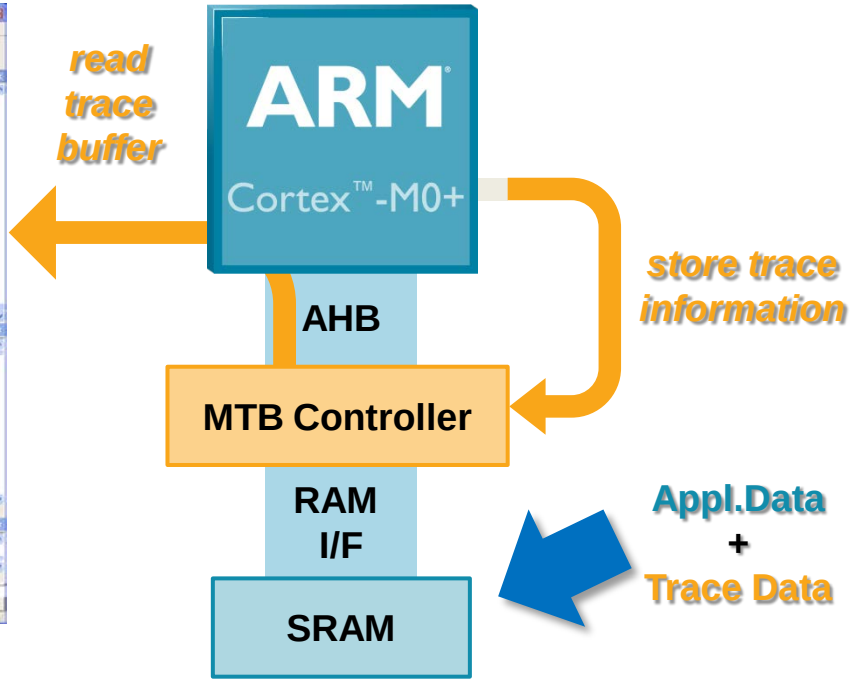
CoreSight™ Micro Trace Buffer (MTB)

- Only 1.5kGate additional
- Trace stored in RAM (non intrusive)
- Read over Serial Wire Debug* (CPU stopped)

CoreSight™ Debug & Trace IP by ARM

E A S E O F U S E





- **Bring fast debug advantages of trace to low-end devices**

*Semiconductor vendor Freescale

Dynamic Power Consumption

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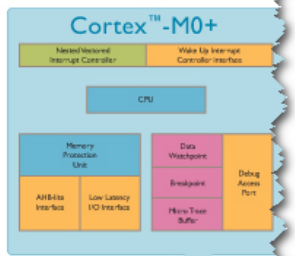
Cortex-M0+ Processor

The ARM Cortex™-M0+ processor is the most energy efficient ARM processor available. It builds on the very successful Cortex-M0 processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Along with the Cortex-M0 processor, the exceptionally small silicon area, low power and minimal code footprint of these processors enable developers to achieve 32-bit performance at an 8-bit price point, bypassing the step to 16-bit devices. The Cortex-M0+ processor comes with a wide selection of options to provide flexible development.

Request More Information



(View Larger Cortex-M0+ Processor Ima

Why Cortex-M0+? | Specifications | Technology | Moving from 8/16-bit | Resources

» The most energy efficient ARM processor

An optimized architecture with a core pipeline of just two stages, enables the Cortex-M0+ processor to achieve a power consumption of just 11.2uW/MHz (90LP process, minimal configuration), while raising the performance to 1.77 CoreMark/MHz.

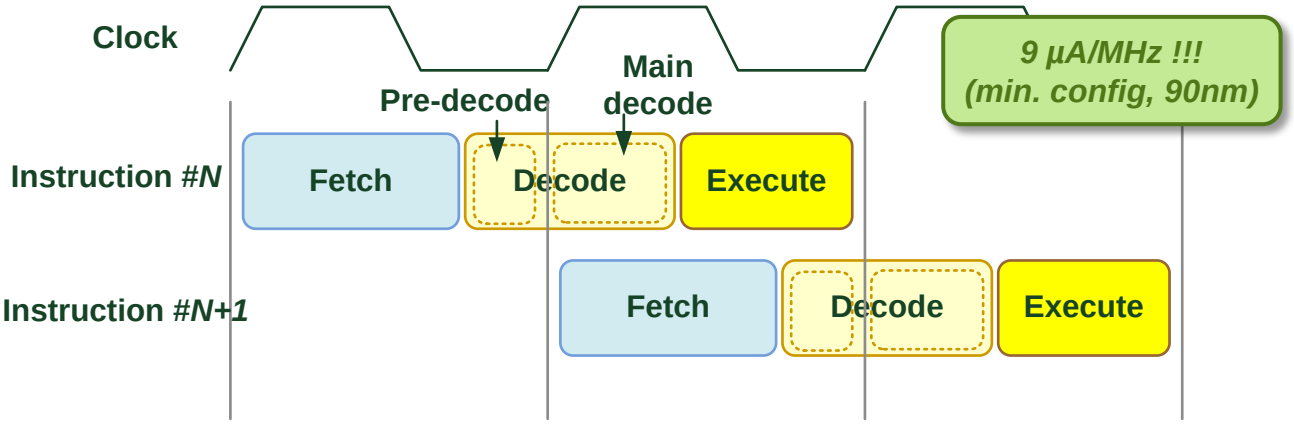
» Simplicity

The Cortex-M0+ processor keeps the same 56 instructions of the Cortex-M0 processor, enabling simple and quick developmer The Thumb® instruction set offers an unrivaled code-density while providing access to 32-bit computation performance. The combination of the these features make the Cortex-M0+ processor a natural and cost effective successor to 8/16-bit devices in a wide variety of applications, while retaining tool and binary upwards compatibility with the feature-rich Cortex-M3 and Cortex-

How?? By Cortex-M0+ design

ENERGY

- **2-stage pipeline von Neumann processor (1st time!)**



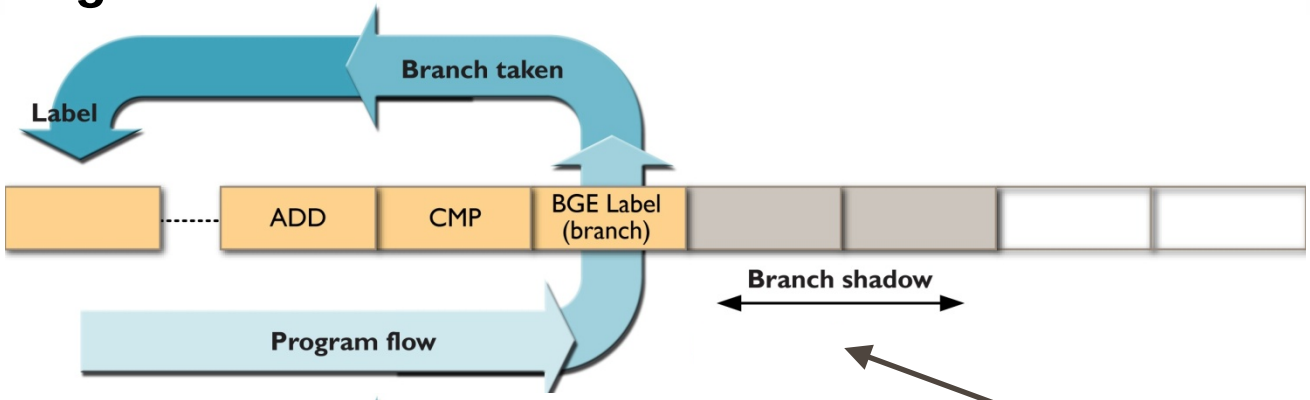
- **Chasing the last µA**
  - Extensive gating of the processor
  - Minimizing flash accesses
- **Save precious run cycles**
  - Faster interrupt entry, faster Branch
  - Faster GPIO & peripheral access

How? Higher efficiency on branch

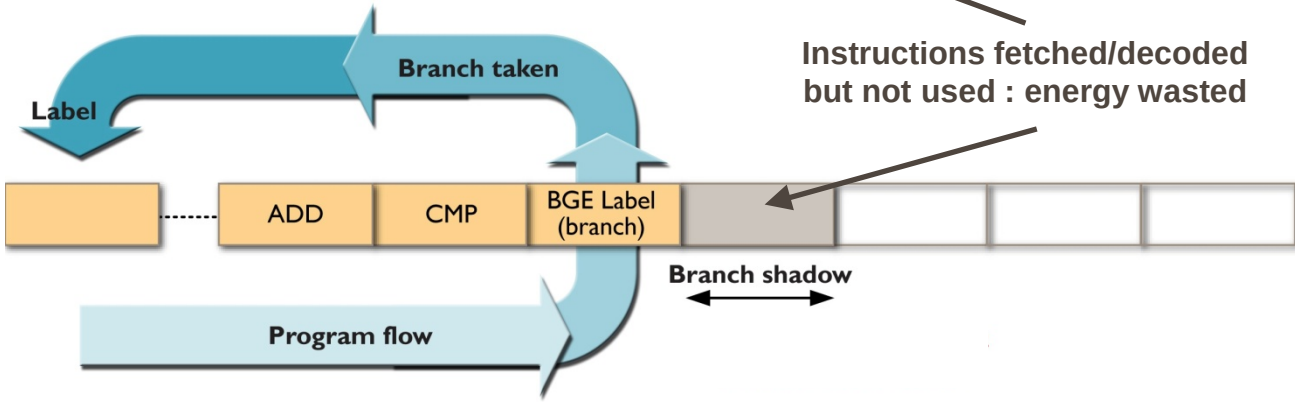
- **In pipelined processors, subsequent instructions are fetched while executing current instructions**

ENERGY

3-stage pipeline



2-stage pipeline

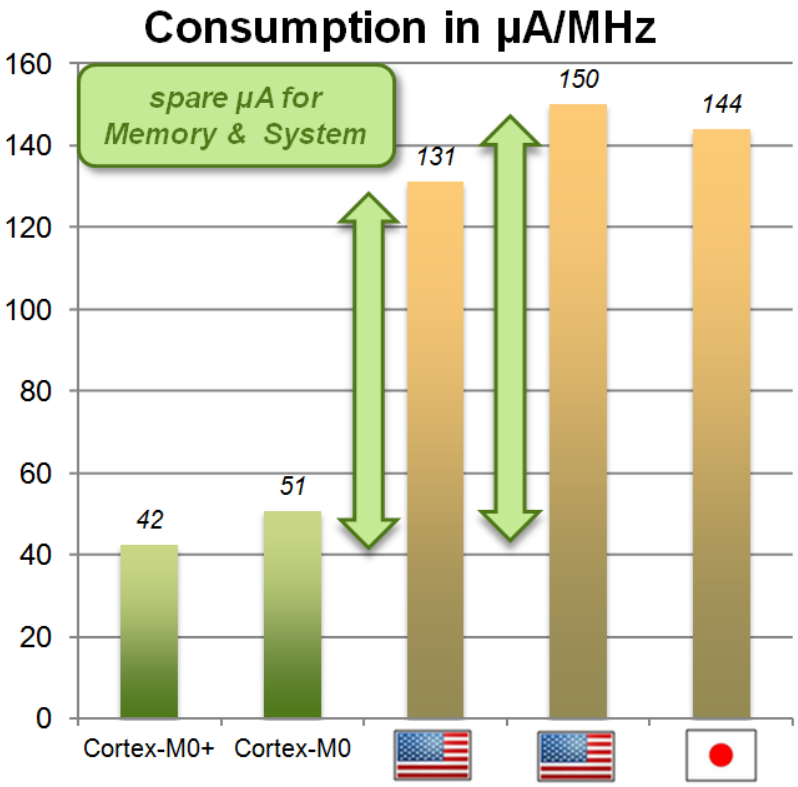


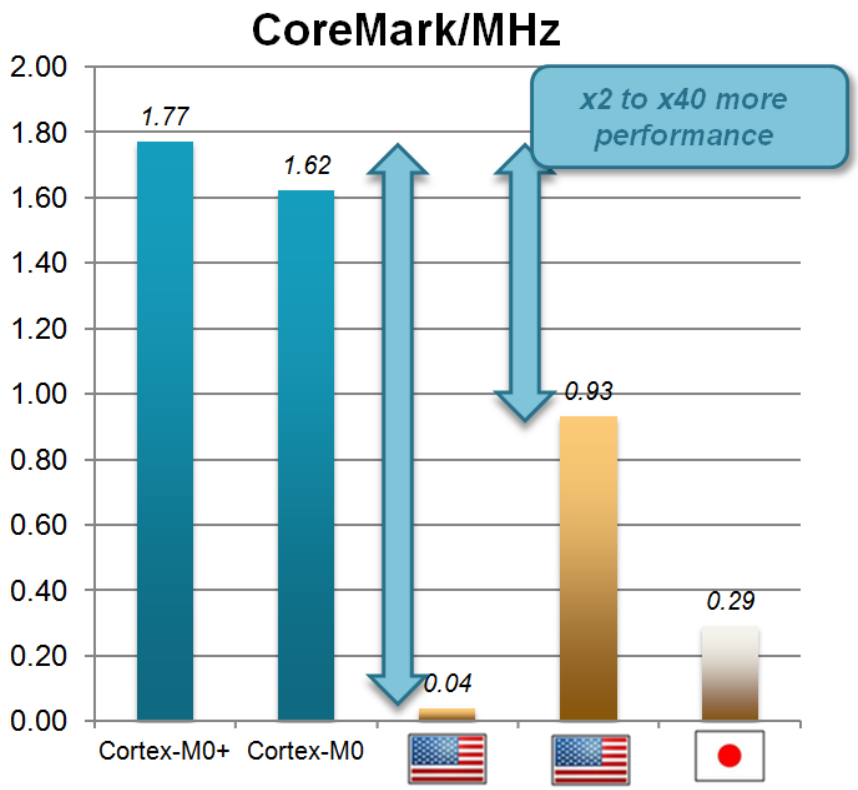
Instructions fetched/decoded but not used : energy wasted

- **In 2-stage pipeline:**
  - Branch shadow is reduced and energy is saved!
  - Branch turn-around is 1 cycle faster!

Dynamic consumption at 8-/16-bit level

- **Enabling to design state-of-the art MCUs**
  - Competitive ultra-low-power: ≥ 90µA/MHz to supply memory and system
  - Quantum leap in performance: at least 2x more performance

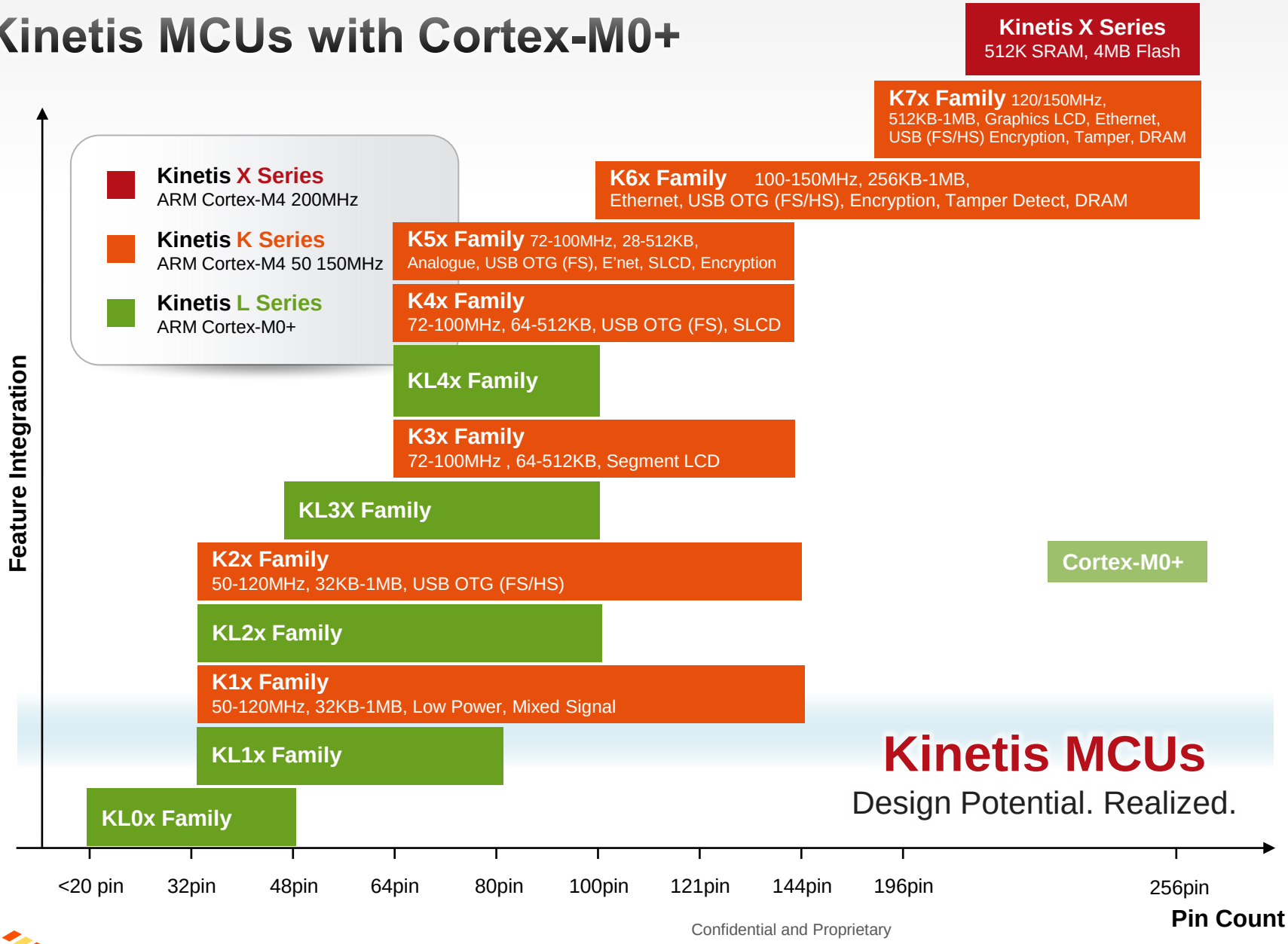




Cortex-M0+: 1.8V, 25C, std configuration, TSMC180ULL, running CoreMark

A, B, C & D: current generation of low-power Flash MCUs, running from Flash in most favourable conditions, ~1.8-2.2V, values from Datasheet/public numbers

Kinetis MCUs with Cortex-M0+



Kinetis MCUs

Design Potential. Realized.