And OR
SOP
POS
OR - AND

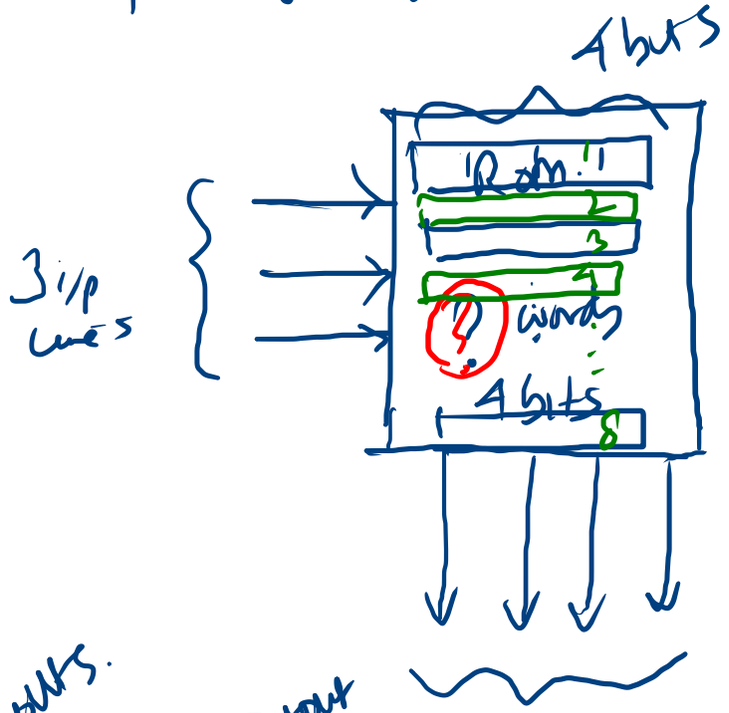
Chapter 3:

Programmable Logic Devices:

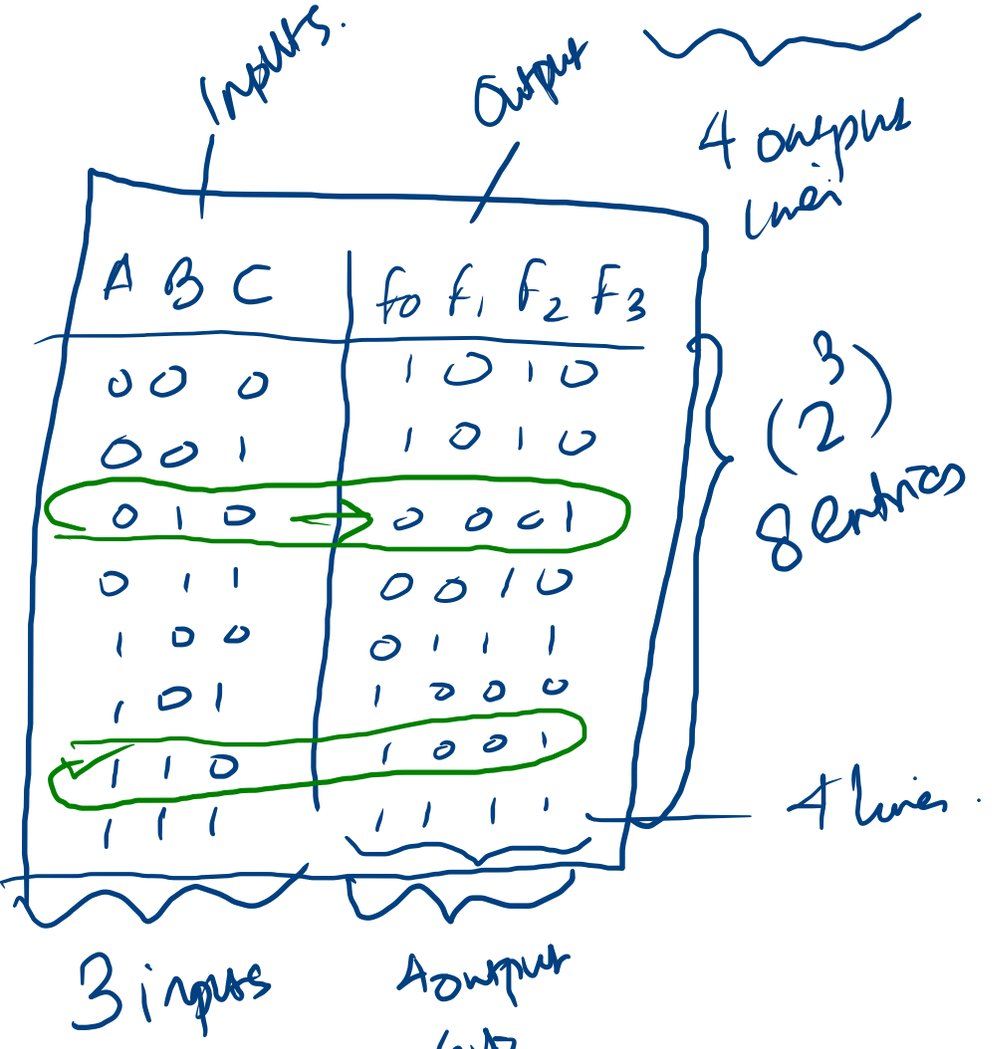
Programmable logic

- Factory Programmable
  - ROM
    - 1970 - 75 A.
    - PROM
      - Prog. ROM.
      - (EEPROM
    - PLA
      - Prog Logic Array
      - AND - OR plane is PLA
      - Both AND & OR plane are programmable
    - MPGA
      - Mask Programmable Gate Array
  - One time programmable
- Field Programmable
  - (Programmable by the designer again & again)
  - SPLD
    - Simple Prog. Logic Device
    - (few 100 gates)
    - Timing - Low
    - PAL
      - Programmable Array Logic
      - AND - OR
      - OR - array is fixed.
      - AND - array is programmable.
    - GAL
      - General Array Logic
  - CPLD
    - Complex PLD
    - few 10000 gates
    - Predictable/medium
    - AMD, Cypress, Lattice
  - FPGA
    - (Field Prog. Gate Array)
    - 1000 - 5 million gates
    - 10-100 million gates
    - Unpredictable
    - Xilinx.
    - Altera

Simple Prog. Logic Device:



A ROM which has n input lines and 'm' output lines contains an array of 2^n words and each word is m bits long.



i/p

010 → ? 0001

110 → ?1001

{ 1. Inputs → mapped to o/p
2 ways to erase our i/p & o/p (Electrical means)

EEPROMs.

Expressed as 2^n x m ROM (n = inputs)

m functions of n variables.

{ 32 words x4 bits →
512K words x 8 bits →

2^n rows & m columns

n = inputs. 3 i/p = 8 rows.

Outputs.

Inputs				Cont S_2	S_1	S_0
A_1	A_0	B_1	B_0	X	Y	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0	1	0	1
1	1	1	1	1	1	0

0
1
5
6

Add these 2 bit numbers

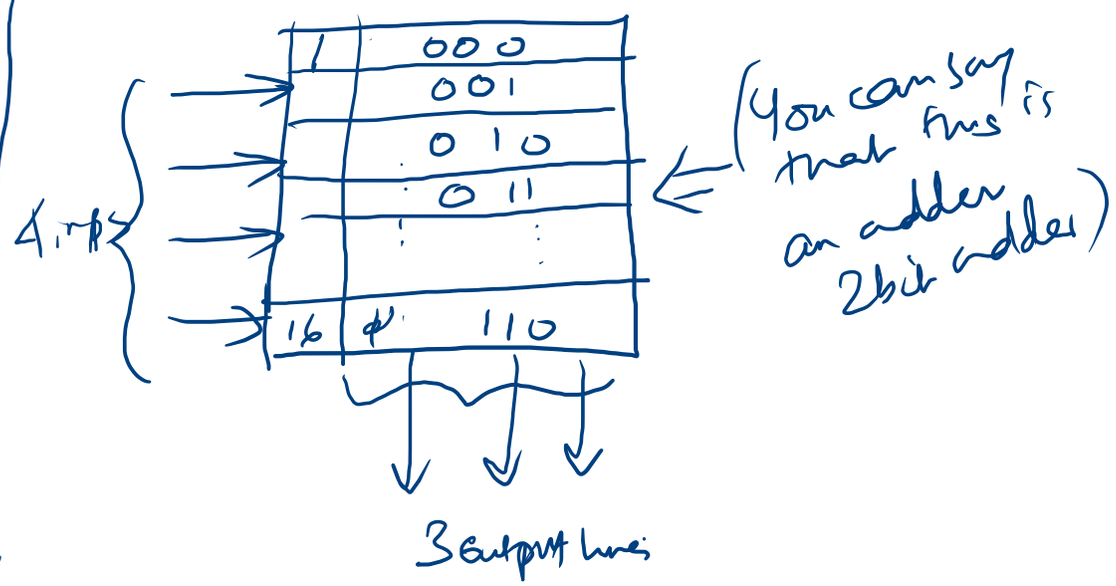
A_1 A_0 + B_1 B_0

Cout Sum1 Sum0

A_1 A_0 + B_1 B_0 = 00 + 00

S: 00 0

S_2 S_1 S_0



Interesting — You can implement ~~any~~ (most) logic functions using ROMs.