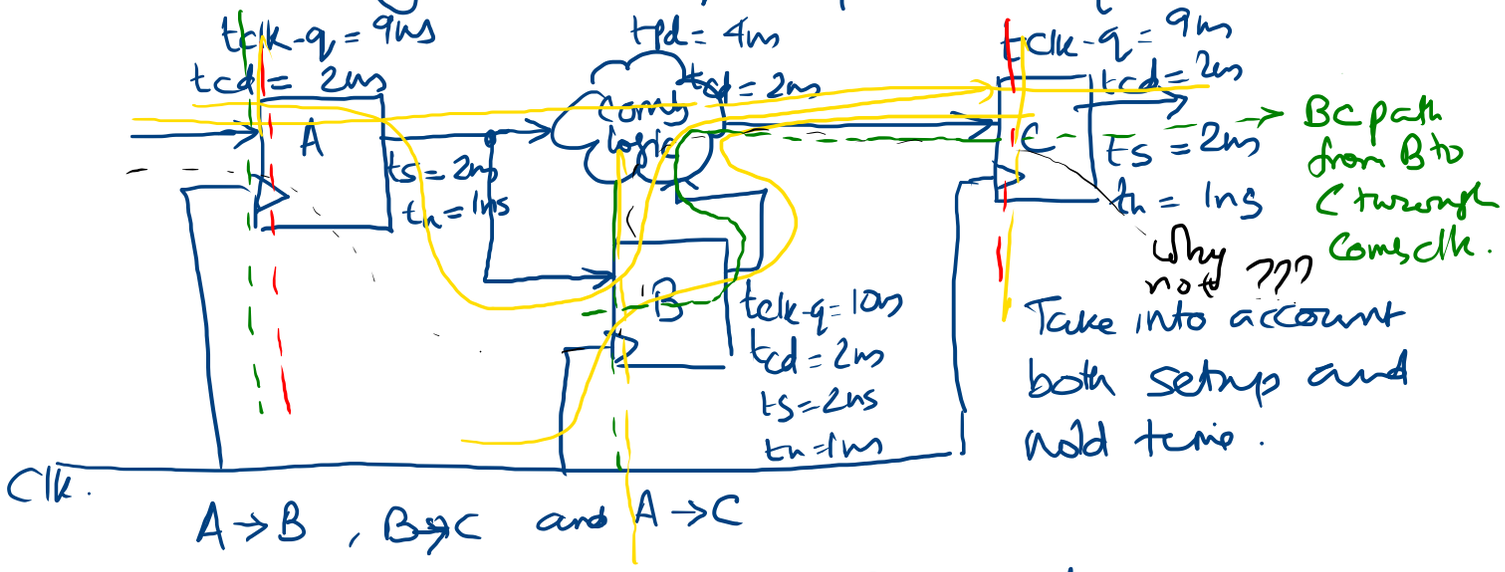
Determining clock frequency of a sequential circuit



A → B , B → C and A → C

$T_{AB} = t_{clk-q(A)} + t_{su(B)} = 9 + 2 = 11$ ns

$T_{AC} = t_{clk-q(A)} + t_{pD(cc)} + t_{su(C)} = 9 + 4 + 2 = 15$ns

$T_{BC} = t_{clk-q(B)} + t_{pD(cc)} + t_{su(C)} = 10 + 4 + 2 = 16$ns

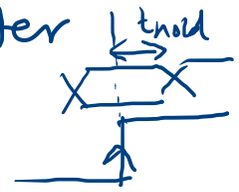
max clk frequency (or $T_{min} = 16$ns) $= \frac{1}{16ns} = 62.5$ MHz

$A \to B \to cc \to C$

Why not ?

Validate FF hold time :-

hold time requirement on FF_B → that the input to B should not change until at least 2 ns after the rising edge of the clk.



$$t_h(B) \leq t_{cd}(A) + t_{cd}(comb)$$

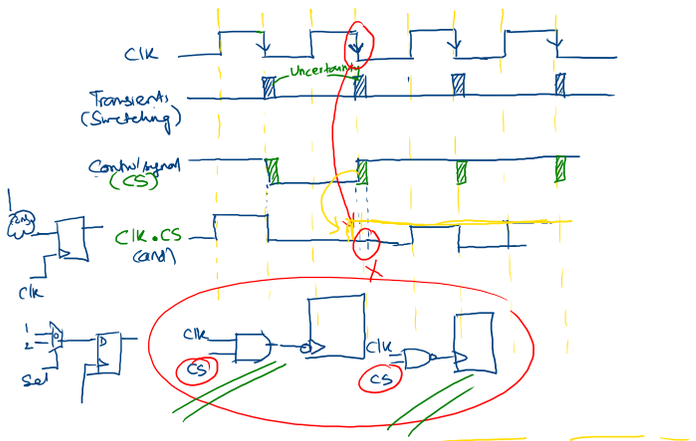
2ns + 2ns.

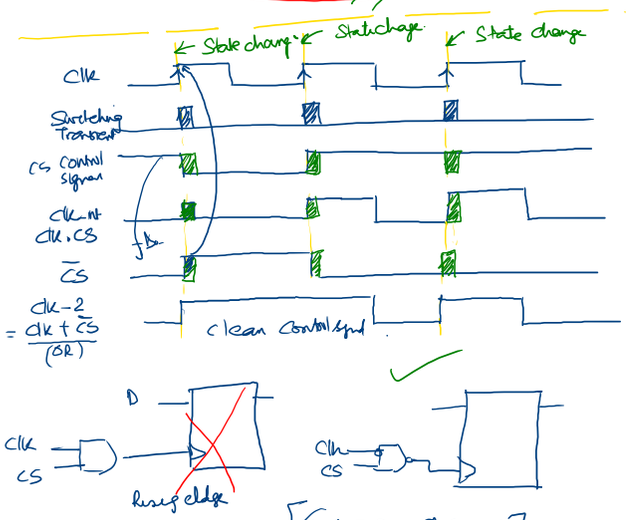
Since t_h (2ns) is less than

2ns $t_h(B) \leq t_{cd}(A)$ [A to B path]

1ns $t_h(C) \leq t_{cd}(A) + t_{cd}(comb)$ [A to C path] (2+2 = 4ns)

1ns $t_h(C) \leq t_{cd}(B) + t_{cd}(comb)$ [B to C path] (2ns + 2ns)





[GATED CLOCKS]

Principles [Synchronous Design]

1. All clock i/p to the ffs, regs, are driven by clk or a derivative clk (ended clk with control signal)
2. All state changes occur immediately following the active edge of the clk (setup, hold time has to be taken care of)
3. Advantages of such a design style (synchronous) all transients, noise and other inconsistency of data that occurs between the clk will have no effect on the system performance and functionality.