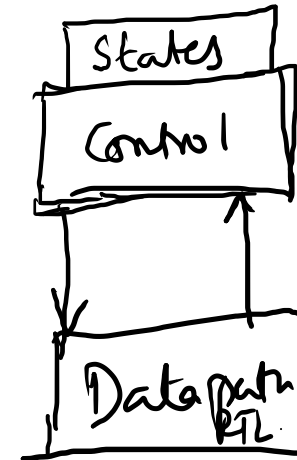
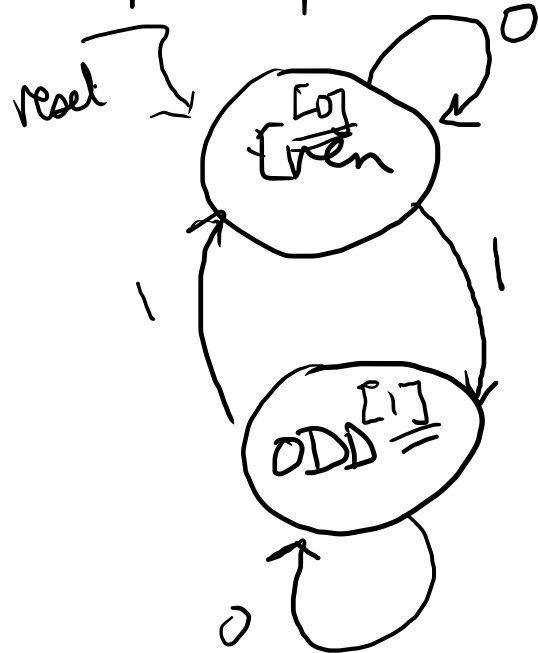


# FSMS:

1. Design the problem with simple words.
2. Encode binary (similar) value to the states
3. State Table
4. K-maps for expressions
5. Logic diagram



Odd parity checker:  $\leftarrow$   $QD \leftarrow$  no of ones is odd then you signal '1' as a flag. otherwise 0.



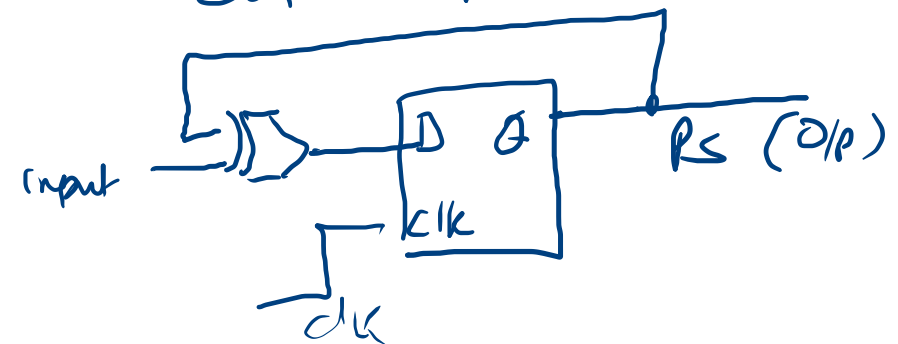
PS	PS	Input	NS	O/p
0	Even	0	Even 0	0
0	Even	1	Odd 1	0
1	Odd	0	Odd 1	1
1	Odd	1	Even 0	1

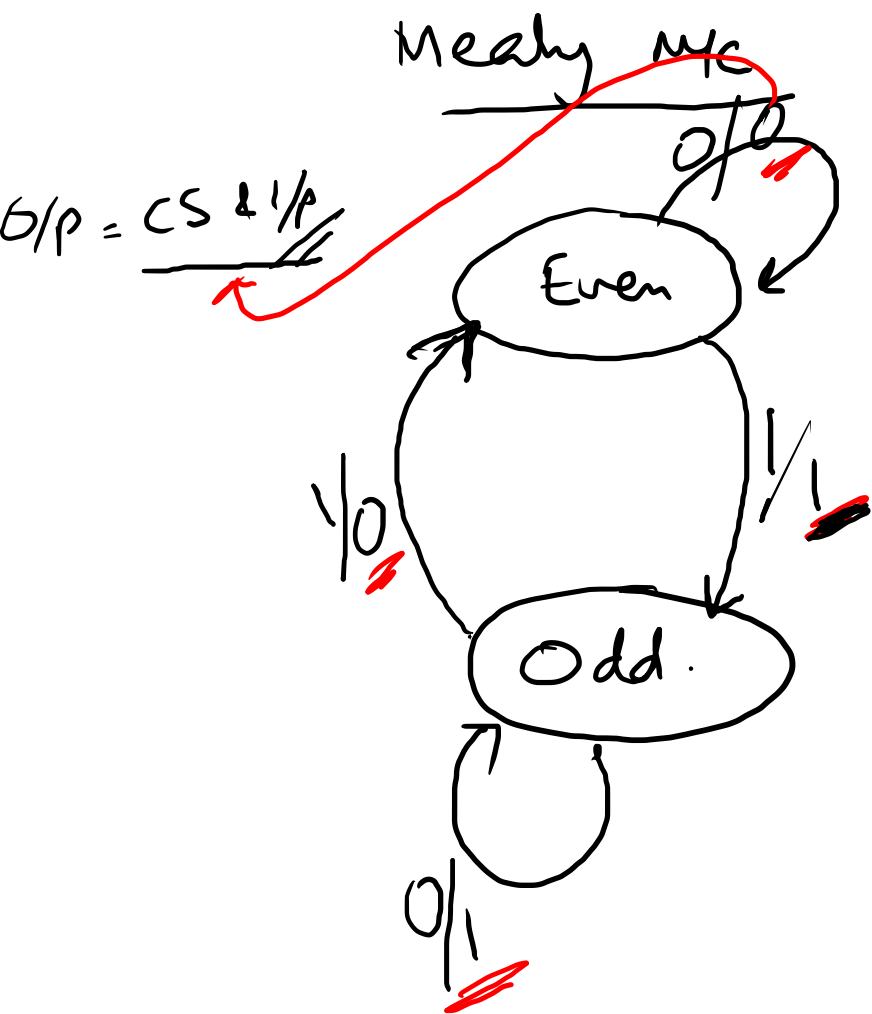
Even = 0  
Odd = 1 } Encode these States as 0 and 1

NS Equations

$$NS = PS \oplus \text{Input}$$

$$\text{Out} = PS$$





Edge Detector  $\rightarrow$  L to R

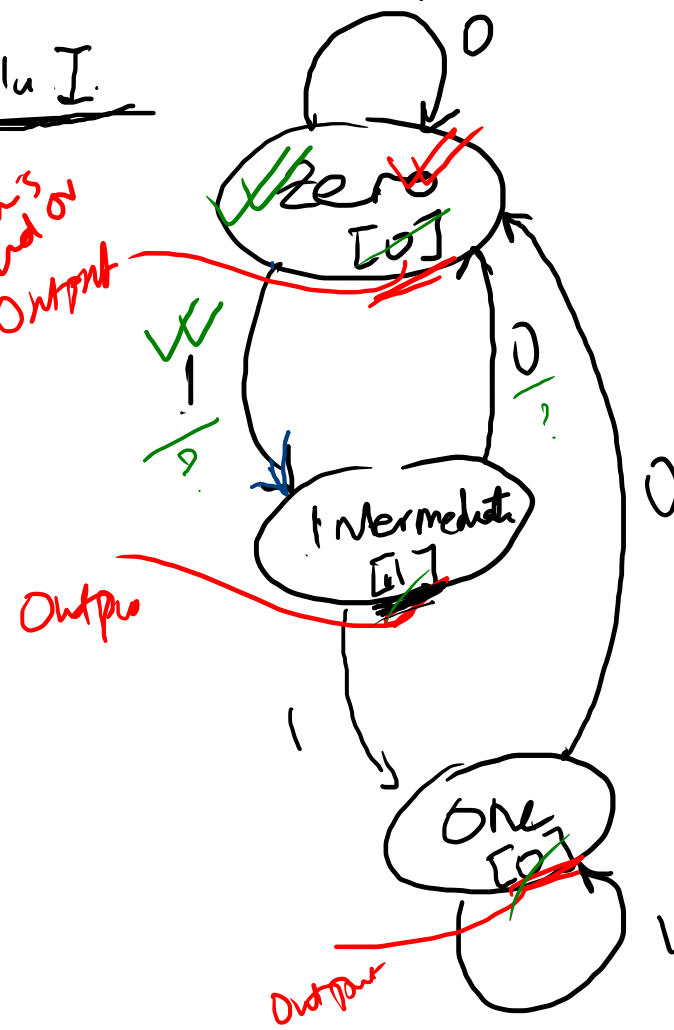
00010101100

O/p is 1 if the i/p bitstream changes from 0 to 1.

Solu I.

Output in this is 1 and 0 is output

Use 1 in the state.



In	PS	NS	D/P
0	Zero 00	Zero 00	0
1	Zero 00	Int 01	0 1 state
0	Int 01	Zero 00	1 0 Encode
1	Int 01	One 11	1 0
0	One 11	Zero 00	0 11
1	One 11	One 11	0

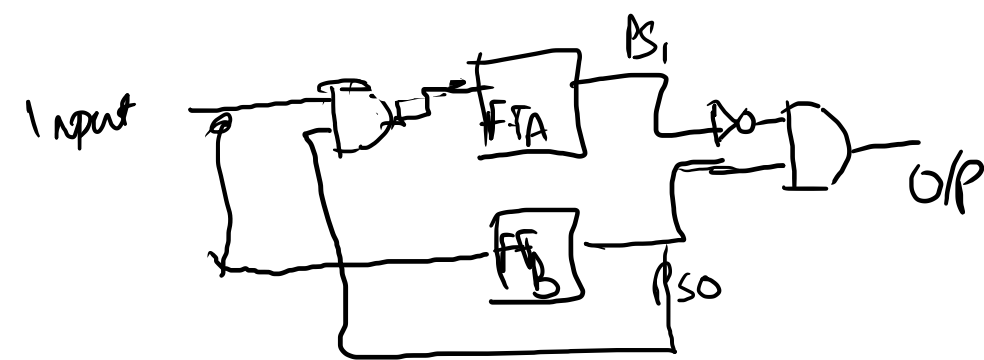
$$A = In \cdot PS_0$$

$$B = In$$

$$O/p = \overline{PS_1} \cdot PS_0$$

This can be derived from the K-maps.

1  $\rightarrow$  0





Soln I.

Soln II.

Soln II.

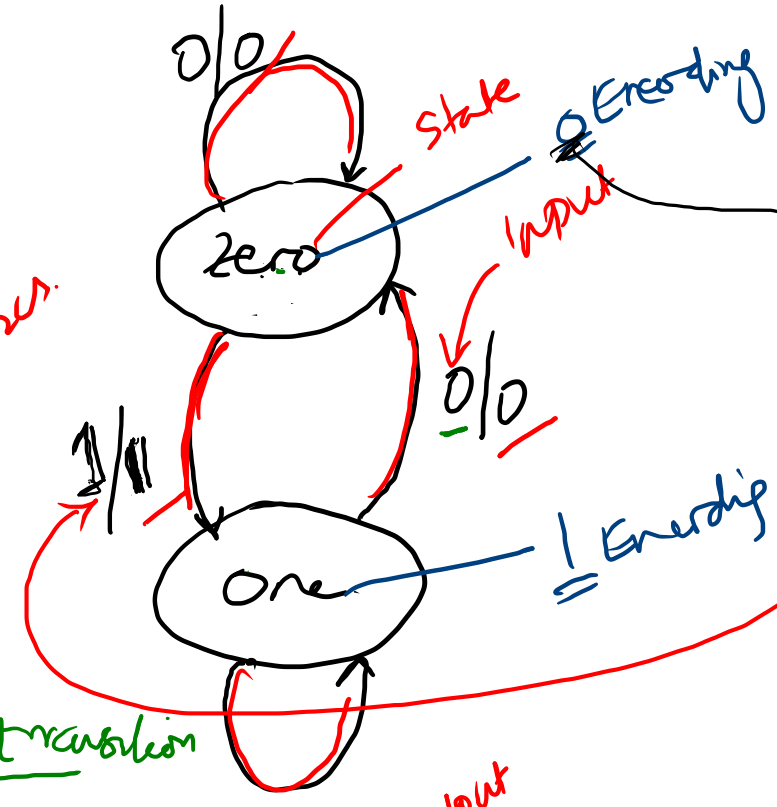
Moore  
more states  
Synchronous  
outputs  
( $O/P = f(\text{state})$ )

have NO glitches  
or erroneous O/P for  
a small amount of time

Mealy  
less states  
this case, the  
output is on the  
transition lines/edges.  
glitches due to  
I/P changes  
& the  
sync. states.

0 → 1 transition

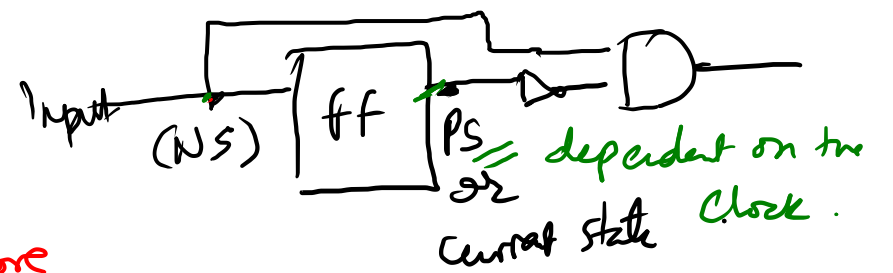
1 → 0 transition  
from state one to zero



In	PS	NS	output
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	0

$$NS = I/P$$

$$\text{Output} = \text{Input} \cdot PS$$

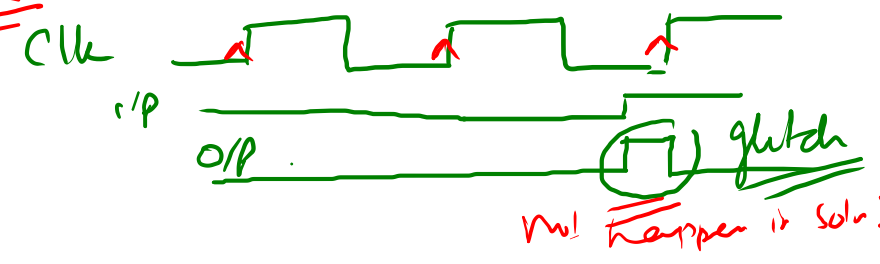


Soln I:

Soln II.

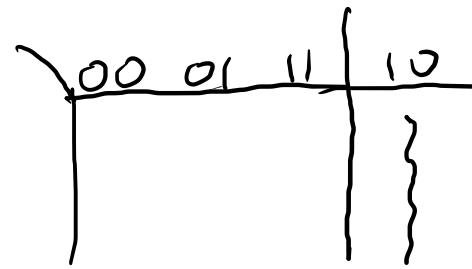
S

In mealy



Zero 00

Int. 01  
One 11



State Reduction: (Result in fewer gates / fewer flipflops)

PS	NS		OP
	A=0	A=1	
S0	S0	S1	0
S1	S1	S2	1
S2	S2	S1	0

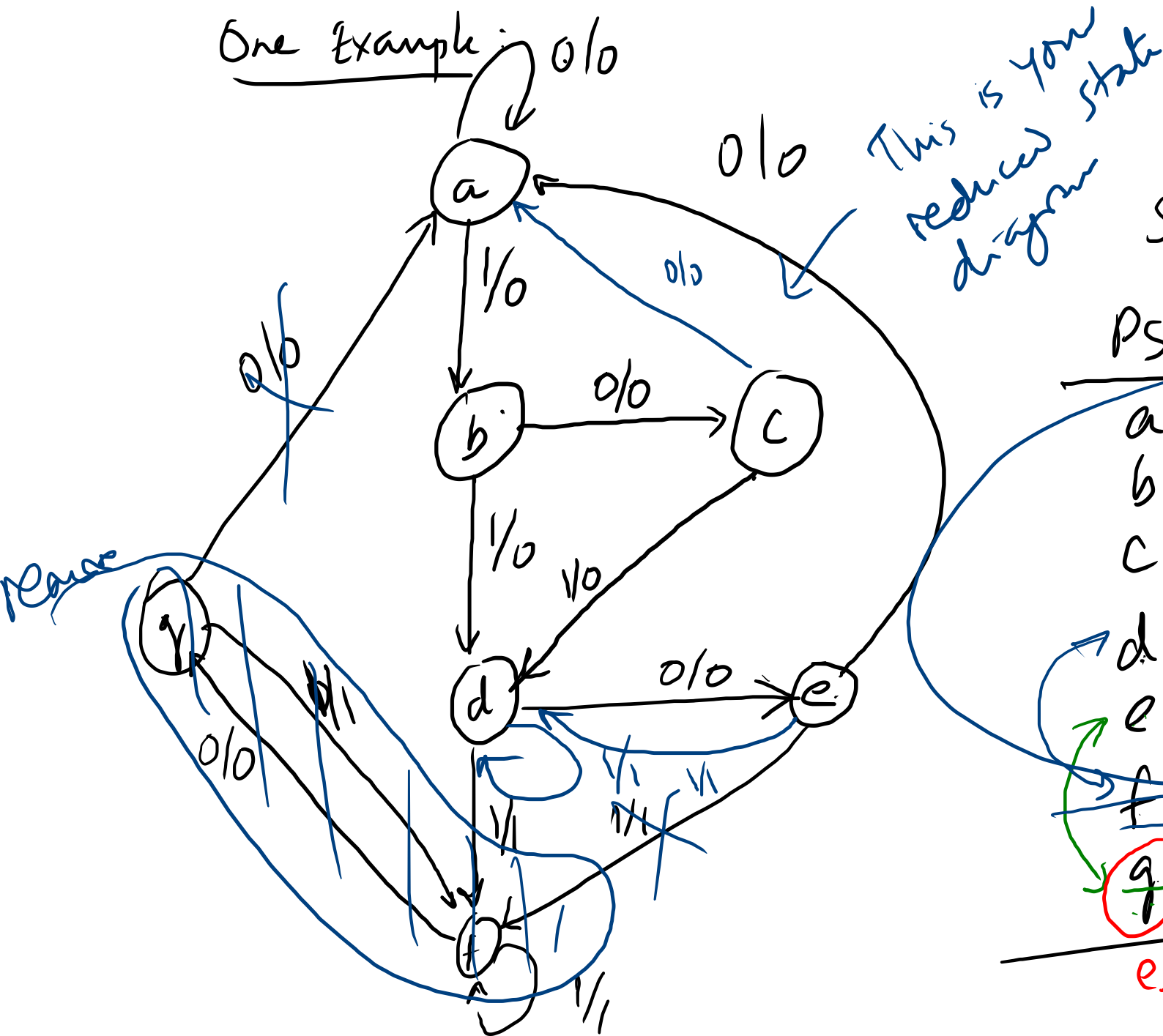
→ we will do a row matching in the State table

→ In two states if the 2 states have same OP & transitions are same to and

- they go to the ~~same~~ same next State.
- or both self loop
- or both transition to each other then

they are EQUIVALENT. (Very close to FPI)

One Example:



State Transition table

PS	NS		Output	
	input=0	input=1	in=0	in=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	<del>a</del>	<del>f</del>	0	1
g	a	f	0	1

*Reduced state table*