VIT
Vellore Institute of Technology

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING

Continuous Assessment Test - II, April 2024

Winter Semester 2023-2024

Course Name & Code: Computer Architecture and Organization, BCSE205L

Programme: B.Tech **Class Number(s): Common to all** **Slot: D1+TD1**

Duration: 90 mins **Max Marks: 50**

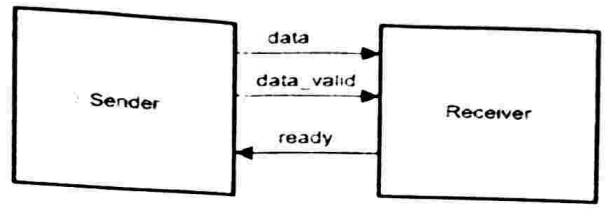
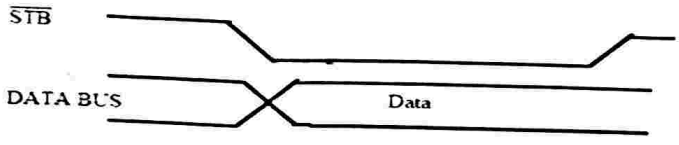
Sl. No	Question	Max. Mark
1	**a)** A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:	10

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program. 1.55 ~~258~~ 25.8 0.003875 (5 marks)

b) Differentiate between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory? Justify using appropriate block diagrams. (5 marks)

2	Suppose that a 2M × 16 RAM memory is built using 256K × 8 RAM chips and 1K x 8 ROM memory is build using 256 x 8 ROM chips with the word addressable memory, find the following: a) How many RAM chips and ROM chips are necessary? 16 , 4 b) If we were accessing one full word in RAM, how many chips would be involved? 2 c) How many address bits are needed for each RAM chip? 22 d) How many memory banks are required in RAM? *Hint: Numbers of banks are addressable units in main memory.* 21 e) If high-order interleaving is used in RAM chip, where would address $(1B)_{16}$ be located? Also, for a low-order interleaving?	10
3	**a)** Consider a 32-bit microprocessor that has an on-chip 16-kB four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Identify the set number in cache for mapping the given memory address ABCDE8F8. (5 marks)	10

	b) Given a page reference string: 1.2.3.4.2.1.5.6.2.1.2.3.7.6.3.2.1.2.3.6. Assume cache line size = 4. Calculate the hit ratio & miss ratio for LRU replacement algorithm. (5 marks)	
4	**a)** The processor needs to transfer a file of 29154 kilobytes from disk to main memory. The memory is byte addressable. The size of data count register of a DMA controller is 16 bits. Calculate the minimum number of times the DMA controller needs to get the control of system bus from the processor to transfer the complete file from disk to main memory in following modes? (5 marks) i. Cycle stealing mode ii. Block transfer/Burst transfer mode **b)** Identify the type of I/O interfacing from following figures and justify your answer (5 marks) i.  ii.  	
5	**a)** Assume in a program variable *i* has 4-byte value 0x01234567. Address given by &x is 0x100. Draw the internal byte storage representations if program is executed in big endian and little-endian architectures. (5 marks) **b)** i) In memory mapped IO there may not be enough address space to address all the peripheral device. Justify the statement. ii) Suggest and explain the technique to avoid the wastage of CPU burst time. (5 marks)	