VIT
Vellore Institute of Technology

School of Computer Science Engineering and Information Systems

Fall Semester 2023-2024

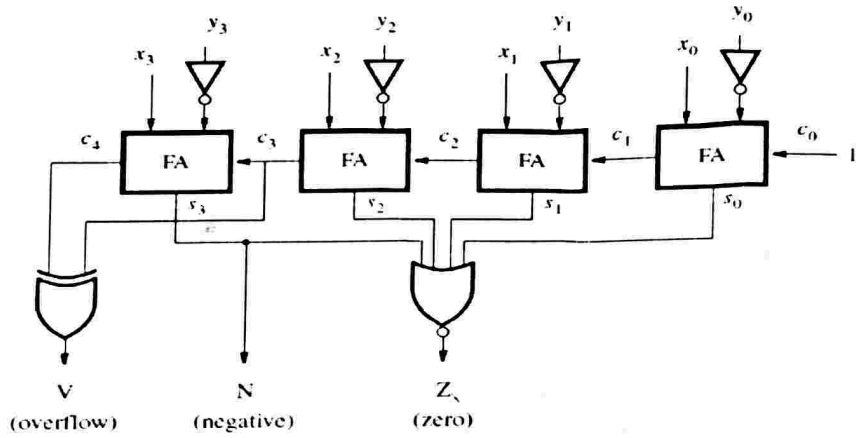
Open Book Exam-Continuous Assessment Test – II

Programme Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE102L & Digital Systems Design **Slot: B1+TB1**

Exam Duration: 90 Min. **Maximum Marks:** 50

Answer all the questions

Q. No.	Question
1	One arithmetic circuit is shown in Figure 1; it contains four 1-bit Full Adders (FA). Write the Verilog code using structural modeling to specify the operation of the arithmetic circuit and also write its test bench. **[10 Marks]** **Note:** The individual FA should be designed by Data flow modeling.  Figure.1
2.	Assume that registers M and Q of the sequential Booth's multiplier are initialized with the values -15 and 10. **[10 Marks]** i. Perform the multiplication operation according to Booth's algorithm. ii. After multiplication, how many subtraction and addition operations will be performed? Write the answer in decimal. iii. Write the logical block diagram that implements the Booth's multiplier. **Note:** Consider M (6 bit) = Multiplicand and Q (6Bit) = Multiplier
3.	A New clocked A-B Flip-Flop is defined with two inputs, A and B, in addition to the clocked input. Refer the table for the flip flop function. **[10 Marks]**

P.T.O.

CLK	A	B	Q_{n+1}
0	×	×	Q_n
↑	0	0	1
↑	0	1	Q_n
↑	1	0	Q_n
↑	1	1	0

$AB + \bar{A}Q(t) + \bar{B}Q(t)$

i. Provide the Characteristics table and Characteristic equation for the A-B flip flop.
ii. Provide the Excitation table and input equations.
iii. Implement the A-B flip flop using a D flip flop.

4. A 4-bit shift register circuit is configured for right-shift operation is D_{in} to Q_1, Q_1 to Q_2, Q_2 to Q_3, Q_3 to Q_4, is shown in Figure. 2. If the present state of the shift register is $Q_1Q_2Q_3Q_4$=0110

i. Write the truth table and timing diagram for 8 number of clock cycles .
ii. Calculate the number of clock cycles required to reach the state $Q_1Q_2Q_3Q_4$=1111
iii. Implement Verilog model of the given diagram **[10 Marks]**

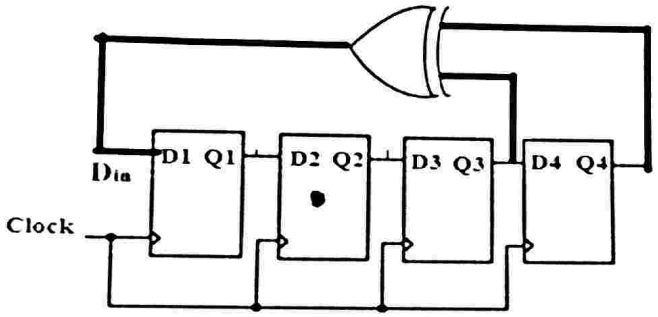


Figure.2

Design a counter for the given sequence as shown in the Figure. 3 using T Flip flops. **[10 Marks]**

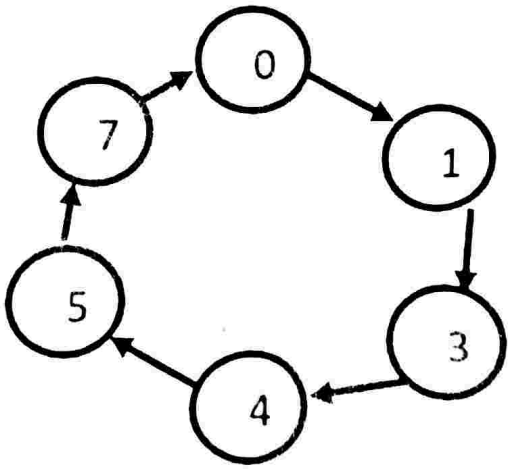


Figure.3