VIT
Vellore Institute of Technology

School of Computer Science Engineering and Information Systems

Fall Semester 2023-2024

Continuous Assessment Test – I

Programme Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE102L & Digital Systems Design **Slot: B1+TB1**

Exam Duration: 90 Min. **Maximum Marks:** 50

Answer all the questions

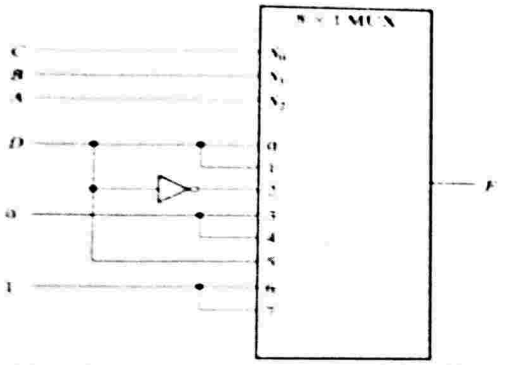
Q. No.	Question	Max Marks	CO	BL
1.	Simplify the Boolean function $F(a,b,c,d) = \pi M\,(0,2,4,6,9,11,13,15)$ using K-map and draw the logical diagram using only NOR gate.	10	CO1	BL3
2.	a) Find the optimized expression in term of SOP and POS for the given function $F(a,b,c,d) = \sum m\,(0,2,5,7,8,10,13,15)$ b) Draw the schematic of optimized SOP function "F" in CMOS logic style.	10	CO1	BL6
3.	a) Execute the following verilog program for the given input a =4'b1010, b = 4'bx101 and compute the output.	10	CO2	BL5

Line	Program
1	module DA (c, d, e, f, g, h, a, b);
2	input [3:0]a, b;
3	output d, h, [3:0] c, d, e, f, g;
4	assign c= a ^ b;
5	assign d = a && b;
6	assign e = ({a[3:2], 2{b[1]}});
7	assign f = ~ a ;
8	assign g = (a ~ ^ b);
9	assign h = (a !== b);
10	endmodule

b) Rewrite the below verilog code in structural modeling and provide the testbench code (with four random test cases) to verify it.

```
module sample (O,s,w,x,y,z);
input [1:0]s;
input w,x,y,z;
output reg O;
always @ (s or w or x or y or z)
begin
case(s)
        2'b00: O = w ;
```

```
            2'b01: O = x;
            2'b10: O = y;
            2'b11: O = z;
        endcase
        end
        endmodule
```

4.	Identify the given Boolean function (F) represented in terms of multiplexer and implement the function (F) using 3 to 8 decoder logic. 	10	CO3	BL6
5.	Design a combinational circuit with less number of logic gates for the following truth table and write the dataflow modeling in verilog HDL for the design.	10	CO3	BL6

Inputs				Outputs			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1