VIT
Vellore Institute of Technology

Final Assessment Test – November/December 2023

Course: BECE102L - Digital Systems Design

Class NBR(s): 4121 / 4125 / 4126 / 4127 / 4128 / 4129 / 4131 / 4132 / 4133 / 4134 / 4135 / 4136 / 4137 / 4138 / 4140 / 4142 / 4144 / 4145 / 4147 / 4148 / 4244 / 4257 / 4261 / 4265 / 4287

Slot: B1+TB1

Time: Three Hours

Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

General Instructions :

1. **Assume suitable values, in case of any missing data.**
2. **Necessary intermediate steps for each solution is mandatory**

Answer ALL Questions

(10 X 10 = 100 Marks)

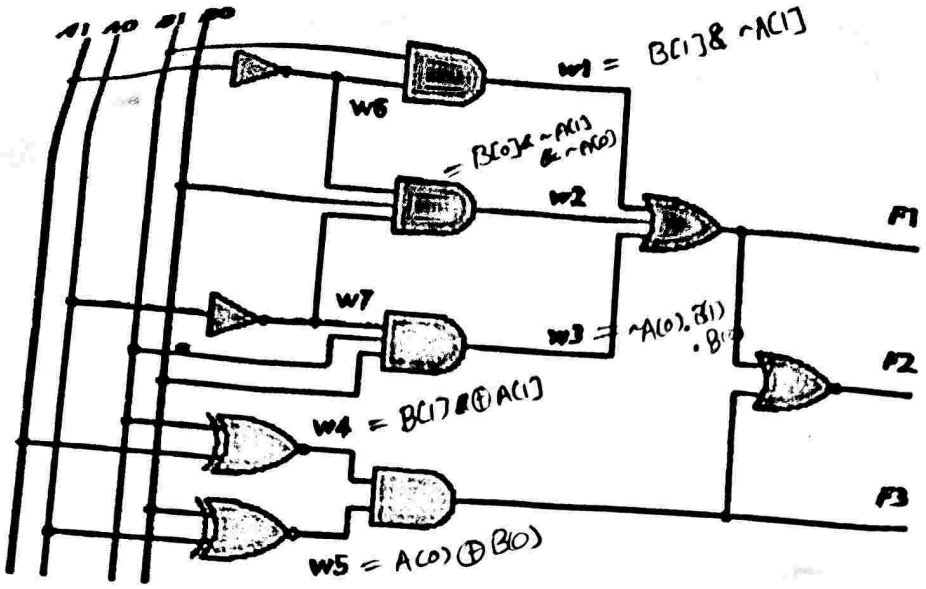
1. Simplify the Boolean function $F = (\bar{A}\bar{B}D + AB)C + \bar{C}$ using K-map and sketch the logic diagram using NAND gates only.

2. Using Boolean algebra and postulates reduce the function $F = \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + BD + BC\bar{D}$. Sketch the CMOS logic style schematic for the simplified function. Assume that both the true and complement version of each input variables are available as gate input.

3. i) Execute the following verilog code for the given input a = 4'b1010, b = 4'b1101 and compute the output Y.

```
module program (a, b, Y);
input [3:0] a, b;
output [4:0] Y;
  assign  Y[0] = ~ (a & b);
  assign  Y[1] = (a[2] > b[0]) && ( a[3] < b[3]);
  assign  Y[2] = (a != = b);
  assign  Y[3] = (a != b) ? 1'b1 : 1'b0;
 assign  Y[4] = (a << 2) + (b >> 1);
endmodule
```

ii) Develop a Verilog code for the logic diagram given below using structural modelling.

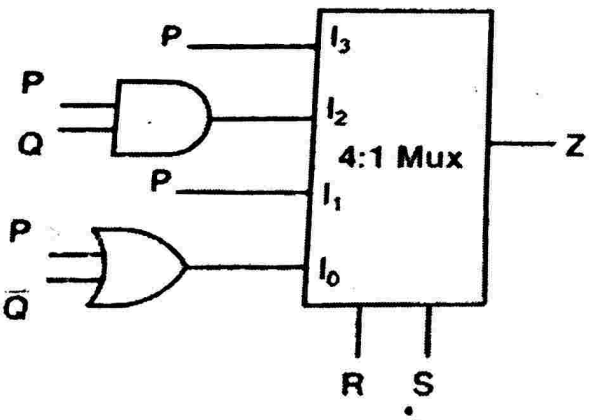


4. The majority circuit is a combinational circuit, whose output is equal to 1 if the input variables have more 1's than 0's, equal to don't care when number of 0's and 1's are equal, otherwise the output is '0'.

   i. Design a 4-input majority circuit by finding the circuit's truth table, Boolean equation, and the logic diagram. $AB + C$

   ii. Using dataflow model construct the verilog code and its testbench to verify it.

5. i) Identify the Boolean function (Z) from the circuit shown below and implement the same with 3x8 decoder.



$P\bar{R}\bar{S} + \bar{Q}RS + P\bar{R}S + P\bar{Q}R\bar{S} + PRS$

ii) Design and implement the circuit using 4x1 multiplexer which has 3 inputs (A, B, C) and one output (Y). The output is low when odd number of 1's are detected in the input, otherwise the output logic '1'. Choose A and C as the select inputs.

6. Develop a Verilog code for the combinational circuit which performs 4-bit addition and subtraction operation based on the control input.

7. A PQ flip-flop has four operations, no change, clear to 0, set 1 and toggle, when inputs P and Q are 01, 00, 11 and 10, respectively.
   (i) Determine the characteristic table of the flip-flop.
   (ii) Find the characteristic Equation of the flip-flop.
   (iii) Determine the excitation table.
   (iv) Convert the flip-flop to a D flip-flop.

8. Using positive edge triggered D flip-flop, design a synchronous counter which counts the following sequence 000, 111, 110, 101, 100, 011, 010, 001, 000.

9. Construct a Mealy based sequence detector to detect a sequence 1101 in overlapping fashion using D flip-flop.

10. Implement the following Boolean function with the programmable logic devices PAL and PLA.
   (i) $A(x,y,z) = \sum m(1, 2, 4, 6)$
   (ii) $B(x,y,z) = \pi M(2, 3, 4, 5)$

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