Multiple Choice Questions on 8086 Microprocessor

1. A microprocessor is a	chip integrating	g all the functions of a	CPU of a computer.
A. multiple	B. single	C. double	D. triple
ANSWER: B			
2. Microprocessor is a/an _	circuit that fur	nctions as the CPU of t	he compute
A. electronic	B. mechanic	C. integrating	D. processing
ANSWER: A			
3. Microprocessor is the	of the computer	and it perform all the o	computational tasks
A. main	B. heart	C. important	D. simple
ANSWER: B			
4. The purpose of the micro	oprocessor is to control	I	
	B. switches		D. tasks
ANSWER: A		2	
5. The first digital electroni	ic computer was built i	n the year	
A. 1950	B. 1960	C. 1940	D. 1930
ANSWER: C			
6. In 1960's texas institute i			
A. integrated circuit	ts B. micropro	cessor C. vacuum	tubes D. transistor
ANSWER: A			
7. The intel 8086 micropro			
A. 8 bit	B. 16 bit	C. 32 bit	D. 4 bit
ANSWER: B			
8. The microprocessor can			
	B. I/O device	C. processor	D. register
ANSWER: A			
9. In 8086 microprocessor			
A. 12 bit B. 10	O bit C. 10	6 bit D. 2	0 bit
ANSWER: D			
10. The work of EU is			
	B. decoding	C. processing	D. calculations
ANSWER: B			
11. The 16 bit flag of 8086			
	result of ALU operation		
C. the result of addi	tion	D. the resul	t of subtraction
ANSWER: A			
12. The CF is known as		~ ~	
	B. condition flag	C. common flag	D. single flag
.ANSWER: A			
13. The SF is called as			
_	B. sign flag	C. single flag	D. condition flag
ANSWER: B			
14. The OF is called as			
	B. overdue flag	C. one flag	D. over flag
ANSWER: A			

15. The IF is called as				
A. initial flag	B. indicate flag	C. interrupt flag	D. inter flag	
ANSWER: C	-	2 0	-	
16. The register AX is formed	d by grouping			
A. AH & AL	B. BH & BL	C. CH & CL	D. DH & DL	
ANSWER: A				
17. The SP is indicated by	 			
	B. stack pointer	C. source pointer	D. destination pointer	
ANSWER: B				
18. The BP is indicated by				
A. base pointer	B. binary pointer	C. bit pointer	D. digital pointer	
ANSWER: A				
19. The SS is called as				
A. single stack	B. stack segment	C. sequence stack	.D. random stack	
ANSWER: B				
20. The index register are use				
A. memory register	B. offset address	C. segment memory	D. offset memory	
ANSWER: A				
21. The BIU contains FIFO r				
A. 8	B. 6	C. 4	D. 12	
ANSWER: B				
22. The BIU prefetches the in				
	B. register	C. memory	D. stack	
ANSWER: A				
23. The 1 MB byte of memor	ry can be divided into _	segment		
A. 1 Kbyte	B. 64 Kbyte	C. 33 Kbyte	D. 34 Kbyte	
ANSWER: B				
24. The DS is called as				
A. data segment	B. digital segment	C. divide segment	D. decode segment	
ANSWER: A				
25. The CS register stores ins		in code segment		
A. stream	B. path	C. codes	D. stream line	
ANSWER: C				
26. The IP is bits in length				
A. 8 bits	B. 4 bits	C. 16 bits	D. 32 bits	
ANSWER: C				
27. The push source copies a word from source to				
A. stack	B. memory	C. register	D. destination	
ANSWER: A				
28. LDs copies to consecutive words from memory to register and				
A. ES	B. DS	C. SS	D. CS	
ANSWER: B				
29. INC destination increments the content of destination by				
A. 1	B. 2	C. 30	D. 41	
ANSWER: A				

30. IMUL source is a signed			
A. multiplication		C. subtraction	D. division
ANSWER: A			
31destination in	verts each bit of destin	ation	
A. NOT			D. OR
ANSWER: A			
32. The JS is called as			
A. jump the signed bi		B. jump single bit	
C. jump simple bit		D. jump signal it	
ANSWER: A		0 1 0	
33. Instruction providing bot	h segment base and of	fset address are called	
	_	C. low type	
ANSWER: B	• •		
34. The conditional branch in	nstruction specify	for branchin	g
A. conditions	B. instruction	C. address	D. memory
ANSWER: A			·
35. The microprocessor deter	rmines whether the spe	ecified condition exists	or not by testing the
	•		, ,
A. carry flag	B. conditional flag	C. common flag	D. sign flag
ANSWER: B	_	-	
36. The LES copies to words	from memory to regi	ster and	
A. DS	B. CS	C. ES	D. DS
ANSWER: C			
37. The translate	s a byte from one code	e to another code	
	B. XCHNG		D. PUSH
ANSWER: A			
38. The contains an	offset instead of actua	al address	
A. SP	B. IP	C. ES	D. SS
ANSWER: B			
39. The 8086 fetches instruct	tion one after another	from of m	emory
A. code segment	B. IP	C. ES	D. SS
ANSWER: A			
40. The BIU contains FIFO r	register of size 6 bytes	called	
A. queue	B. stack	C. segment	D. register
ANSWER: A			
41. The is requ	iired to synchronize th	e internal operands in	the processor CLK
Signal			
A. UR Signal	B. Vcc	C. AIE	D. Ground
ANSWER: A			
42. The pin of minimum mod	de AD0-AD15 has	address	
A. 16 bit	B. 20 bit	C. 32 bit	D. 4 bit
ANSWER: B			
43. The pin of minimum mode AD0- AD15 has data bus			
A. 4 bit	B. 20 bit	C. 16 bit	D. 32 bit
ANSWER: C			
44. The address bits are sent	out on lines through		

A. A16-19	B. A0-17	C. D0-D17	D. C0-C17
ANSWER: A			
45 is used to wri	te into memory		
A. RD	B. WR	C. RD / WR	D. CLK
ANSWER: B			
46. The functions of Pins from	om 24 to 31 depend on	the mode in which	is operating
A. 8085	B. 8086		
ANSWER: B			
47. The RD, WR, M/IO is the	ne heart of control for a	a mode	
		mpatibility mode	D. control mode
ANSWER: A			_ , , , , , , , , , , , , , , , , , , ,
48. In a minimum mode the	re is a	n the system bus	
	B. double		D. triple
ANSWER: A	D. dodolo	o. manpro	2. unpre
49. If MN/MX is low the 80	186 operates in	mode	
		C. both (A) and (B)	D medium
ANSWER: B	D. Maximum	C. 00th (11) and (D)	D. medium
50. In max mode, control bu	s signal So S1 and S2	are sent out in	form
		C. shared	
ANSWER: B	D. Cheoded	C. Shared	D. unshared
51. The bus controller d	levice decodes the sign	als to produce the cont	rol bus signal
A. internal	_	<u>-</u>	
ANSWER: C	D. data	C. CAUTHAI	D. address
52. A Instruction at the	he and of interrupt cars	vice program takes the	evecution back to the
interrupted program	ne end of interrupt serv	vice program takes the	execution back to the
1 1 0	B. return	C. data	D. line
ANSWER: B	D. ICIUIII	C. uata	D. IIIIe
	a ara ta	define a flexible set of	aammanda
53. The main concerns of th	e are to	D. maninhanal intenface	Commands
A. memory interface	,	B. peripheral interface	ie –
C. both (A) and (B)		D. control interface	
.ANSWER: A		. 41	he able to used from
54. Primary function of mer	nory interfacing is that	thesnould	be able to read from
and write into register	D '	C 1 1D	D
A. multiprocessor	B. microprocessor	C. dual Processor	D. coprocessor
ANSWER: B	4 1 1111		
55. To perform any operation	<u>-</u>	•	ъ.
A. register	B. memory	C. interface	D. system
ANSWER: A			
56. The Microprocessor place			5 2211
A. 4 bit	B. 8 bit	C. 16 bit	D. 32 bit
ANSWER: C			
57. The Microprocessor place	ces 16 bit address on th	ne add lines from that a	ddress by
register should be selected	_		
A. address	B. one	C. two	D. three
ANSWER: B			

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72. CS connect the output of	: · 			
A. encoder	B. decoder	C. slave program	D. buffer	
ANSWER: B				
73. In which year, 8086 was introduced?				
A. 1978	B. 1979	C. 1977	D. 1981	
ANSWER: A				
74. Expansion for HMOS ted	chnology			
A. high level mode o	xygen semiconductor			
B. high level metal of	xygen semiconductor			
C. high performance	medium oxide semicor	nductor		
D. high performance	metal oxide semicondu	ictor		
ANSWER: D				
75. 8086 and 8088 contains	transistors			
A. 29000	B. 24000	C. 34000	D. 54000	
ANSWER: A				
76. ALE stands for				
A. address latch enab	ole	B. address level enable		
C. address leak enabl	e	D. address leak exten	sion	
ANSWER: A				
77. What is DEN?				
A. direct enable	B. data entered	C. data enable	D. data encoding	
ANSWER: C				
78. In 8086, Example for No	on maskable interrupts a	are		
A. TRAP	B. RST6.5	C. INTR	D. RST6.6	
ANSWER: A				
79. In 8086 the overflow flag	g is set when	·		
A. the sum is more th	nan 16 bits.			
B. signed numbers go	o out of their range afte	r an arithmetic operation	on.	
C. carry and sign flag	gs are set.			
D. subtraction				
ANSWER: B				
80. In 8086 microprocessor the following has the highest priority among all type interrupts?				
A. NMI	B. DIV 0	C. TYPE 255	D. OVER FLOW	
ANSWER: A				
81. In 8086 microprocessor one of the following statements is not true?				
A. coprocessor is interfaced in max mode. B. coprocessor is interfaced in min mode.				
C. I/O can be interfaced in max / min mode. D. supports pipelining				
ANSWER: B				
82. Address line for TRAP is?				
A. 0023H	B. 0024H	C. 0033H	D. 0099H	
ANSWER: B				
83. Access time is faster for				
A. ROM	B. SRAM	C. DRAM	D. ERAM	
ANSWER: B				

•			
0 C. 8085	D. 4008		
k C. counter	D. flags		
	_		
asic element within the microproces	ssor?		
B. Arithmetic logic unit (Al	LU)		
D. Control unit			
I for certain types of data transfer?			
B. Interrupt-driven I/O			
D. Direct memory access (I	DMA)		
B. Control bus			
D. None of the above			
)			
B. 2 – bit data bus			
D. 8 – bit data bus	D. 8 – bit data bus		
plexed data and address lines?			
86 C. 80386	D. Pentium		
cister C. Memory location	D. Assembler		
•			
n unit (EU)?			
J) B. Clock			
, and the second			
<u> </u>			
	ons		
, ,	D. 8,388,608 locations		
,,			
arithmetic instruction?			
, == = (= = \ 2020)			
	C. 8085 C. counter asic element within the microproces B. Arithmetic logic unit (All D. Control unit for certain types of data transfer? B. Interrupt-driven I/O D. Direct memory access (I B. Control bus D. None of the above B. 2 – bit data bus D. 8 – bit data bus D. 8 – bit data bus clexed data and address lines? C. 80386 C. Memory location a unit (EU)? J) B. Clock D. Flags B. 2,097,152 location		

95. During a read operation to	he CPU fetches	S		
A. a program instructi	ion	B. another address		
C. data itself		D. all of the above		
Ans.: D				
96. Which of the following is	s not an 8086/8	088 general-purpose registe	er?	
_		B. Data segment (DS)		
C. Stack segment (SS)	D. Address segment (AS)		
Ans.: D				
97. A 20-bit address bus allo	ws access to a 1	memory of capacity		
A. 1 MB	B. 2 MB	C. 4 MB	D. 8 MB	
Ans.: A				
98. Which microprocessor ac	cepts the progr	am written for 8086 withou	ut any changes?	
A. 8085	B. 8086	C. 8087	D. 8088	
Ans.: D				
99. Which group of instruction	ons do not affec	et the flags?		
A. Arithmetic operations		B. Logic operations		
C. Data transfer operations		D. Branch operations		
Ans.: C				
100. The result of MOV AL,	65 is to store			
A. store 0100 0010 in AL		B. store 42	H in AL	
C. store 40H in AL		D. store 01	00 0001 in AL	
Ans.: D				