Computer Organisation and Architecture Lab

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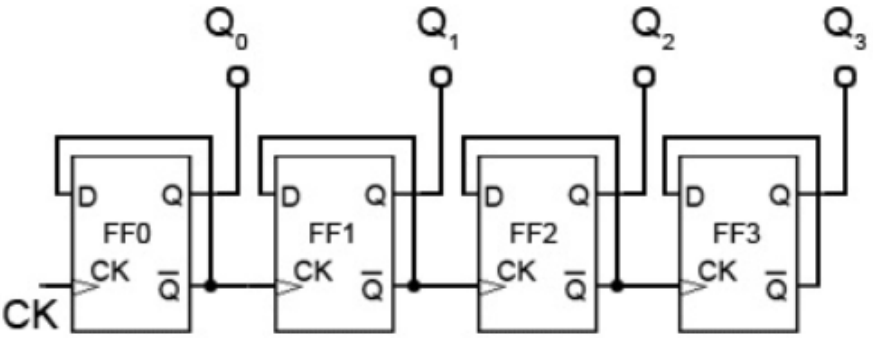
Verilog Assignment 2

4 bit asynchronous up counter:

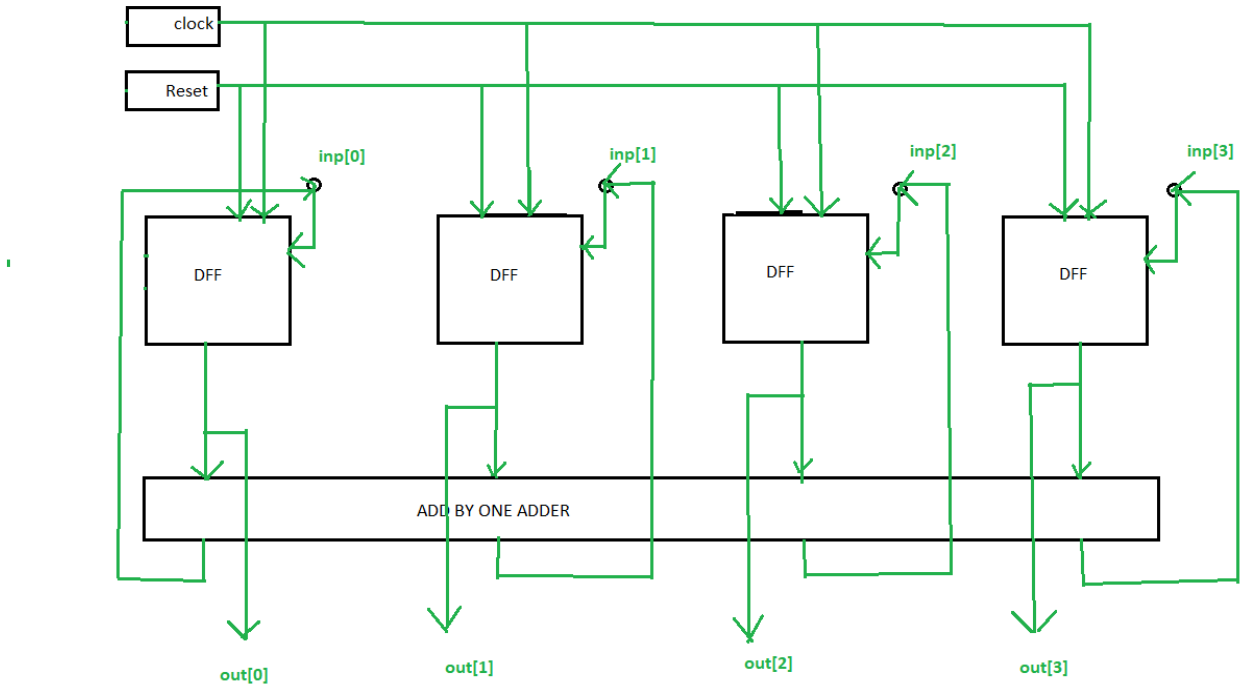
A 4 bit asynchronous UP counter with D flip flop is shown in above diagram. It is capable of counting numbers from 0 to 15. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop.

4 bit asynchronous up counter Architecture :

A 4 bit asynchronous UP counter with D flip flop



A 4 bit asynchronous UP counter with D flip flop



In structural Implementation of the Up Counter, we have used 4 DFFs for making the circuit structural. We are giving clock and asynchronous reset as input for each DFF and with clock and reset we are giving 1 bit of 4 bit counter in each DFF. Each DFF is given a bit as output. We have passed that bit as input for Add by 1 adder which is an optimised version of 4 bit CLA.

In Add by 1 bit adder, since we are adding by 1 each time, so there are some of the bits in CLA which remain 0, so we can say that there are some of the operations in the CLA circuit which are redundant, so we can save some delay.

The bitwise operations in the Add by 1 bit Adder are following: -

Input → 4 bit ***in_***

Output → 4 bit ***out_***

out_[0] = ~in_[0]

out_[1] = in_[1] ^ in_[0]

out_[2] = in_[2] ^ (in_[1] & in_[0])

out_[3] = in_[3] ^ (in_[2] & in_[1] & in_[0])

After passing the 4 bit input through this Add by 1 adder, we shall get next counter (counter +1) as an output of Add by 1 Adder and we shall send it back to the DFFs.

Finally we are returning the outputs of the DFFs.