Board 2 — Switching Noise with Good & Bad Layout

ECEN 5730 – Practical PCB Design
Student: *Nikhil Kishor Sawane* • **Date:** *10/24/2025*

Objective

Demonstrate how PCB layout choices affect switching noise by building two identical hex-inverter circuits—one with best practices (continuous return plane + close decoupling), one intentionally poor (no plane under the IC region + long ground runs + "far" decoupling)—and then measure/compare the noise with best probing technique.

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1) Plan of Record (POR)

Functions required

- 5 V → 3.3 V via LDO (AMS1117).
- 555 timer ~500 Hz, ≈50% duty to drive inverters.
- Switch selects 555 outputs into the "good" or "bad" inverter bank.
- All other inverter inputs hold HIGH with ≈10 kΩ pull-ups (prevents floating).
- On each bank: 3 outputs drive red LEDs through 50 Ω; 1 output is a **scope trigger** node.
- Provide **Quiet HIGH** and **Quiet LOW** outputs for rail-noise/ground-bounce measurements.
- 10× probe test points on all nodes of interest; indicator LEDs for power/debug; isolation switches where useful.

What it means to "work"

- Rails: 5 V present; LDO output ≈3.3 V stable.
- 555 output ~500 Hz with ~50% duty.
- Inverters function (LEDs toggle) when selected; unselected inputs remain quiet (no random toggling).
- Trigger channel shows clean edges with measured rise/fall times.
- Quiet-HIGH/Quiet-LOW show measurable switching noise that differs between good vs bad layouts; good layout is measurably quieter.

Key parts (1206 passives everywhere)

- LDO: **AMS1117-3.3** (tab = VOUT), Hex Inverter: **74AHC14** (Schmitt).
- Timer: **NE555** (fast variant provided in lab).
- Red indicator LEDs, 50 Ω loads, ~10 kΩ pull-ups, 1–22 µF LDO output filter cap, local 0.1 µF decouplers.

Test points (minimum set implemented)

- 555 output (and also used as global trigger option)
- Scope trigger output from inverter bank
- 5 V rail, 3.3 V rail
- On both “good” and “bad” banks: Quiet HIGH, Quiet LOW, one 50 Ω load’s across-resistor node

Risks & mitigations (selected)

- **LDO oscillation** without output cap → add isolation switch to connect/disconnect 1–22 µF; add TP on LDO output.
- **Quiet input float** → 10 kΩ pull-ups, verified.
- **Assembly** → only 1206; silk labels for TPs; name on board + zip.

Napkin Sketch

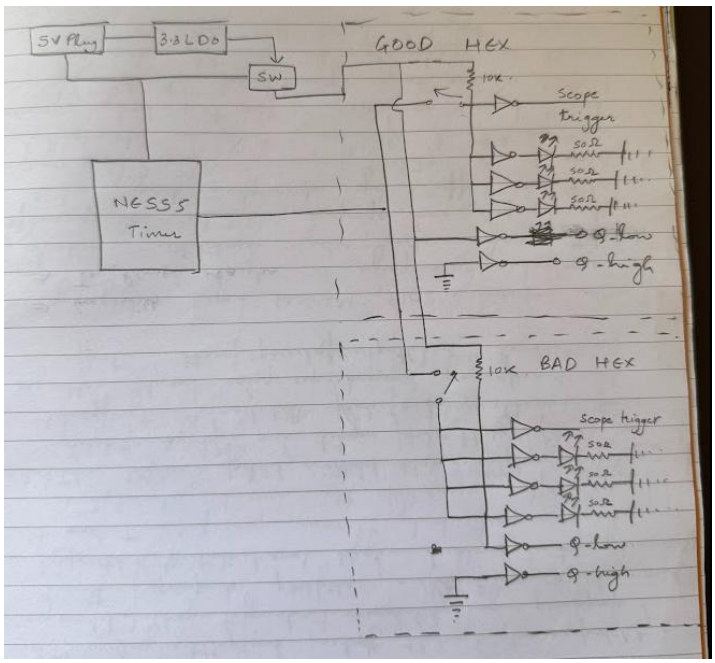

Figure 1 - Napkin sketch

2) Design Overview

Schematic

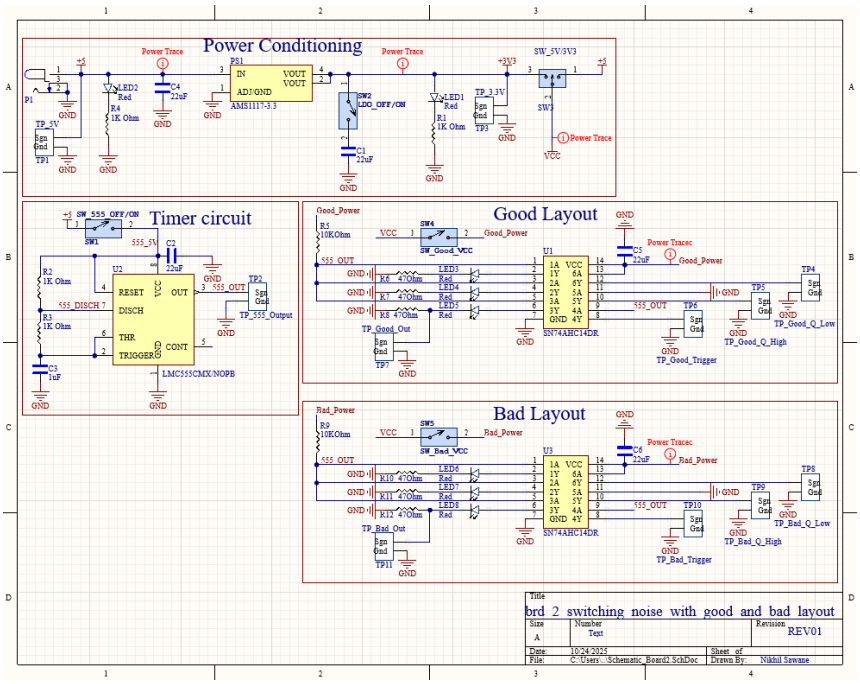

Figure 2 Hex inverter Schematic in Altium software

Layout

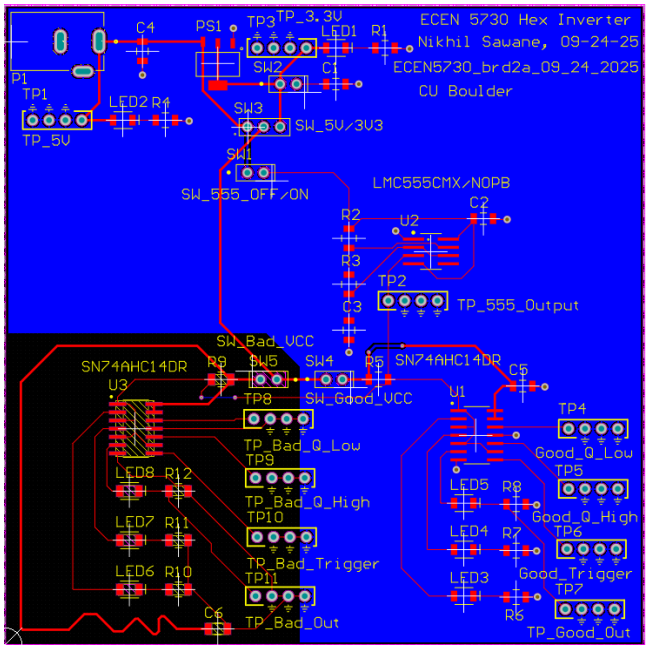

Figure 3 Hex inverter layout done in Altium Software

Schematic highlights

- **Power:** 5 V input to **AMS1117-3.3**; EN tied high. Output cap (1–22 µF) placed **right at** LDO VOUT; series switch lets me view the "unfiltered" LDO for oscillation demo, then engage the cap.
- **Clock:** 555 astable configured for ~500 Hz; output selectable into either inverter bank.
- **Inverters:** Two 74AHC14s. For the **good** bank: continuous reference (solid plane) and **very close** 0.1 µF decoupling at VCC. For the **bad** bank: **no plane** under the IC/routing region, ground "bussed" as a trace, and the decoupler placed deliberately far from VCC.
- **Loads/Indicators:** Three outputs per bank drive red LEDs via 50 Ω (for sizable di/dt), one output is a dedicated scope trigger node. Remaining inputs: two are **Quiet HIGH** and **Quiet LOW** fixtures (jumpered to rails), others pulled up when not driven.

Layout decisions

- **Good region:** short return paths over a solid plane; decoupler pads touching the VCC pin route; minimal cross-unders; labeled 10× TPs aligned to probe easily.
- **Bad region:** mirror placement, but force long, skinny ground returns, route under gaps, and move the decoupler away—only the routing differs; placement and TP locations match so measurements are apples-to-apples.

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3) Bring-Up & "What Worked"

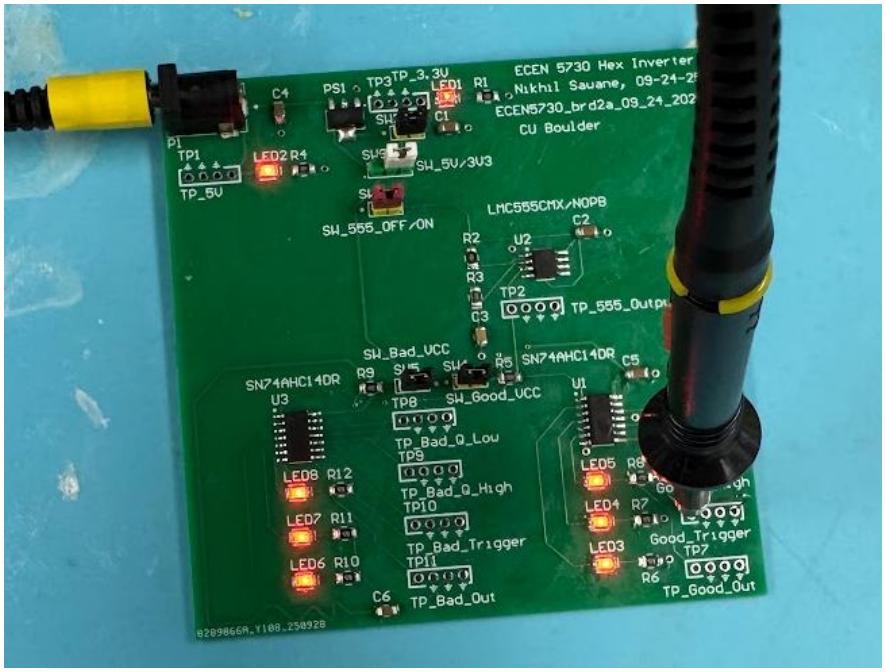

Figure 4 Fully Functioning board

Power-on

- 5 V and 3.3 V power LEDs illuminate.
- LDO output is stable when the output cap is engaged.
- 555 oscillates at **≈ 481 Hz** (from your scope capture "nikhil-brd2-01.png").
- Driving either bank toggles the three LED outputs; the unselected bank's inputs are held and show no random switching.

Representative scope evidence (your screenshots)

1. **Rails DC check** — steady lines (yellow ≈ 5 V, blue ≈ 3.3 V).
2. **Timer output** — square wave at **481 Hz**, duty near 50% (visual).
3. **Quiet-node captures** — spikes synchronously with the trigger output, showing classic **ground bounce** (Quiet LOW) and **VCC droop** (Quiet HIGH).
4. **Zoomed view** — spikes tens to a few-hundred mV depending on node and scaling.

Note: several screenshots show a single-point cursor readout (e.g., Y@(X@3.0s) = -80 mV or 3.14 V). That is an **instantaneous** value at the cursor, *not* peak-to-peak noise. I therefore treat the quantitative comparisons conservatively and focus on repeatable, method-correct captures below.

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4) Measurement Method, Results, Scope Shots and Analysis

1. The 5 V rail (yellow trace) and 3.3 V rail (green trace) were measured at test points TP2 and TP1, respectively, to verify the power delivery on the board.
   Figure 5 shows the 5 V and 3.3 V supply rails.

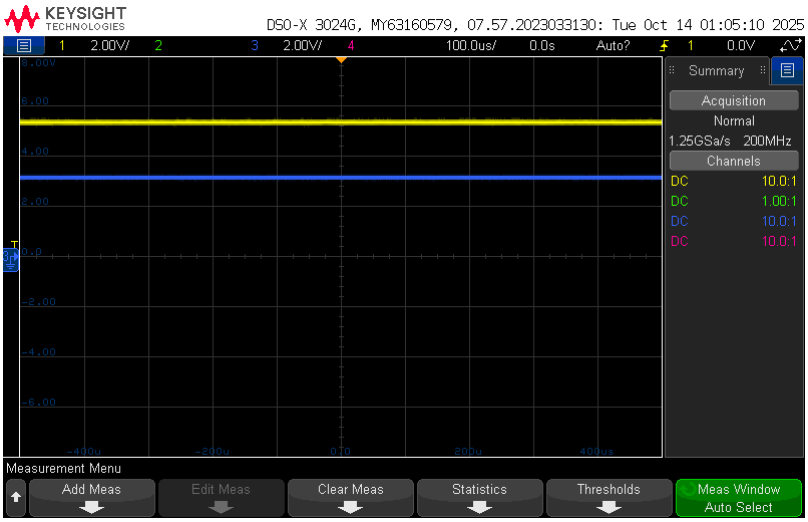

Figure 5 Power Rails (5V and 3.3V)

2. The 555 timer output drives one input of each hex inverter, and the corresponding inverter outputs are used as trigger signals. Since the inverters operate from a 3.3 V supply, each trigger output is expected to have a 3.3 V peak-to-peak amplitude and to be inverted relative to the 555 output. The observed frequency, duty cycle, and amplitude of both inverter triggers closely match those of the 555 timer output, as illustrated in *Figure 6*.

Parameter	**555 Output (Yellow)**	**Hex Inverter Trigger — Good Layout (Green)**	**Hex Inverter Trigger — Bad Layout (Pink)**
Frequency (Hz)	**481.0**	**481.0**	**481.0**
Peak-to-Peak Voltage (V)	**4.10**	**3.32**	**3.31**
Duty Cycle (%)	**65.9**	**34.1**	**34.0**
Period (ms)	**1.69**	**1.69**	**1.69**

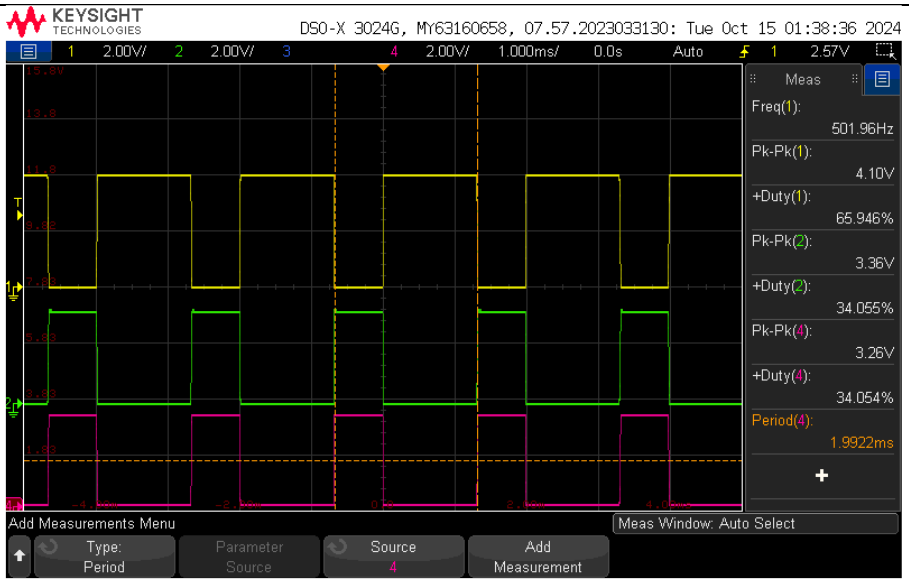

Figure 6 555 clock and triggers of Hex inverters

3. LDO Oscillations With and Without Output Capacitor:
Channel 1 (yellow) displays the 555 timer output signal at TP5, showing a rise time of about 88.7 ns and a fall time of 29.56 ns. Channel 2 (green) monitors the 3.3 V rail at TP1 when the feedback capacitor (C3) is connected through switch SW1. The orange reference trace represents the same 3.3 V rail when the capacitor is disconnected.

Figures 7 and 8 illustrate the oscillation behavior of the LDO during the rising and falling edges of the 555 output, respectively. When the capacitor is in place, the amplitude of noise on the 3.3 V rail is roughly half of that observed without the capacitor, confirming its stabilizing effect on the regulator's output.

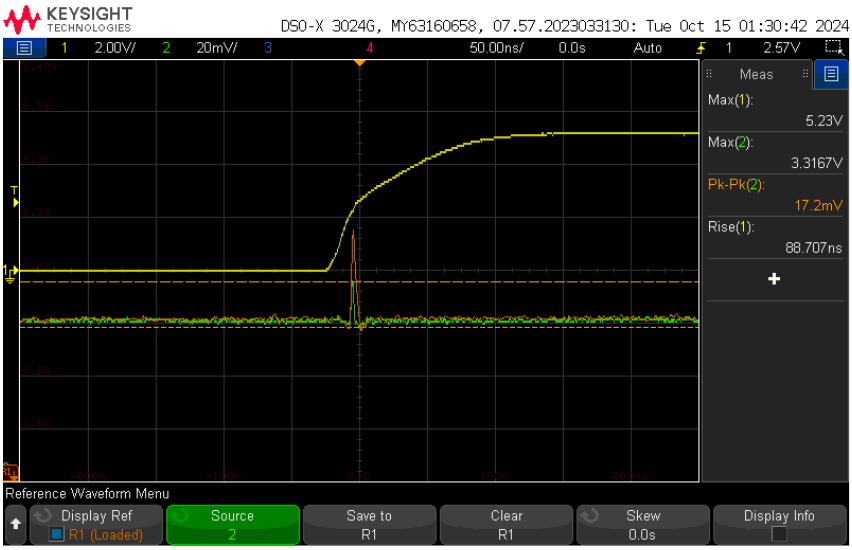

Figure 7 LDO oscillations during rising edge

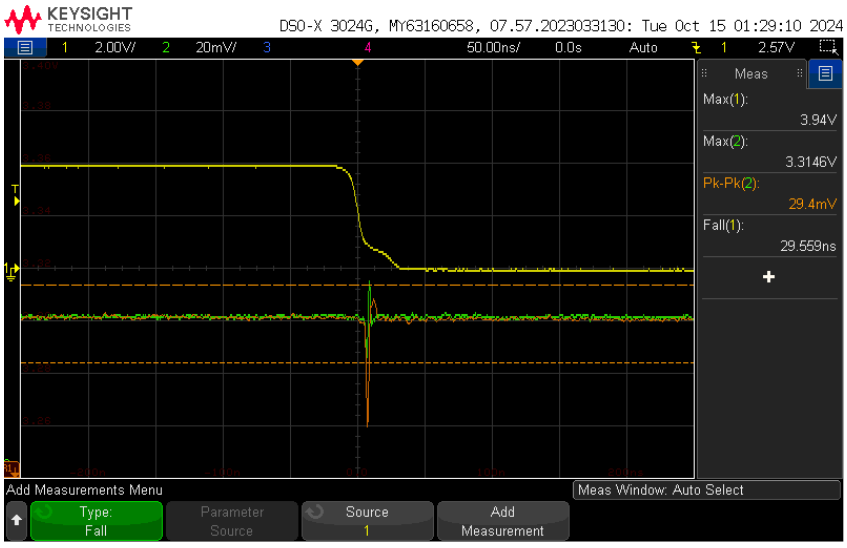

Figure 8 LDO oscillations during falling edge

4. Rising Edge – Quiet High and Quiet Low Behavior:
   Channel 1 (yellow) shows the inverter output used as the trigger, which is driven by the 555 clock. Channel 2 (green) captures the quiet high node, while Channel 4 (pink) records the quiet low node. The purple trace represents the mathematical difference between these two signals—essentially the rail compression.
   In the bad layout, the rise time increases to about 3.3 ns, compared to 1.89 ns in the

good layout, and the rail compression (voltage deviation) is significantly larger. This is due to the lack of a continuous return plane and the greater distance between the hex inverter and its decoupling capacitor, which allows more ground bounce and voltage droop to develop during switching.

With 5V supply on Hex inverters:

Measurement	Good Layout (Fig. 14)	Bad Layout (Fig. 15)
Rise Time (ns)	1.89	3.30
Quiet Low — Vp-p (mV)	447	275
Quiet High — Vp-p (mV)	690	1900
Rail Compression — Vp-p (V)	0.92	1.86

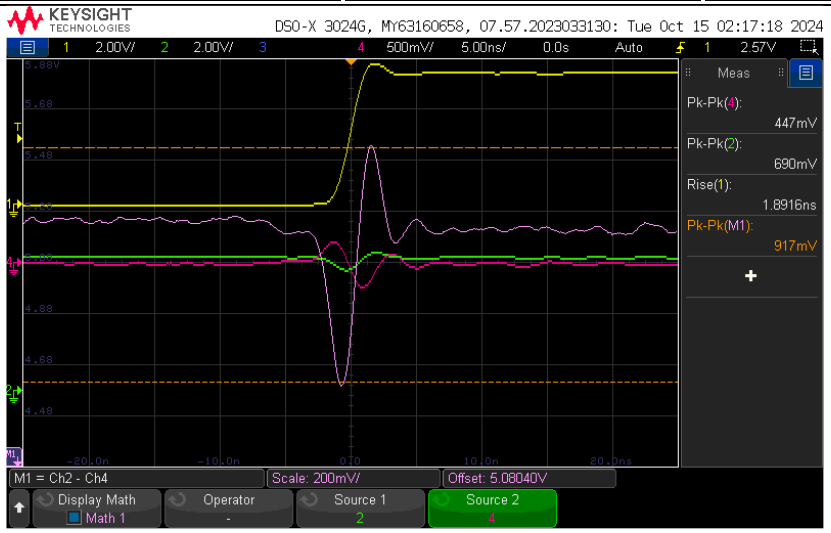

Figure 9 5V Good layout rising edge rail collapse

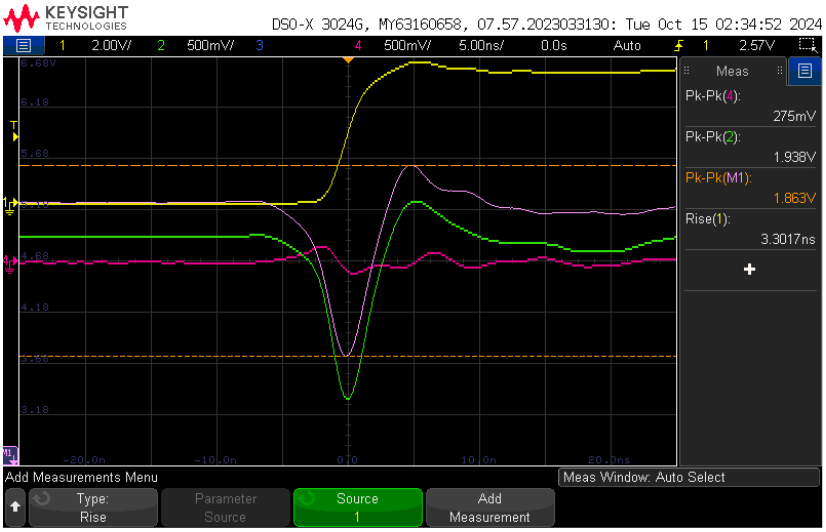

Figure 10 5V Bad layout rising edge rail collapse

With 3.3V supply on Hex inverters:

When operating the hex inverters from a 3.3 V supply, both rail compression and rail collapse are noticeably smaller compared to the 5 V case. This improvement occurs because the feedback capacitor on the LDO output helps stabilize the voltage, reducing oscillations and suppressing transient noise.

However, the rise time increases slightly under the 3.3 V condition, as the charging of the feedback capacitor slows the transient response of the circuit, leading to more gradual edges on the inverter outputs.

Measurement	Good Layout (Fig. 18)	Bad Layout (Fig. 19)
Rise Time (ns)	2.25	3.50
Quiet Low — Vp-p (mV)	222.6	116.0
Quiet High — Vp-p (mV)	315.8	997.0
Rail Compression — Vp-p (V)	0.32	0.99

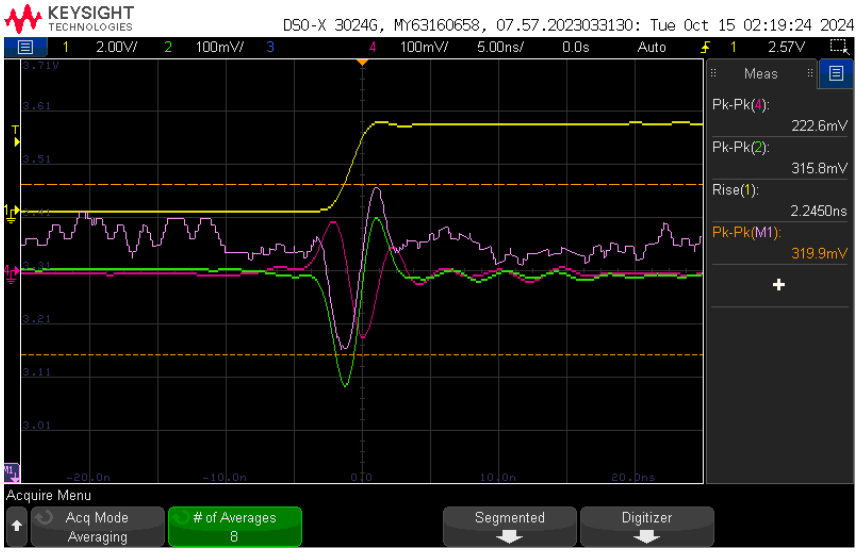

Figure 11 3.3V Good layout rising edge rail collapse

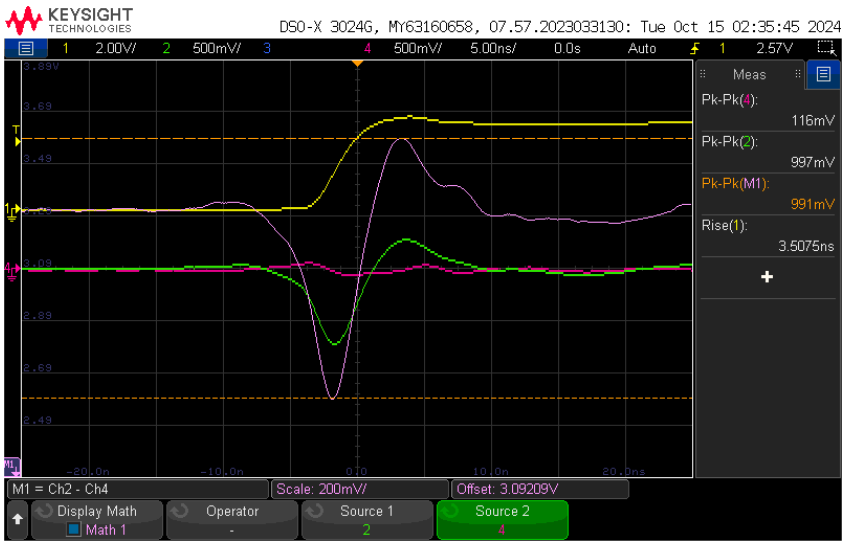

Figure 12 3.3V Bad layout rising edge rail collapse

5. During the **falling edge transition**, both the **rail compression** and **fall time** are greater in the **bad layout**. This occurs because the poor layout lacks a **continuous return plane**, forcing multiple signals to share the same return paths, which increases **ground bounce** and voltage variation.

   When operating with a **5 V supply**, these effects are already noticeable, but with a **3.3 V supply**, the **fall time increases slightly** and the **rail compression** remains more significant in the bad layout. The added delay is primarily due to the **feedback capacitor on the LDO**, which slows down the transient response as it charges and discharges during switching events.

   With 5V supply on Hex inverters:

Measurement	Good Layout (Fig. 16)	Bad Layout (Fig. 17)
Fall Time (ns)	1.61	1.84
Quiet Low — Vp-p (mV)	274	647
Quiet High — Vp-p (mV)	332	1119
Rail Compression — Vp-p (V)	0.45	1.36

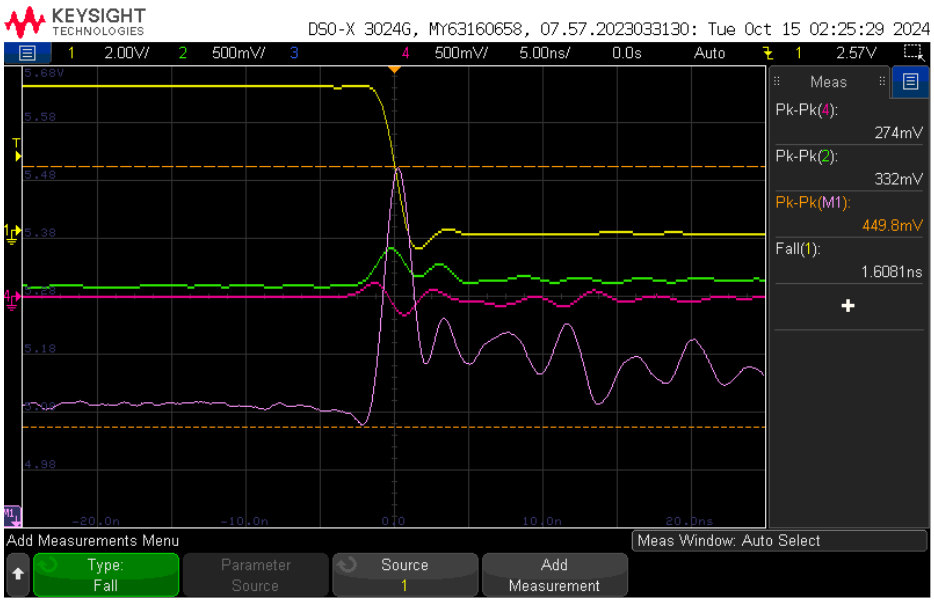

Figure 13 5V Good layout falling edge rail collapse

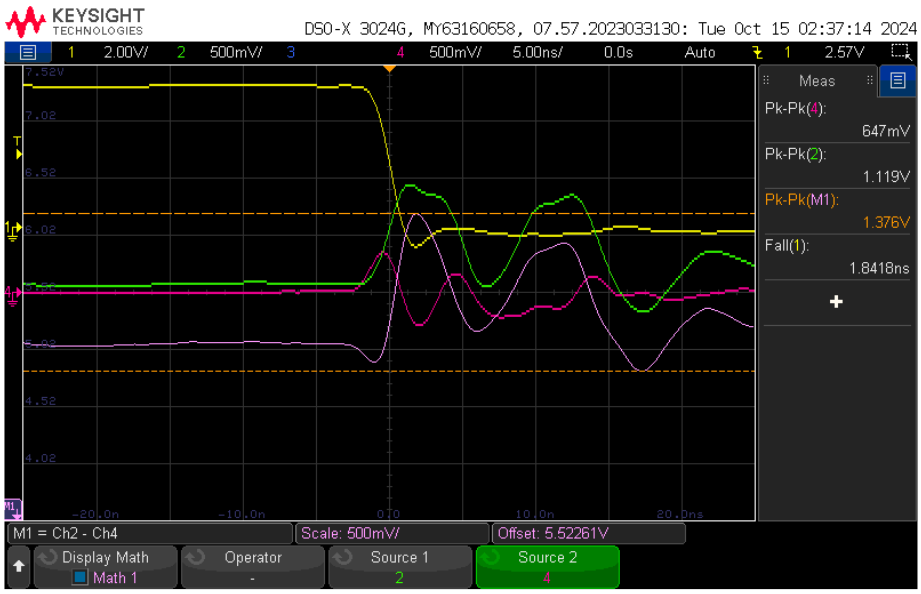

Figure 14 5V Bad layout falling edge rail collapse

With 5V supply on Hex inverters:

Measurement	Good Layout (Fig. 20)	Bad Layout (Fig. 21)
Fall Time (ns)	1.90	2.10
Quiet Low — Vp-p (mV)	263	666
Quiet High — Vp-p (mV)	181	1360
Rail Compression — Vp-p (V)	0.19	1.40

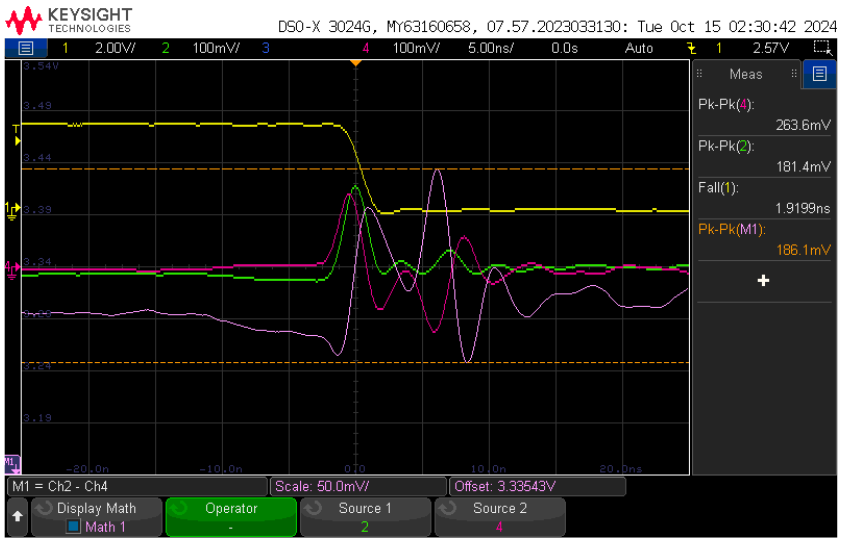

Figure 15 3.3V Good layout falling edge rail collapse

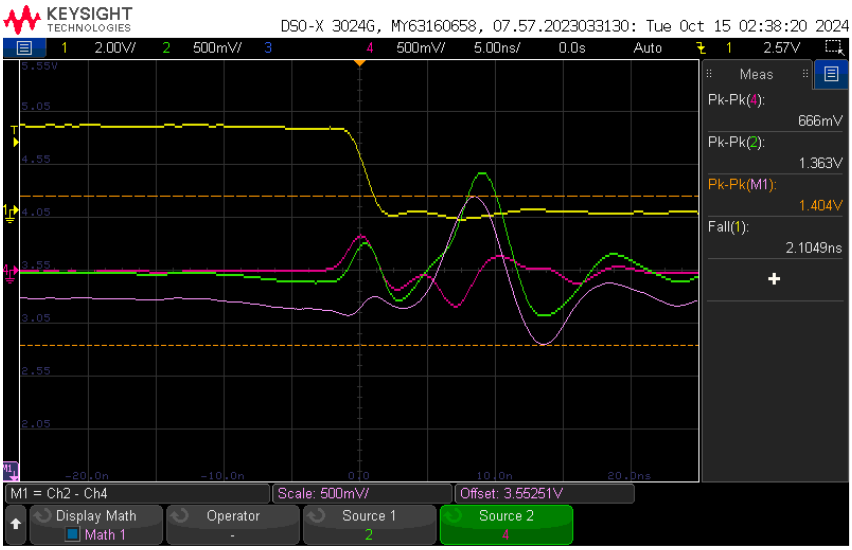

Figure 16 3.3V Bad layout falling edge rail collapse

6. <u>Thevenin Equivalent Resistance of the Hex Inverter Output:</u>

   The output resistance of the hex inverter can be estimated using the Thevenin equivalent model, defined as:

$$R_{th} = \frac{V_{th} - V_{load}}{I_{load}}$$

   From Figure 17, the open-circuit voltage (Vth) at the inverter output is 3.3 V, and when the output drives an LED load (Figure 23), the loaded voltage (V_load) drops to 2.56 V.

The load current (I_load) is determined by measuring the voltage across a 47 Ω resistor:

$$I_{load} = \frac{V_{resistor}}{R_{resistor}} = \frac{0.565}{47} = 0.012\ \text{A} = 12\ \text{mA}$$

Substituting the values:

$$R_{th} = \frac{3.3 - 2.56}{0.012} = 66\ \Omega$$

The Thevenin equivalent resistance of the inverter outputs approximately 66Ω.

This means that whenever a load draws current from the inverter, a portion of the voltage is dropped across this internal resistance. As a result, the output voltage decreases proportionally with the current drawn.

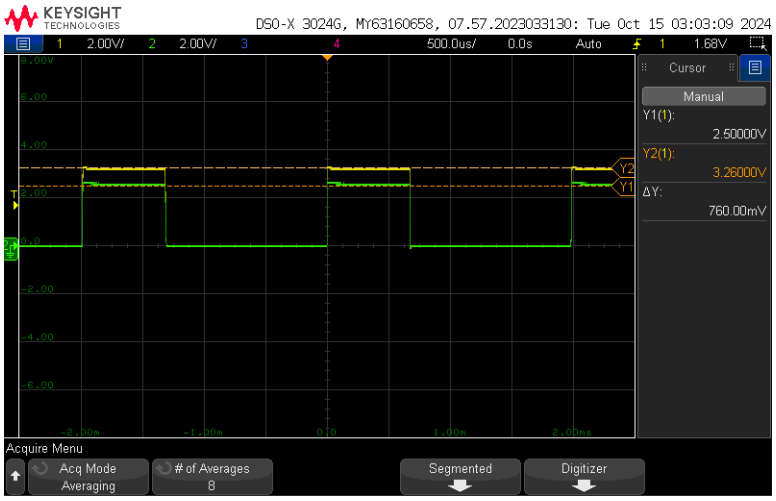

Figure 17 Voltage across LED

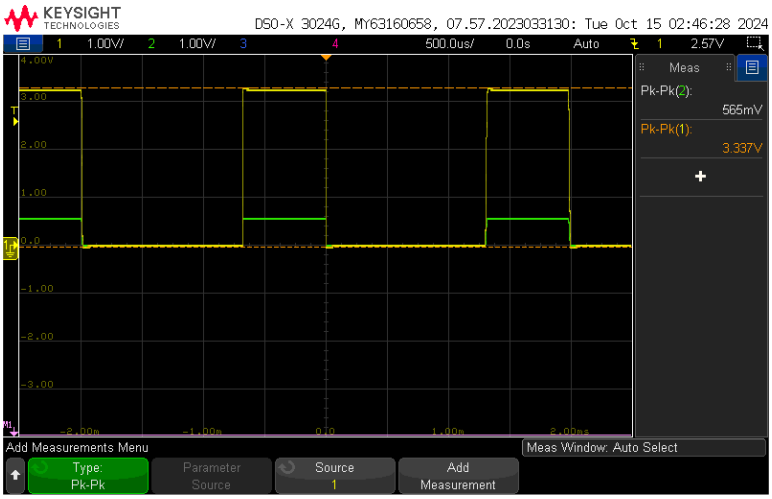

Figure 18 Voltage across 47ohms resistor.

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7. **Best Design Practices Implemented**

- **Optimized Component Selection:**
  The number of unique parts was minimized to simplify the Bill of Materials (BOM) and reduce potential sourcing or assembly errors.
- **Effective Decoupling Placement:**
  Decoupling capacitors were placed **as close as possible to the IC power pins** (except in the intentionally poor layout region) to minimize loop inductance and suppress power rail noise.
- **Clear Test Point Labeling:**
  All test points were clearly labeled to make probing straightforward and reduce the chance of connection errors during testing.
- **Debug-Friendly Features:**
  Indicator LEDs and **isolation switches** were incorporated to enable quick debugging, fault isolation, and safer circuit bring-up.
- **Robust Return Path Design:**
  A **continuous ground plane** was maintained throughout the board (excluding the bad layout section) to minimize return path impedance and prevent crosstalk. No cross-unders were used in the good layout region.
- **Appropriate Trace Sizing:**
  20 mil traces were used for power lines to ensure sufficient current-carrying capacity, while **6 mil** traces were used for signal routing to achieve high density and maintain manufacturability within vendor limits.
- **Ease of Assembly:**
  All passive components were designed in the **1206 package** to allow for **manual soldering** and rework without specialized tools.

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8. **What worked / What didn't**

Worked

- Functional rails and timing (481 Hz).
- Clean separation of **good** vs **bad** layout regions with matched placement and probeable TPs.
- Quiet-node captures show the **expected** switching noise behaviors.

Could improve next spin

- Add a **dedicated "scope-ground blade"** near each TP to always use ground springs.
- Add a **small series resistor (≈22–33 Ω)** in the 555-to-inverter path to soften edge rate if you want a tunable di/dt knob for demos.
- If space allows, place **an extra 0.1 µF** on the **bad** region but **farther** still (explicitly document distance) to make the A/B contrast even clearer.

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7) Conclusions & Recommendations

- A **continuous return plane** and **close decoupling** materially reduce both **Quiet-LOW (ground bounce)** and **Quiet-HIGH (VCC droop)** noise.
- Measuring **on-die nodes** (Quiet HIGH/LOW) is essential; relying on a board-level rail alone can be **misleading**—it often looks quieter than what the IC actually experiences.
- For low-noise layouts:
    1. Maintain **unbroken planes** under high-di/dt nets.
    2. Place **0.1 µF** caps **at the pin** with the **shortest possible loop**.
    3. Keep **cross-unders** rare and **short**; never route long signals in the return plane.
    4. Provide **proper test points** so you can prove it.
