ECEN 5730 – Practical PCB Design (Fall 2025)

Board 1 Report

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Objective

The purpose of this lab was to get familiar with the complete PCB design flow, starting from a conceptual sketch to a functioning circuit. Specifically, I designed and built a 555 timer in astable mode to generate a square wave around 500 Hz with ~60% duty cycle. The circuit drives multiple LEDs through different current-limiting resistors. Along the way, I practiced schematic capture in Altium, manual solder assembly, and measured rise/fall times, duty cycle, and noise on the power rail to better understand non-ideal behavior of the 555 IC.

Plan of Record (POR)

My design included:

1. A DC barrel jack for 5 V supply
2. NE555 timer in astable configuration targeting 500 Hz
3. 4 identical LEDs in parallel, each with a different resistor (47 Ω, 300 Ω,1 kΩ,10 kΩ)
4. A power indicator LED
5. Test points for 5 V rail, 555 output, and current measurement
6. Header pins to isolate supply/output for debug

Napkin Sketch

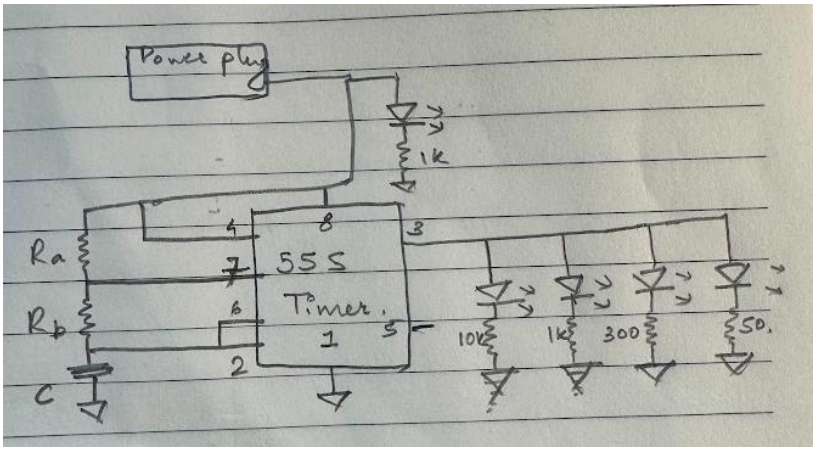


Figure 1 - Napkin sketch 555 timer (Astable mode)

Component Selection and Calculations

- LED forward drop ≈ 2 V. With 5 V drive:
  - 47 Ω → (5-2)/47 ≈ 64 mA
  - 300 Ω → 10 mA
  - 1 kΩ → 3 mA
  - 10 kΩ → 0.3 mA
- Total current ≈ 77 mA. The NE555 can source/sink up to ~200 mA, so it is sufficient.
- Frequency equation:

$$f = \frac{1.44}{((Ra\ +\ 2Rb)\ *\ C)}$$

  With Ra = Rb = 1 kΩ, solving for 500 Hz → C ≈ 1 µF.
- Expected duty cycle ≈ 66%.

$$Duty\ cycle = \frac{TON}{TON + TOFF} = \frac{0.693\ (Ra + Rb)C}{[0.693(Ra + Rb)C\} + 0.693(Rb)C}$$

Bill of Materials (BOM)

- NE555DR timer IC
- Resistors: 47 Ω, 300 Ω, 1 kΩ, 10 kΩ (LED paths)
- Resistors: 1 kΩ × 2 (timing)
- Capacitors: 1 µF (timing), 22 µF × 2 (decoupling)
- LEDs: 5 total
- DC barrel jack
- Header pins/test points

Schematic and Layout

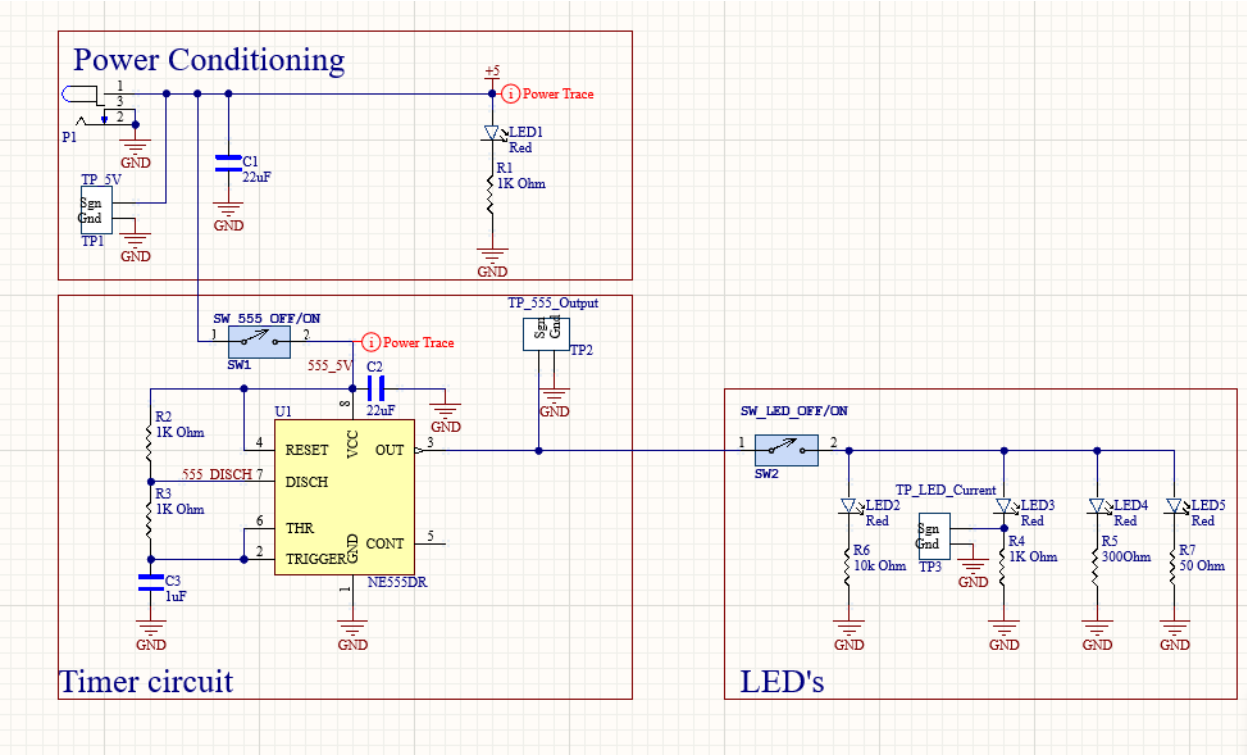


Figure 2 555 Timer Schematic in Altium

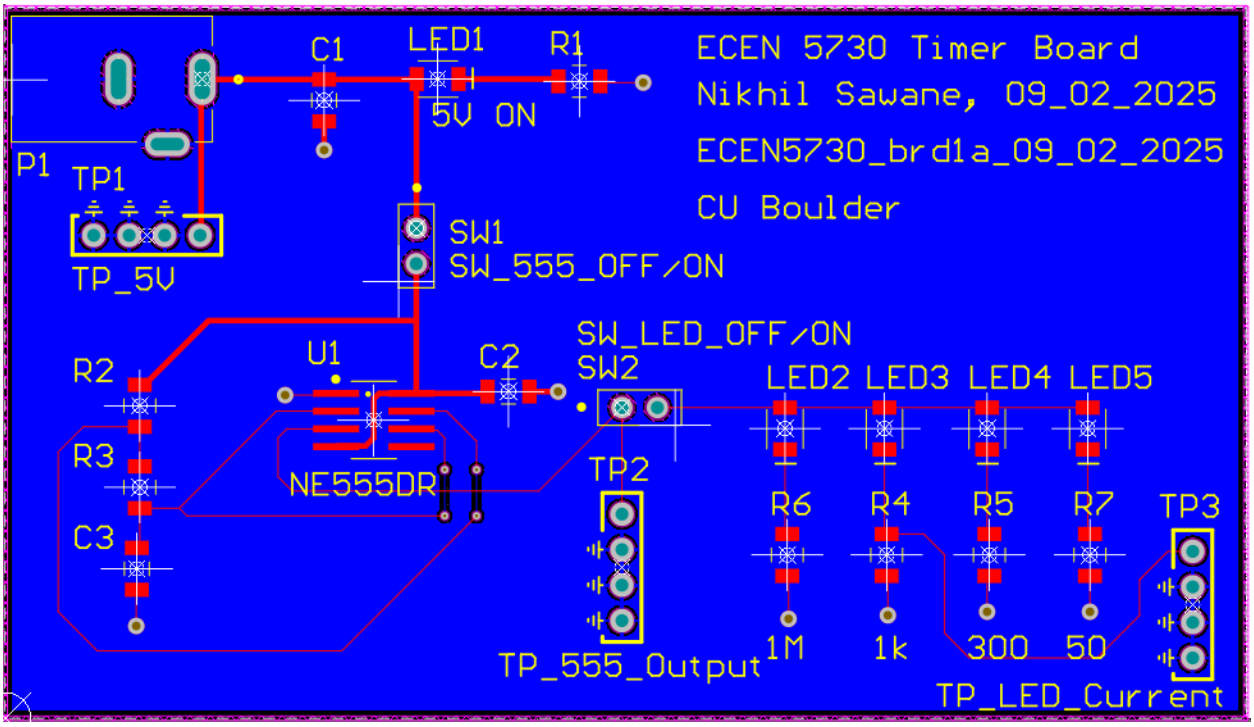
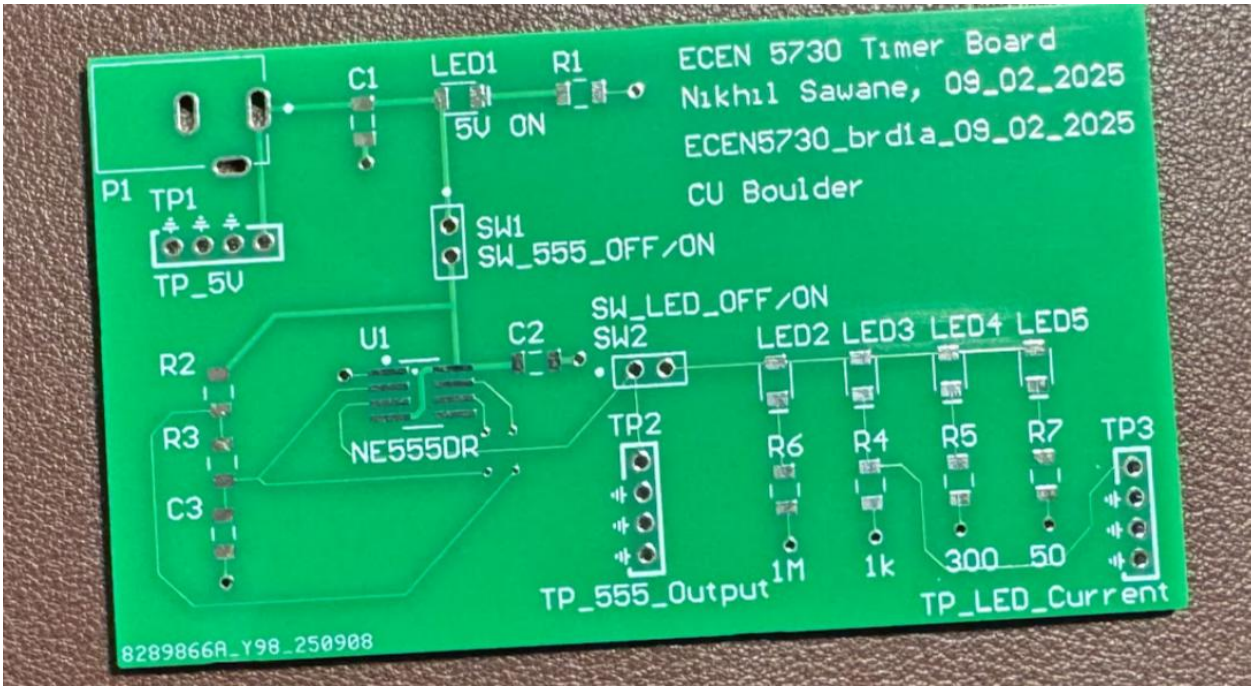


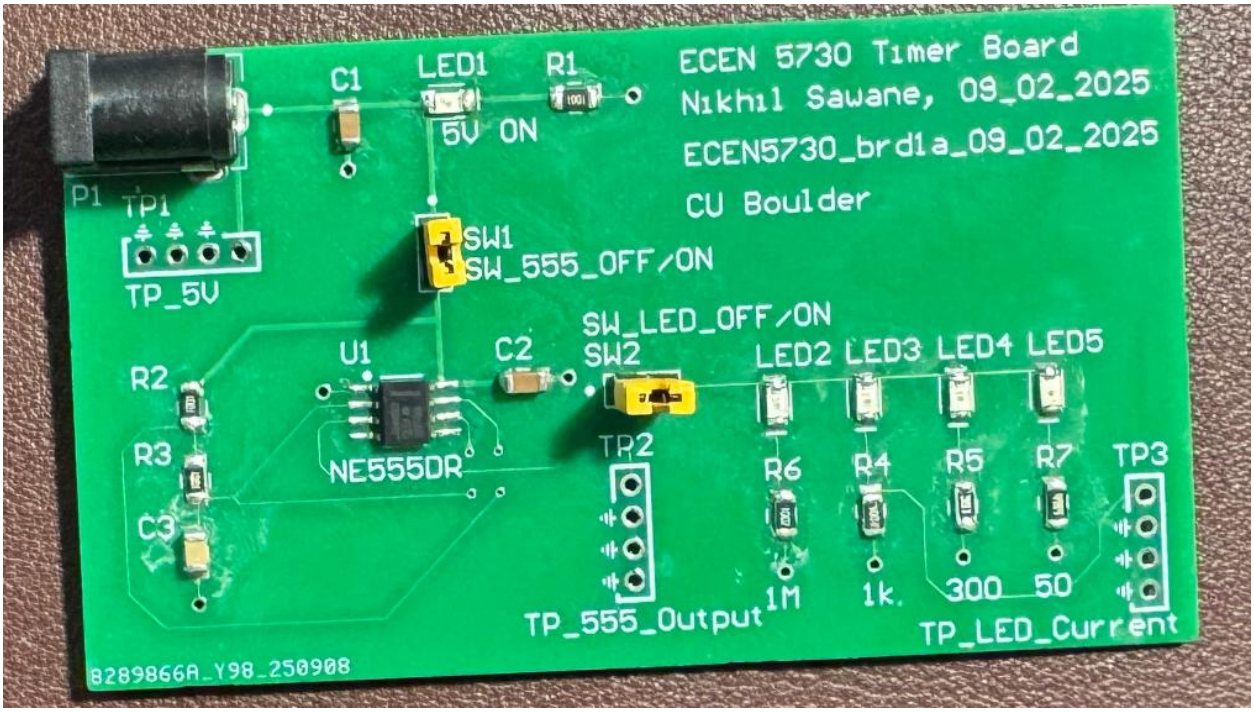
Figure 3 555 timer layout done in Altium Software

Assembly

- **Before soldering:**



- **After soldering:**



What it means to work

1. Board is powered with a 5 V AC to DC regulator and can be measured at TP1.
2. When the power is on, indicator LED Should turn ON.

3. The 555 timer outputs a square wave signal with a frequency and duty cycle of about 500 Hz and 66% and rise time is around 100 ns. This can be measured at the test point TP2.
4. 555 timer output should drive four LEDS of different brightnesses, controlled by resistors. LED with 47Ω should be the brightest.
5. The current through the LED with 1KΩ can be measured at test point TP3.

Bring-Up and Testing

To confirm functionality:

6. Applied 5 V supply → power LED turned on
7. Measured ~500 Hz square wave with ~66% duty cycle at TP2
8. LEDs lit with brightness proportional to resistor values (47 Ω brightest)
9. Verified current through 1 kΩ LED path at TP3

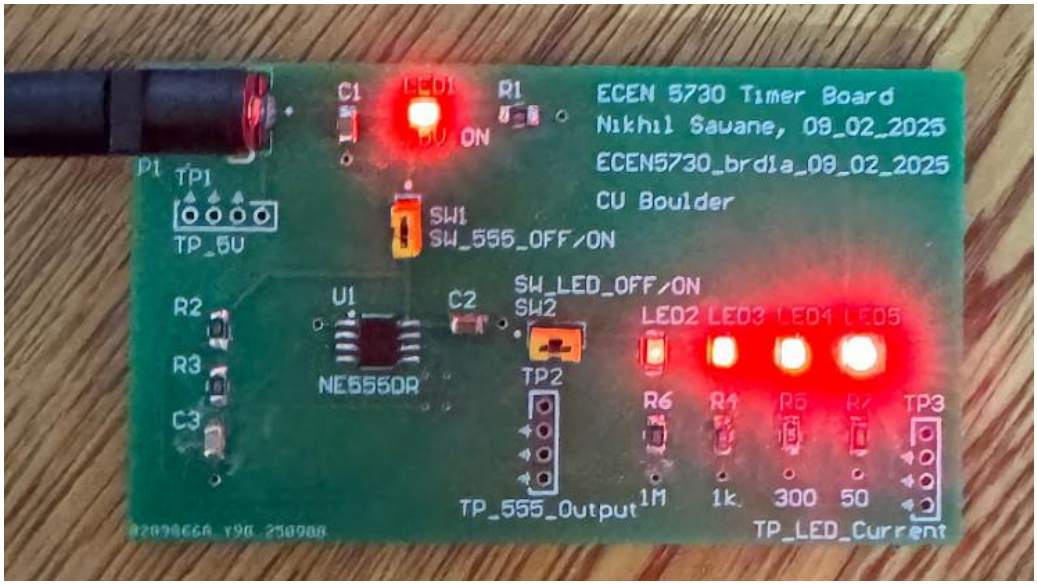


Figure 5 Fully Functioning board

Measurements and Analysis

- **Internal resistance of 555 output:**
  - No-load Vout = 5.1 V
  - Loaded Vout = 3.76 V
  - Equivalent load resistance = 38.9 Ω
  - Rth ≈ 14 Ω

This shows the 555 behaves as a non-ideal source with finite output resistance.

- **Scope captures:**

On the oscilloscope, **Channel 1 (yellow)** was connected to the 555-timer output at TP2, while **Channel 4 (pink)** monitored the power rail at TP1.
By toggling the isolation switch (SW2), I compared the 555 output with and without the LED load attached. The measured waveforms closely matched the expected theoretical behavior. The main difference observed was a reduction in output voltage when the LEDs were connected. This drop occurs because the 555 timer has a finite output resistance, so part of the voltage is lost across it under load. Effective output resistance can be estimated using the Thevenin equivalent model.

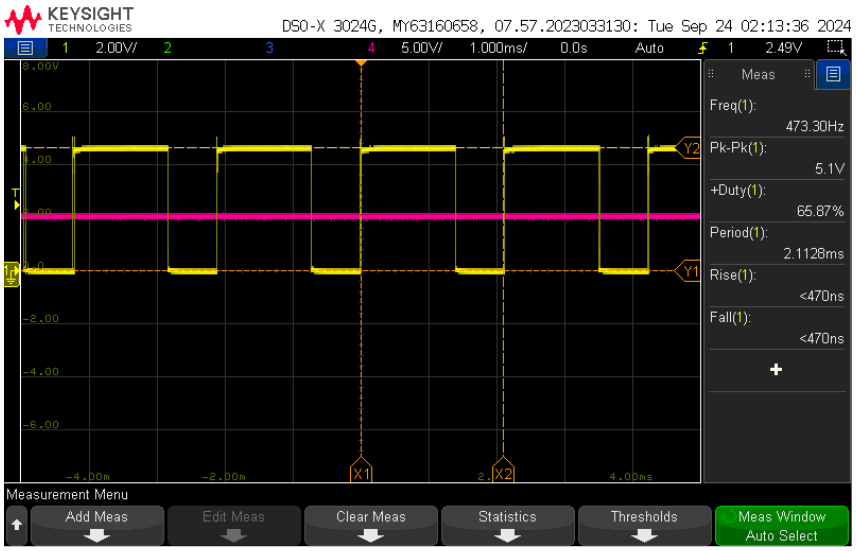


Figure 6 555 timer without load

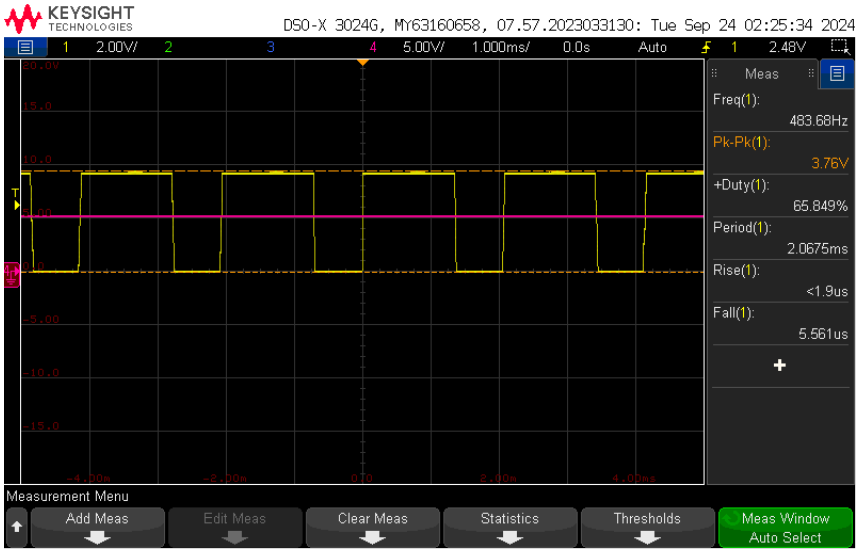


Figure 7 555 timer with load

When no load was attached, the 555 output showed a rise time of about 90.8 ns and a fall time of about 27.6 ns. Correspondingly, the noise observed on the 5 V rail was roughly 26 mV during the rising

edge (Figure 8) and 2.8 mV during the falling edge (Figure 9). This noise results from the voltage drop across the inductance of the power rail's signal–return loop, driven by the rapid change in current (dI/dt) as the 555 output switches. Because the fall transition is relatively fast, the associated noise is small. Even though the rise transition produced about 26 mV of disturbance, this level is still minor and does not pose an issue for the circuit's operation.

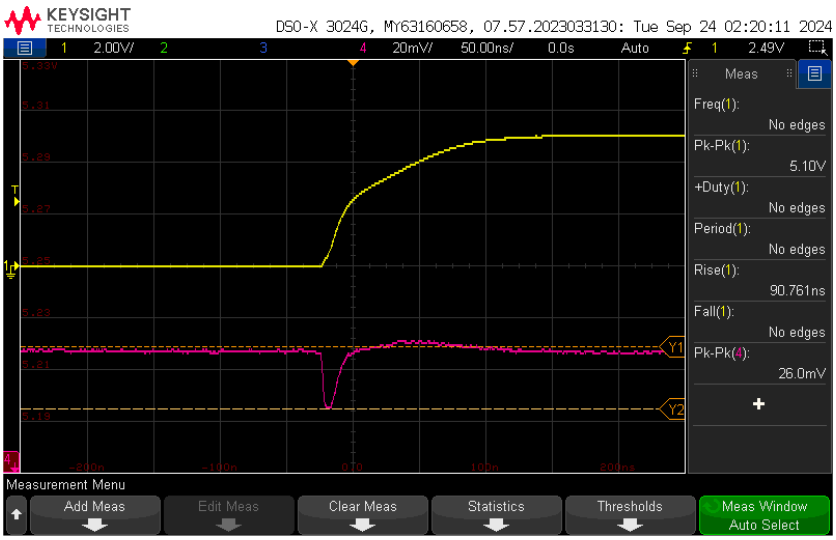


Figure 8 555 output rise time without load

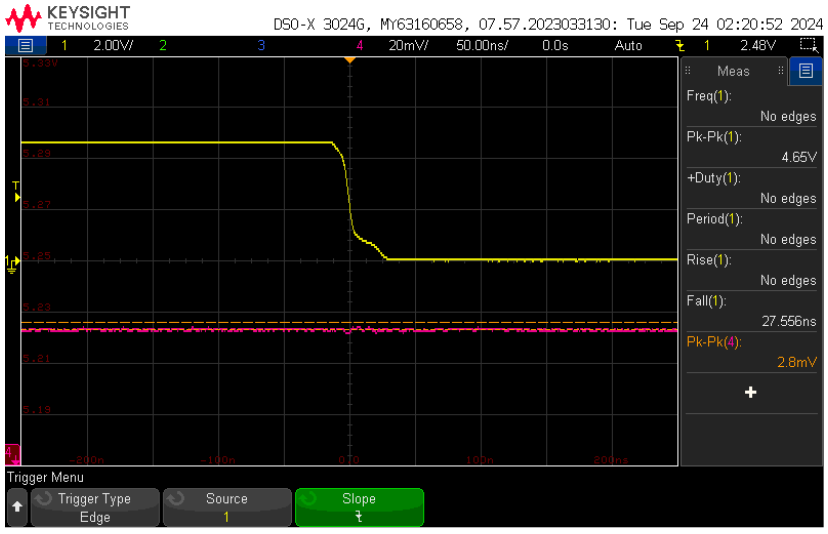


Figure 9 555 output fall time without load

With the load connected, the 555 outputs exhibited a rise time of about 48.7 ns and a fall time of about 50 ns. The corresponding disturbances on the 5 V rail measured roughly 26 mV during the rising edge (Figure 10) and 3.6 mV during the falling edge (Figure 11). Although the rise time was faster compared to the no-load case, the presence of a decoupling capacitor placed close to the 555-timer helped suppress additional noise, preventing any increase in supply rail fluctuations.

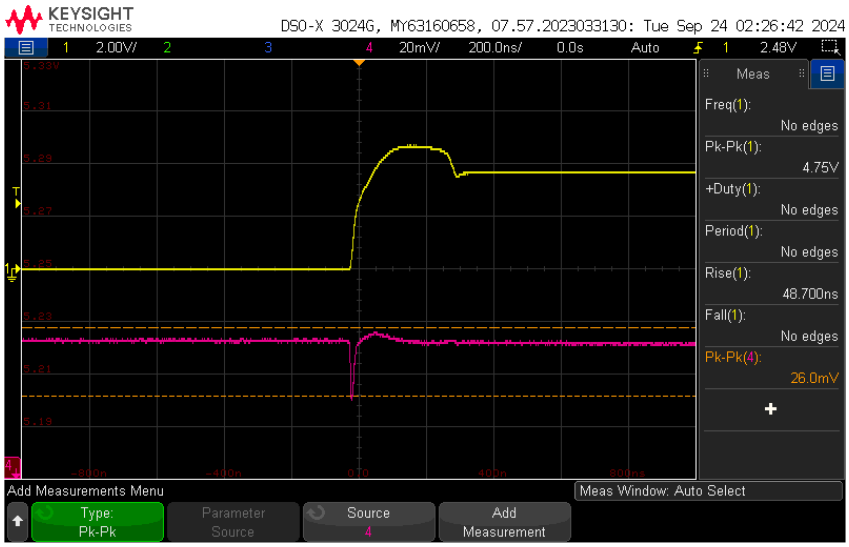


Figure 10 555 output rise time with load

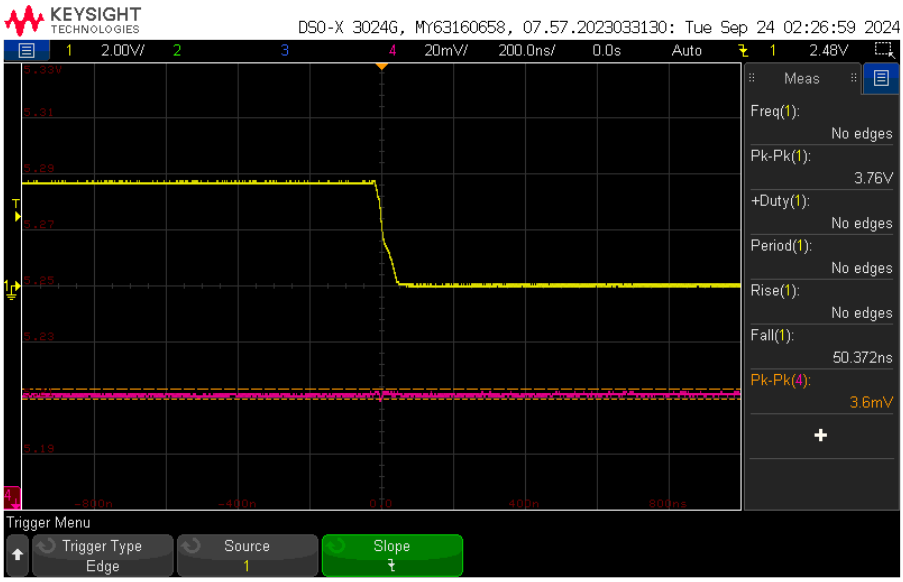


Figure 11 555 output fall time with load

When monitoring the 555 output together with the voltage across the 1 kΩ resistor, the current through the resistor was obtained using Ohm's law, yielding approximately 1.66 mA. In this measurement setup, Channel 1 (yellow) captured the 555 output at TP2, while Channel 4 (pink) displayed the voltage drop across the 1 kΩ resistor at TP3.

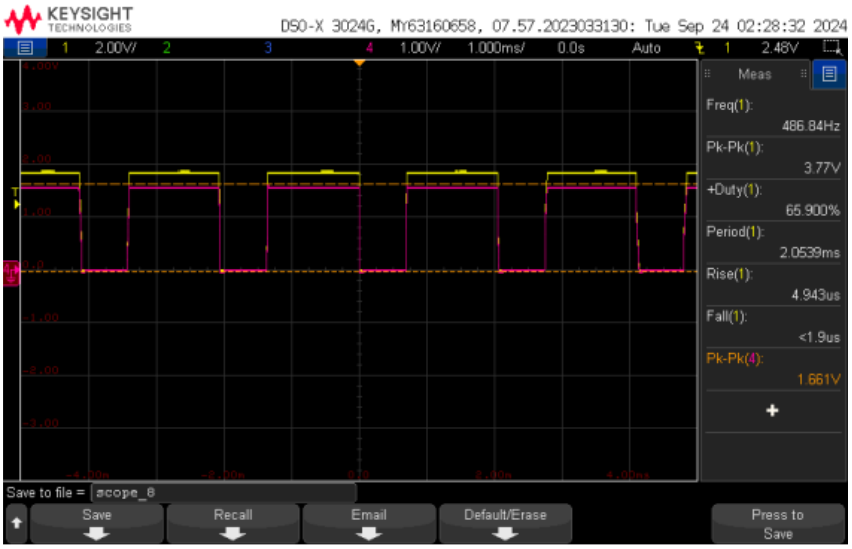


Figure 12 Voltage across 1KΩ

- **Switching noise:**
    - About 26 mV on rising edge
    - A few mV on falling edge
    - Decoupling capacitors helped keep noise small

Figure of Merit (Measured Values)

Condition	Vpp (V)	Frequency (Hz)	Duty Cycle (%)	Notes
No load	5.1	473	65.9	Slight overshoot
With load	3.8	484	65.8	Drop due to Rth ≈14Ω

Best Design Practices Implemented

1. **Minimized unique components –** Selected parts were chosen to reduce the number of distinct values wherever possible.
2. **Proper decoupling –** A capacitor was placed close to the 555 timer to effectively minimize loop inductance in the power rail and suppress switching noise.
3. **Clear test point labeling –** Test points were clearly marked to avoid soft errors and make measurements straightforward.
4. **Debugging features –** An indicator LED and isolation switches were added to speed up troubleshooting during bring-up.

5. **Return path integrity –** A continuous ground plane was maintained, and no cross-unders were used, which helps avoid crosstalk issues.
6. **Appropriate trace widths –** Power traces were routed with 20 mil width to support higher currents, while signal traces were kept at 6 mil width for maximum routing density at the lowest fabrication cost.

Conclusion

This lab gave me hands-on experience with the full PCB workflow: defining requirements, schematic/layout in Altium, soldering, bring-up, and testing. I observed how non-ideal effects like internal resistance of the 555 and supply rail noise show up in practice. The biggest lesson was that decoupling capacitors are critical in stabilizing the power rail and minimizing switching noise. I also learned the importance of debugging skills—something as small as a cold solder joint can prevent the circuit from functioning.
