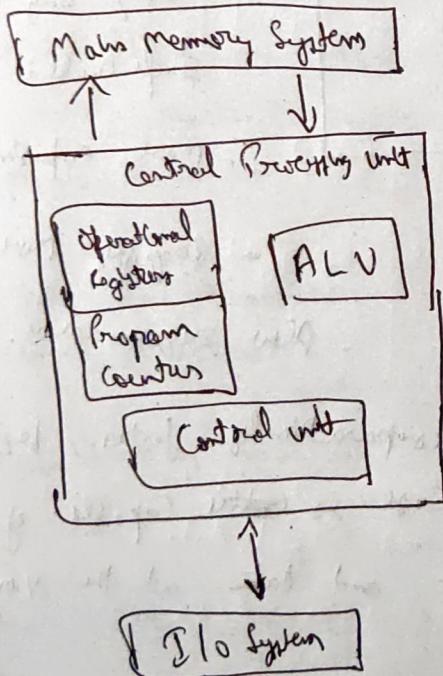


# MCA - I

1) With a diagram explain Von-Neumann & Harvard architecture

## Von-Neumann Architecture

- Ans
- Von-Neumann architecture is a digital computer architecture, whose design is based on the concept of stored Program Computers where program data and instruction data are stored in same memory.
  - Same physical memory address is used for instructions and data.

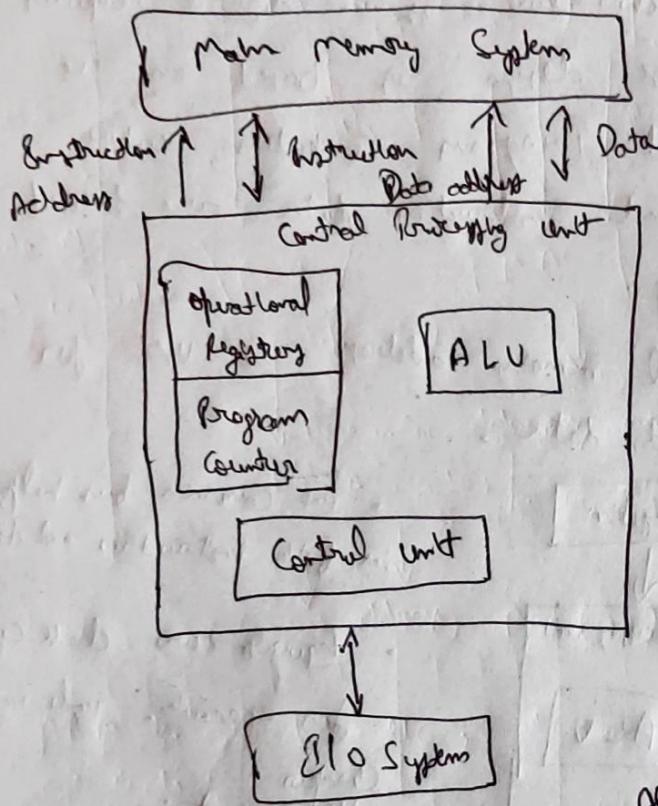


- One common bus helps in both instructions and data.
- Requires two clock cycles for executing single inst.
- ~~High~~ Cost.
- Requires less hardware.
- Requires less space.
- Speed is comparatively slower.

## Von Neumann arch

## Harvard Architecture:

- Modern type of Computer ~~arch~~ that follows concept of Relay-based model by Harvard Mark-1.
- Has separate physical address for storing and occupying both instruction & data.



• Harvard arch uses separate buses for transfer of both data & instructions.

• executes any instruction using only one single cycle.

• More expensive.

• Requires more space.

• Also requires more hardware.

- Overall execution speed is comparatively faster, because the processor, in this case is ~~not~~ capable of fetching both instructions and data at the very same time.
- Controlling process becomes comparatively complex with this architecture - because it basically fetches data & instruction simultaneously.

## 2) Let's compare RISC vs CISC machines.

### RISC

- emphasis on software to optimize instruction set.
- hard wired unit of programming in the RISC.
- Requires multiple register sets to store the instruction.
- has simple decoding of instruction.
- pipeline is simple.
- Load and Store are independent in the register to register a program's interaction.
- It has more transistors on memory Registers.
- Execution time of RISC is very short.
- Program written for RISC needs more space in memory.

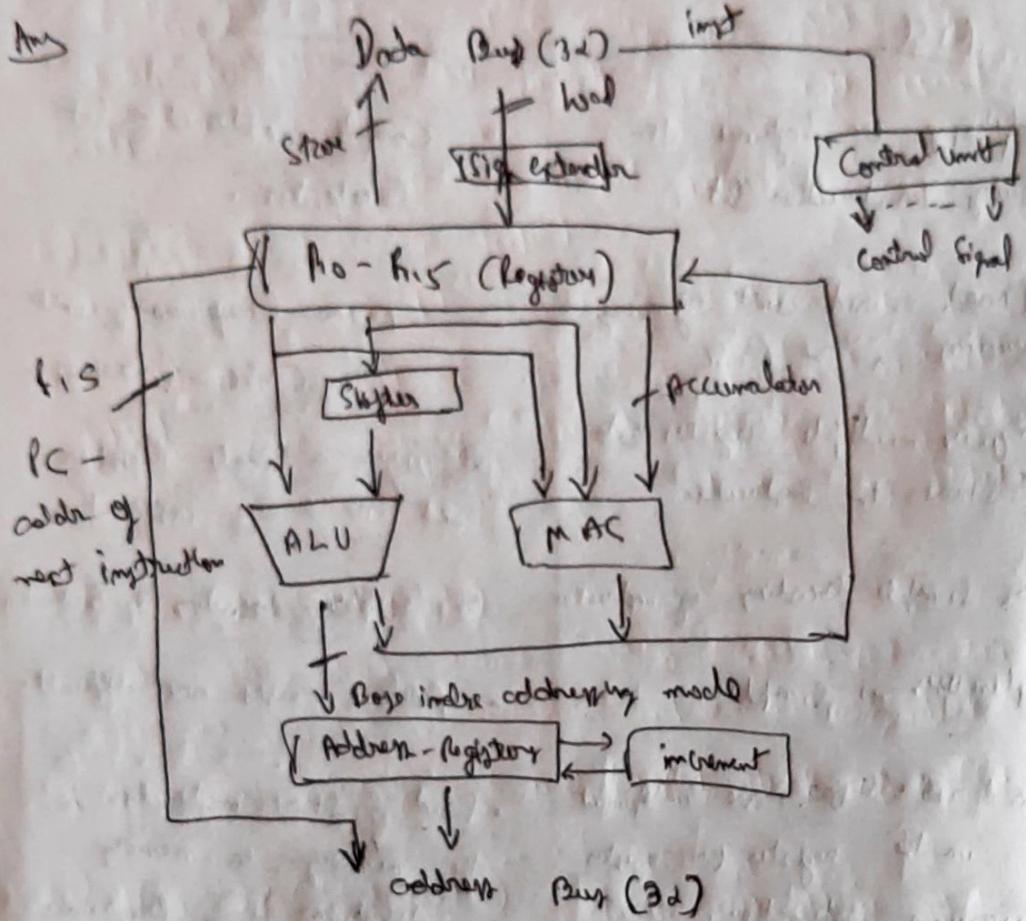
Example: ARM, PA-RISC, AVK, Alpha etc.

### CISC

- Complex instruction Set Computer.
- Micro-Programming unit in CISC Processor.
- Requires a single Register set to store instruction.
- Complex decoding of instruction.
- Pipeline uses are difficult.
- Load & Store instruction in the memory-to-memory interaction of a program.
- CISC has Transistors to store complex instructions.
- Execution time of CISC is longer.
- takes less space in memory.

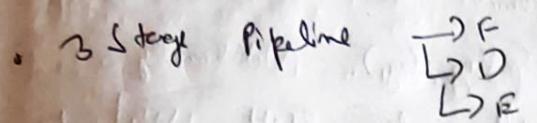
Example: VAX, System 360, Ami) Motorola 68000 family.

3.) With a next decoder, explain ALU & multiplication?



- ALU is 32-bit ALU, it can do 32-bit operation in one cycle.
- 32-bit ALU
- 32-bit Data Bus
- ALU does not allow mis-aligned data.
- Advanced RISC Machine - RISC architecture. all instructions are of one type - i.e. 32-bit
- 32-bit address Bus.
- n-bit address Bus, then 2^n memory  $2^{32} = 4\text{GB}$  mem

von-neumann Model.



- 32 registers - 32 bits each, 16 available at time.
- ARM works on "Load-Store" model.
- 7 operating modes, 7 interrupt (exceptions), 7 addressing modes.
- 3 data formats (8, 16, 32 bits).

h) with a neat diagram, explain programming model of ARM?

<u>System and User</u>	<u>FIQ</u>	<u>Supervisor</u>	<u>User</u>	<u>IRQ</u>	<u>Undefined</u>
R0	R0	R0	R0	R0	R0
R1	R1	R1	R1	R1	R1
R2	R2	R2	R2	R2	R2
R3	R3	R3	R3	R3	R3
R4	R4	R4	R4	R4	R4
R5	R5	R5	R5	R5	R5
R6	R6	R6	R6	R6	R6
R7	R7	R7	R7	R7	R7
R8	R8 - FIQ	R8	R8	R8	R8
R9	R9 - FIQ	R9	R9	R9	R9
R10	R10 - FIQ	R10	R10	R10	R10
R11	R11 - FIQ	R11	R11	R11	R11
R12	R12 - HLR	R12	R12	R12	R12
R13	R13 - FIQ	R13 - SVC	R13 - abt	R13 - und	R13 - und
R14	R14 - FIQ	R14 - SVC	R14 - abt	R14 - und	R14 - und
R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)	R15 (PC)

ARM - State (Program Status

register.

CPSR

SFSR  
SFSR-fiq

SFSR  
SFSR-SVC

CPSR  
SFSR-abt

CPSR  
SFSR-und

CPSR  
SFSR-und

1.) There are 7 modes of operation.

In each mode, programmer has access to 16 GPRs (R0-R15) and a CPSR (Flag Reg.). Additionally a SFR PSR is also available in all modes except user/system mode.

2.) R15: PC (Program Counter)

PC gives a 32-bit address of instruction to be fetched. This address is put on the address bus and instruction is fetched from memory through the 32-bit data bus. PC is incremented after every instruction is fetched.

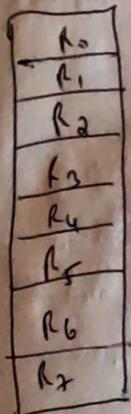
3.) R14: LR (Link Register)

If stores the return address (value of PC) when we perform a BL instruction. While returning back to main program the value of LR will be put back into PC.

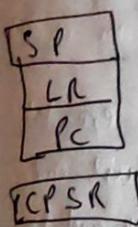
4.) R13: SP (Stack Pointer): Holds the address of top of stack.

5.) Additionally there are some Banked Registers that are available in specific operating modes.

Q) Write a neat diagram to explain the Programmer model for Thumb?



- The Thumb instruction set consists of 16-bit instructions that act as a compact shorthand for a subset of 32-bit instructions of standard ARM. Every Thumb instruction could be instead encoded via the equivalent 32-bit ARM instruction.
- ARM contains only one instruction set: The 32-bit set. When it's operating in the Thumb state, the processor simply expands the smaller shorthand instructions fetched from memory into their 32-bit equivalents.

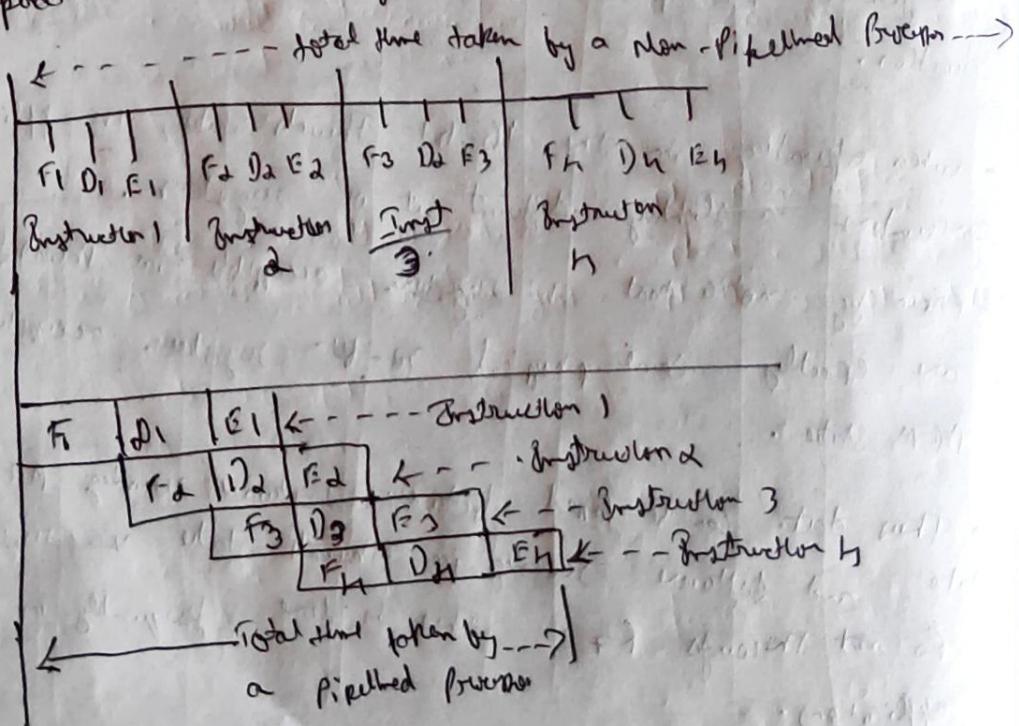


Thumb Programmer Model: The difference b/w the two equivalent instructions lies in how the instructions are fetched & interpreted prior to execution, not in how they function.

- when operating in the 16-bit Thumb state, the application encounters a slightly different set of registers.
  - From fig notice that 12 registers acceptable in Thumb state are exactly same physical 32-bit registers acceptable in ARM state.
- Thus data can be passed between software running ARM state and software running in Thumb state via registers R0 ~~to~~ through R7. This is done frequently in actual applications.

(b) What is pipelining? Explain 3-stage pipeline of ARM?

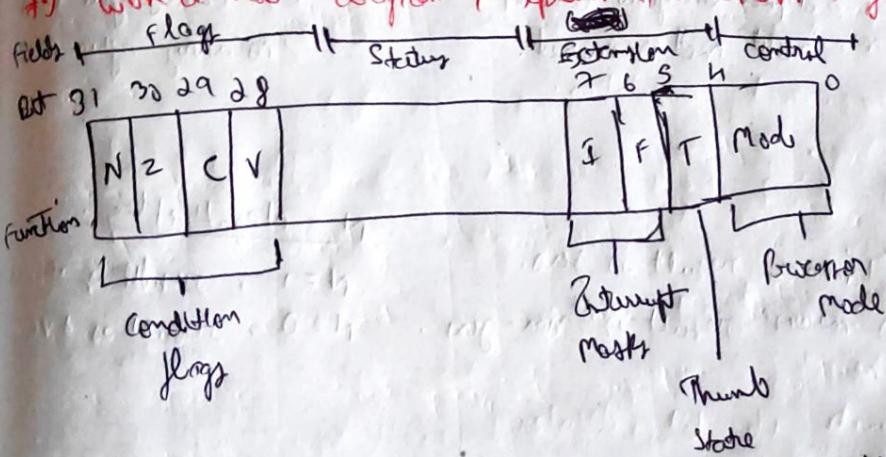
- Pipelining means overlapping various stages of an instruction cycle to improve processor performance.
- ARM can implement a 3-stage pipeline.  
The instruction cycle is divided into 3 distinct stages of fetch, decode and execute. So when one instruction is being executed, the next one is being decoded and subsequently next one is being fetched.
- This means three different instructions are being performed at the same time.
- After the first instruction has been completely executed, every subsequent instruction gets completed in just one cycle, which is needed for execution. The fetch and decode operations have already been performed in background.



- Fetch (F): Here instruction will be fetched from the memory location specified by P.C.
- Decode (D): Here the opcode is decoded and control signals are produced for execution.
- Execute (E): Here the decoded instruction is executed.

Pipelining fails during a branch as it assumes that a program is always executed in a sequential manner. During decode stage of the control unit recognizes that it is a branch inst, then subsequent inst that has been fetched has to be discarded.

7) With a neat diagram, explain the CPSR register.



- Current Program Status Register (CPSR) holds the current status of program.
- When an exception (interrupt occurs), the value of CPSR is saved into SPSR, before invoking the ISR.
- While returning back to main program, the value of SPSR is put back into CPSR to restore the previous state of original program.

- T: Thumb State: If  $T=1$ , then processor is in Thumb state.  
 $T=0$ , then Processor is in normal ARM state.
- F: Fast Interrupt Mask  
 If  $F=1$ , FI are disabled (masked)  
 If  $F=0$ , Fast Interrupts are enabled (un-masked).  
 A fast interrupt occurs through the nFIQ pin.

### • I: Interrupt Request Mask

- If  $I=1$ , then normal interrupts are disabled (masked)
- If  $I=0$ , then normal interrupts are enabled (un-masked)

### Condition flags

#### • V: Overflow flag

$V=1$ , signed overflow occurred.  
 $V=0$ , ~~not~~ not occurred.

#### Carry flag

$C=1$ , Carry after MSB  
 $C=0$ , no carry after MSB

#### • Z: Zero flag:

$Z=1$ , means result is zero.  
 $Z=0$ , 0 means result is non-zero.

#### N - Negative flag:

$N=1$ , result is negtive.  
 $N=0$ , result is +ve.

## Q) Explain 7 different modes of ARM:

### a.) User Mode:

- normal mode in which all user programs are executed.
- only non-privileged mode.
- has limited access to memory, I/O components and flags.
- All the other modes can be entered through different kinds of exceptions.

### b.) Fast Interrupt Request Mode:

- Entered when a high Priority interrupt occurs through nFIQ Pin.
- As this mode is used for high Priority interrupts, the ISR should be executed with minimum latency.

### c.) Interrupt Request Mode:

This is a normal Interrupt Mode and is invoked when a low Priority interrupt occurs on the nIRQ Pin.  
Here ~~the~~ interrupt latency is much and nested interrupts are allowed.

### d.) Supervisor Mode: enters this mode on reset.

- It is used to execute the BIOS Program.
- This mode can also be invoked by programmer by SWI.

### e.) Abort mode: entered when an unsuccessful attempt is made to access a memory location. ~~use~~ the protection mechanism. Some locations are not accessible in some of modes.

f.) undefined mode: It used to enter undefined instruction.  
This generally occurs when a Co-Processor instruction is encountered but a Co-Processor is not present in System.

g.) System mode: This is a Privileged version of User mode.  
The user ~~not~~ program can invoke this mode to gain full control over CPSR and memory. Needless to say, this mode should be used very carefully by programmers.

9.) Explain nomenclature in ARM?

• ARM 7TDMs Processor.

- 32 bit Processor Advanced Machine.

T → Thumb Architecture machine.

D → Debug Extension.

M → Enhanced extension.

E → Encrypted emulation.

ARM {T} {D} {M} {E} {J} {F} {S}

T → Series.

D → memory management unit.

M → Cache.

T → Thumb 16-bit decoder.

D → JTAG Debugger.

M → embedded ICE (Emulation)

E → Enhanced instruction by DSP.

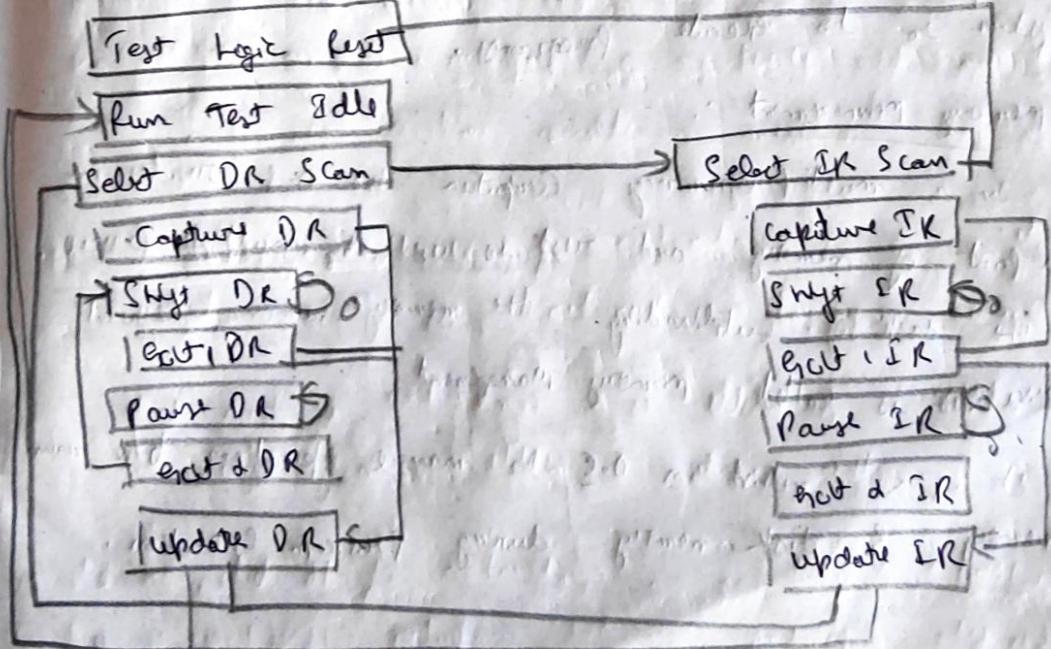
J → JAVA acceleration by Zarafa.

F → Floating Point.

S → Synthesizable Version.

10.) What is JTAG? Explain JTAG State Diagram.

- JTAG has become a standard in embedded Systems and it is available in every microcontroller or FPGA on market.
- If we have programmed a micro controller there is a strong chance that we have used JTAG or the related Standard.
- JTAG is Joint Test action group, is an industry Standard for verifying designs & Testing PCB's after manufacture.
- It implements standards for on chip instructions.
- It specifies the use of a dedicated debug port implementing serial communication interface for low-overhead access.
- Test access port (TAP) that implements a stateful protocol to access a set of test registers.



11.) What is Single Tasking? Give examples of Single tasking applications.

Ans Single tasking means doing one task at a time with as little distraction & interruption as possible.

e.g. Micro controllers are known as computer on chips. They are designed to perform a single task only because its processing power as well as memory is not suitable for installing an OS.

(a) What is MMU? Why MMU required? Give examples of Processor with MMU support?

Ans The memory can be defined as a collection of data in a specific format. It is used to store a instruction & processed data. The memory Comprises a large array or group of words, or bytes, each with its own location. The primary motive of a computer system is to execute programs.

Memory Management:

- In a multi programming Computer the O.S resides in a part of memory and rest is used by multiple process. The task of subdividing the memory among different processes is called memory management.
- It is a method in O.S to manage operations b/w main memory & disk memory during process execution.

Why required?: Allocate & de-allocate the memory before & after the process execution.

- To keep track of used memory space by process.
- To minimize fragmentation issues.
- To maintain data integrity while executing of process.

Eg: IBM System/360 model 67, IBM System 1370

ARM: Application based processor implement MMU designed by ARM's virtual memory system architecture.

13.) What is Endianess? List the types? Give examples.

It is a computer science term that describes how data is stored. Specifically, it defines which end of a multi-byte data type contains the most significant values.

Types:

(i) Big-Endian:

Is the most common way to store binary data. It places the most significant value first, followed LSB.

Eg: Big-Endian representation of integer 123 places the hundreds value (1) first, followed by the tens value (2) then the ones value (3).

(ii) Little-Endian: Little-Endian stores the least-significant value first, followed by increasingly more significant values. For example, the number 123 in little-Endian notation is [321], The text string "ABC" is [CBA].

14.) Write a C-program to find endianness of a given number?

Ans. #include < stdio.h >  
int main()

unsigned int x = 0x76543210;

char \*c = (char \*) ;

If (\*c == 0x10)

{  
printf ("underlying architecture is little endian\n");  
}

else

{  
printf ("underlying architecture is big endian\n");  
}

return 0;

}

15) Explain:  
a) bit: Is the smallest unit of information that can be stored in a computer. Bits in computer are grouped to form a large unit of information.

b) Byte: Is a combination of eight bits. Eight bits ~~represent~~ represent a character & is called a byte.

c) nibble: A nibble is a combination of four bits, in other words a nibble is half byte.

d) word: A word is a combination of 16 bits, 32-bits or 64 bits depending on the computer. 16 is known as quad word.

Length	Name	Example
1	Bit	0
4	Nibble	1011
8	Byte	1011 0101
16	Halfword	1011 0101 1001 0001

(b) Explain the word align and half word align in ARM memory.

Ans Different processors have different definition of words  
 for 32-bit Processors, a word is 32 bit (4 bytes).  
 As the name implies, a halfword is 16 bit for a  
 16-bit Processor a word is 16-bit (2 bytes),  
 for 8-bit Processor word is 8 bits..

word alignment: The stored addresses are adjacent and can be divided by 4, the last two digits are 00.

Halfword alignment: That is the stored address are adjacent & divisible by 2, that is last bit is 0:

> ARM arch requires 32-bit ARM instructions that must word aligned & stored in memory & 16-bit Thumb.

Instructions require halfword, aligned & stored.  
 ∴ in ARM state the value of R15 is always divisible by 4, that is lowest 2 bits of the R15 register are always 00.

In Thumb state the value of R15 is always divisible by 2, lowest bit of the R15 register always 0.

18.) Explain the following Addressing modes in ARM  
a) Three address b) Two address c) Single address  
Instructions with respect to ARM.

### Three address Instructions:

This has 3 address field to specify a register or memory location. Program codes are much short in size but number of bits per instructions increase. Program codes are These instructions make creation of program much easier but it does not mean that program will run much faster because now instructions only contain information but each micro-operation will be performed in one cycle only.

Eg: ADD R<sub>3</sub>, R<sub>1</sub>, R<sub>2</sub>

$$R_3 = R_1 + R_2$$

### Two address Instruction:

Here two address can be specified in the instruction. In the one address instruction, the result was stored in the accumulator, here the result can be stored in different locations, i.e. registers or memory locations. But requires more number of bit to represent the address.

Eg: MOV R<sub>1</sub>, R<sub>2</sub>

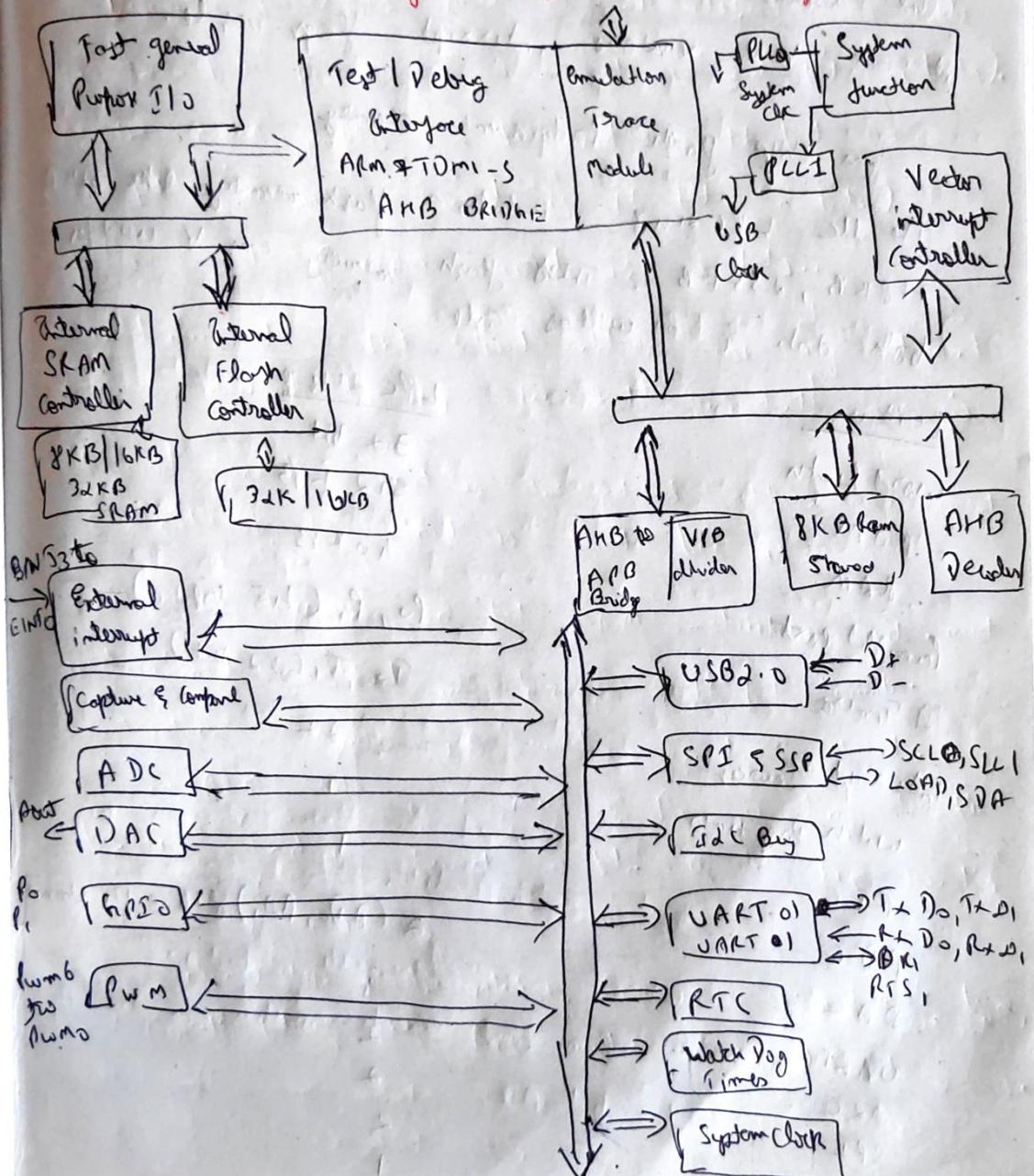
$$R_1 \leftarrow [R_2]$$

one address instruction: This uses an implied accumulator register for data manipulation and other is in the register memory location. Implied means that the CPU already knows that one operand is in the accumulator. So there is no need to specify it.

e.g.: LDR addr

Acc  $\leftarrow$  (addr)

19.) Explain the LPC 2148 micro-controller Block Diagram:



→ ARM7 based LPC2148 micro-controller.

- The ARM7 is a 32-bit general purpose microprocessor & it offers some of the features like little power utilization and high performance. The architecture of an ARM is depended on the principle of CISC.

- Interrupt Sources:

Every peripheral device consists of a single interrupt line called to the (vector interrupt controller), although it can have various interrupt flags inside.

on-chip flash program memory

The mc. LPC2148 includes a flash memory like 32KB, 128KB, 256KB. This flash memory can be used for both data & as well as code.

Features

word length

ROM

RAM

parallel port

2 timers

interrupt sources

watch dog timer

RTC

ADC

DAC

UART

I2C

SPI

USB

LPC2148

32 bit

512 KB

no FB

P0, P1 (16 bits)

T0, T1 (32 bit)

22

1

1

2 (A/D, AD, )  $\times 16 = 12$  channels

1

2

2

2

1

Q7) Explain the software tools involved and processing the `main.c` source file with a neat diagram.

Ans Software analysis and design includes all activities which help the transformation of requirement specification into implementation. Requirement specification specify all functional and non-functional expectations from the software. These requirement specifications come in the shape of human readable and understandable documents, to which a computer has nothing to do.

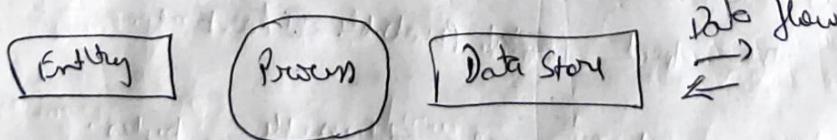
### Design tools:

Data flow diagram: Data flow diagram is graphical representation of flow of data in an information system. It is capable of depicting incoming data flow, outgoing data flow & stored data.

### Types of data flow diagram (DFD)

- Logical DFD: This type of DFD concentrates on the system process & flow of data in the system.
- Physical DFD: This type of DFD, shows the data flow is actually implemented in system.

### DFD Component



Structure Chart: Structure chart is a chart derived from Data flow diagram. It represents the system in more detail than DFD.

### H IPO Diagram

H IPO diagram is a combination of two organized method to analyse the system and provide the means of documentation.

### Structure English

It is the responsibility of higher software management to brief accurate information to the programmers to develop accurate yet fast code.

Q.) Explain the LPC 2148 microcontroller GPI/O pins.

Ans GPI/O: General purpose Parallel Input / Output.

GPI/O registers control the device pins which are not linked to a particular peripheral function. The device pins can be arranged as I/P or O/P.

Individual registers allow for clearing any number of I/P's concurrently. The O/P register value can be read back and the present condition of the port pins.

- GPI/O registers are mapped to the processor but used for the best ~~possible~~ possible I/O time.

- These registers are addressable bytes.

- The total value of a port can be written in the only instruction 10-bit PDL.

The microcontroller like LPC2148 has 32-bit GPIO

i) Port 0

ii) Port 1

Port 0 is a 32 bit Port

- out of these 32 pins, 28 pins can be configured as either general purpose input or output.
- 1 of these 32 bit can be configured as general purpose output only.
- 3 of these 32 pins are reserved. Hence they are not available for use.

Port 1 is also 32 bit Port. Only 16 of these 32 pins are available for use as general-purpose input or output.

iii) With a neat diagram, explain band rate, Bit rate.  
Explain the calculations.

Band rate: Band rate is number of signal units per second. It can be defined as per second number of changes. Band rate focuses on data transmission. Band rate can be calculated as Band rate,  $R = \text{Bit Rate} / \text{the number of bits per baud}$ .

Band rate calculation uses  $\text{band-rate} = \text{Bit Rate} / \text{Number of bits}$ . To calculate the Band rate, Band rate refers to the number of signal or symbol changes that occur per second.

Bit rate: Refers to the rate at which data is processed or transferred. It is usually measured in seconds ranging bps for smaller values to Kbps and mbps.

Bit rate is also known as bit rate or data rate.

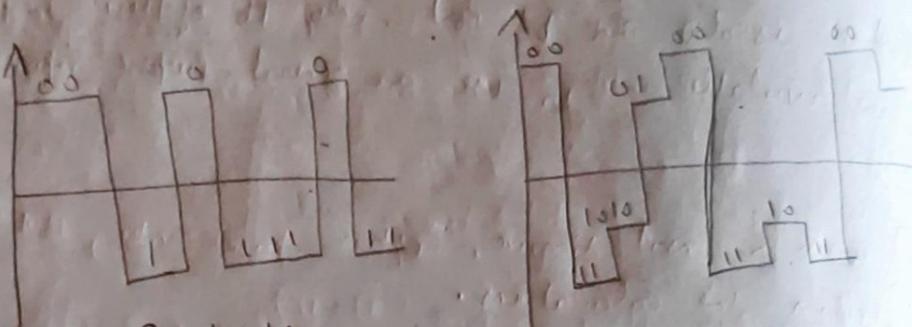
$$BR \text{ (bit rate)} = D \div T$$

where

BR = Bit rate

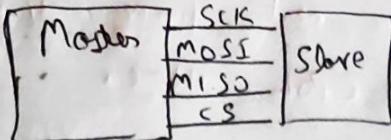
D = Amount of data

T = Time (in Seconds)



Q2.) With a neat diagram explain working and features of SPI Protocol?

Ans SPI is called as a 4-wire bus as it requires four wires for its communication. In case of single Start Select (SS) is not required so SPI requires more communication lines in contrast to VART, I<sup>2</sup>C, USB etc.



- \* SCK or SCLK : serial clock, clock generated by master.
  - \* MOSI or SD<sub>0</sub> : master output slave input, data output from master.
  - \* MISO or SD<sub>1</sub> : master input slave output, data output from slave.
  - \* SS : Slave Select, often an active low input of slave.
- When multiple slave devices are used, an independent slave select line is connected from master to each slave device.

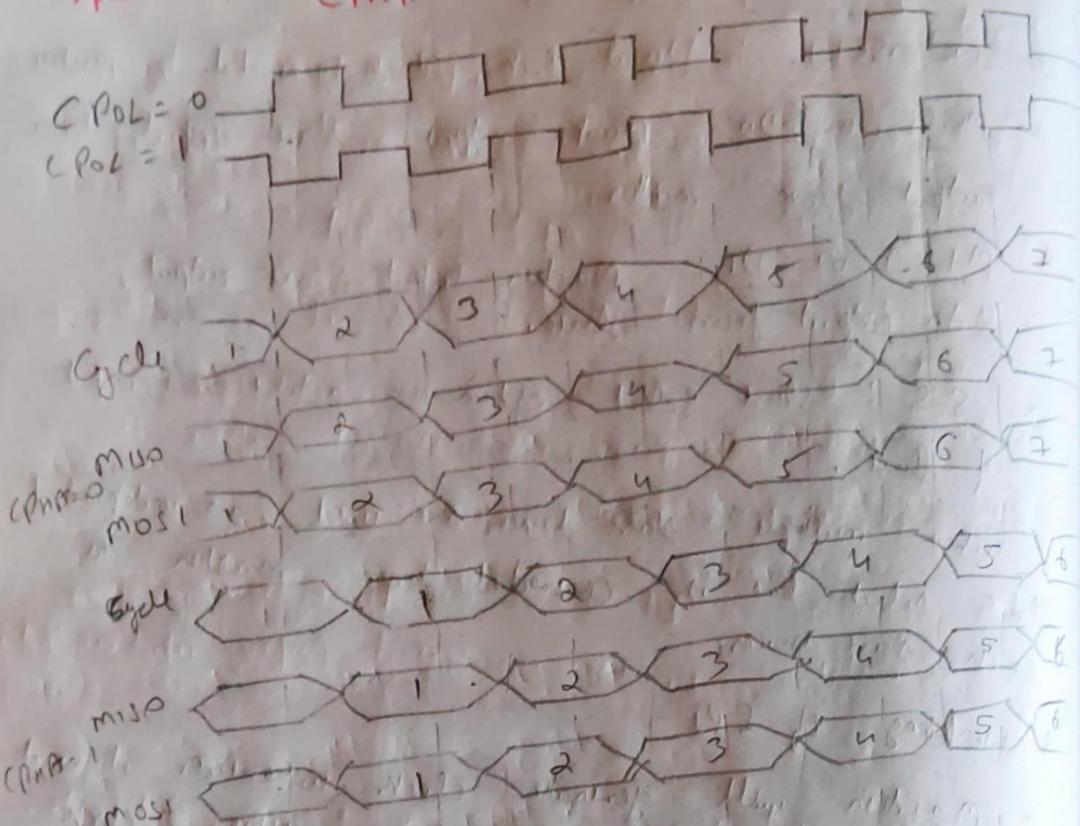
#### \* working of SPI

- master will generate clock whenever it wants to write data to a slave device. After 8 clock pulses data in the master device and data in the slave device ( $B_7 - B_0$ ) is transferred to the master device.

#### Features of SPI:

SPI Signals include the standard serial clock, master in slave out, master out slave in bi-directional serial data and slave select. The SPI master component should be used any time the PSoC device is required to interface with one or more SPI slave devices.

23.) In SPI, with a neat timing diagram, explain the CPNA and CPOL usage.



- **CPOL significance:** This defines whether the clock signal will be high ( $CPOL = 1$ ) or low ( $CPOL = 0$ ) before the chip select goes low.
- **CPHA significance:** It tells whether the data is sampled during first edge of the clock signal or the second edge of the clock signal.

If  $\text{CPHA} = 0$ ,  $\text{CPOL}$  has to be '0' so that sampling can happen during the rising edge of signal.

If  $\text{CPOL} = 1$ ,  $\text{CPOL}$  has to be 1 so that the sampling can happen during the rising edge of signal.

Mode	$\text{CPOL}$	$\text{CPHA}$
0	0	0
1	0	1
2	1	0
3	1	1

Ques.) With a neat diagram explain the features of I<sub>2</sub>C and its working?

Ans) I<sub>2</sub>C stands for Inter - Integrated circuit it is a bus interface connection protocol. Incorporated into devices for serial communication.

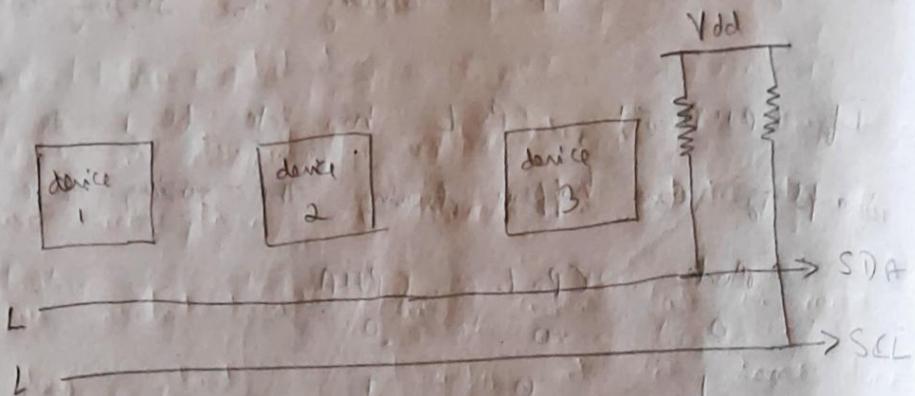
Working of I<sub>2</sub>C Communication Protocol.

It uses only 2 bi-directional open - drain lines for data communication called SDA & SCL. Both these lines are pulled high. Serial Data (SDA): Transfer of data take place through their pin.

Serial Clock (SCL): It carries the clock signal.

I<sub>2</sub>C operates in 2 modes:

- \* Master Mode.
- \* Slave Mode.



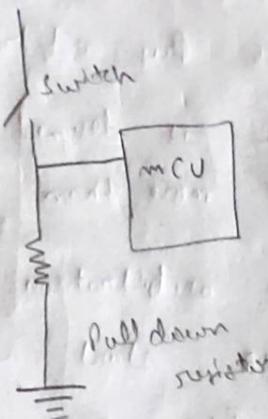
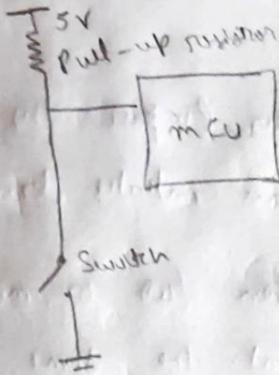
According to I<sup>2</sup>C protocols, the data line can not change when the clock line is high, it can change only when the clock line is low.

- 1.) Start Condition - 1 Bit.
- 2.) Slave address - 8 Bit.
- 3.) Acknowledgment - 1 Bit.

### Features of I<sup>2</sup>C.

- It supports multiple data speed: Standard mode, fast mode, fast-mode plus, high speed mode, and ultra fast mode, I<sup>2</sup>C communication.
- Independent master, slave and monitor functions.
- Supports both multi-master and multi-slave with slave function.
- 10-bit addressing supported with software.
- I<sup>2</sup>C operates in 3 speeds 100 Kbps, 400 Kbps, 3.4 Mbps.

Q5) With a neat diagram, explain the pull up and pull down resistors?



#### Pull-up resistor:

A pull up resistor is used to establish an additional loop over the digital components while making sure that the voltage is well-defined even when the switch is open.

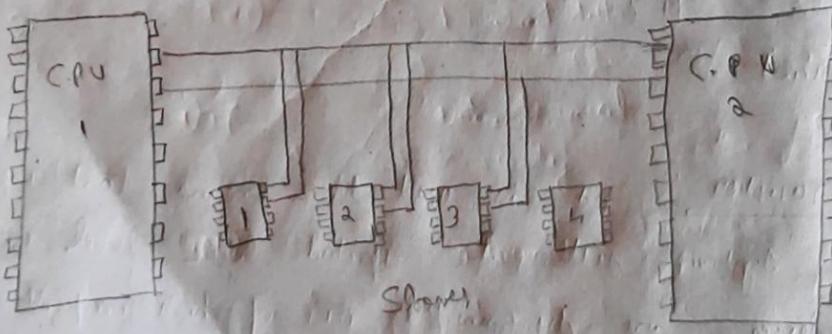
It is used to ensure, that a wire is pulled to a high logical level in the absence of an input signal. Pull up resistor with a fixed value was used to connect the voltage supply and a particular pin in the digital logic circuit.

Pull-down resistor: It is used to ensure that input to logic systems settle at expected logic level whenever external device are disconnected or of high impedance. to ensure that the wire is at a defined low logic level when there are not active connections with other devices. The pull-down resistor holds the logic signal near to zero volts when no other device is connected.

26) With a neat diagram, explain the concept of arbitration in I2C.

### I2C Bus arbitration

- I2C is designed for multi master purpose this means that more than one device can initiate transfer.
- Bus arbitration allows when two or more masters start a transfer at the same time.
- The I2C Bus was originally developed as a multimaster bus, meaning more than one device initiating transfer can be active in the system.
- When using only one master on the Bus there is no real risk of corrupted data, except if a slave device is malfunctioned or if there is a fault condition involving the SDA / SCL bus.



When MCU 1 sends a start condition and sends an address all slaves will listen. If the address does not match the address of CPU 2, this device has to hold back any activity until the bus becomes idle again after a stop condition.

As long as the two MCUs monitor what is going on the bus and as long as they are aware that a transaction is going on because the last ~~issued~~ issued command was not a STOP, there is no problem.

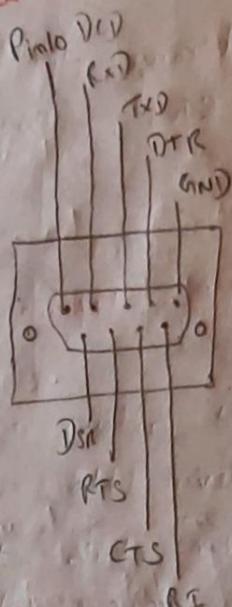
Q) What is clock stretching? Explain clock stretching in I<sub>2</sub>C?

A) Clock Stretching: It allows an I<sub>2</sub>C slave device to force the master device into a wait state. A slave device may perform clock stretching when it needs more time to manage data, such as store received data, or prepare to transmit another type of data.

Clock Stretching in I<sub>2</sub>C: I<sub>2</sub>C devices can slow down communication by stretching SCL. During an SCL low phase, any I<sub>2</sub>C device on the bus may additionally hold down SCL to prevent it from rising high again, enabling them to slow down the SCL clock rate or to stop I<sub>2</sub>C communication for a while.

This is also referred to as clock synchronization. In an I<sub>2</sub>C communication the master device determines the clock speed. Unlike RS232 the I<sub>2</sub>C bus provides an explicit clock signal which defines master and slave frame synchronization exactly to a predefined baud rate.

28) Explain the working of DB9 pins and handshaking with the modem?



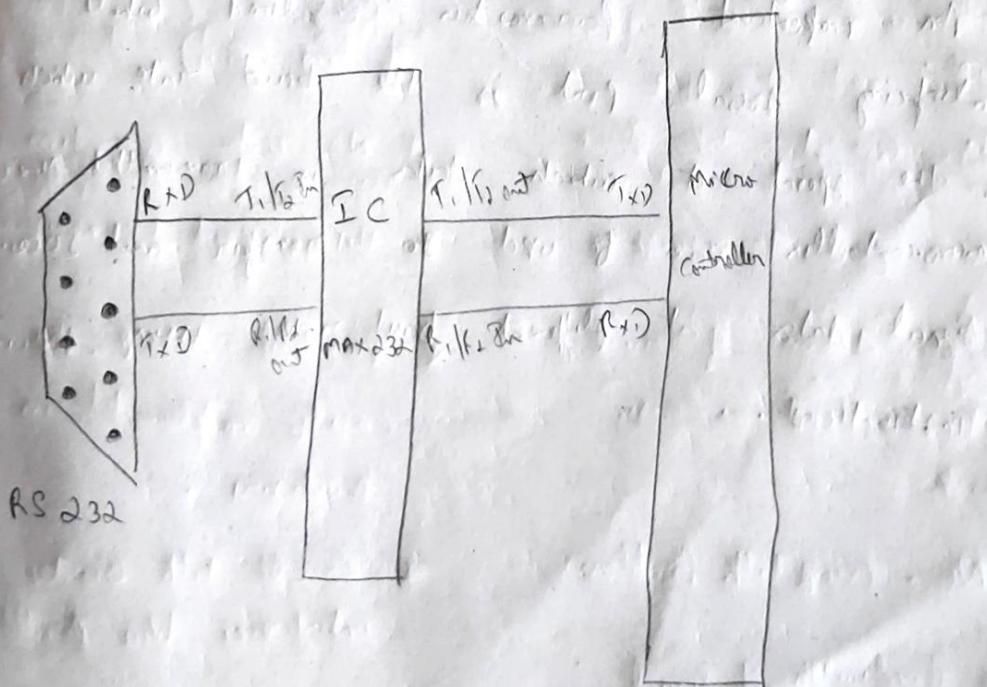
PIN	SIGNAL	SIGNAL NAME	DTE Signal direction
1.	DCD	Data Carrier detect	In
2.	RxD	Receive data	In
3.	TxD	Transmit data	out
4.	DTR	Data terminal ready	out
5.	GND	Ground	-
6.	DSR	Data Set ready	In
7.	RTS	Request to send	out
8.	CTS	Clear to send	In
9.	RI	Ring indicator	In

## Hand Shaking Modem

A modern handshake is what occurs when the receiving modem answers the phone call and the two modems begin to communicate. Before anything else happens, the modem must evaluate the quality of the time, negotiate error control protocols and data compression that they can both support and work out what the most suitable connection speed should be, based on the conditions.

This process is called as hand shake.

Q9.) Explain the RS 232 connection with a micro controller?



- Serial devices collect data from sensor and need to send it to another unit, like a computer for further processing. Data transfer / communication is generally done in two ways serial and parallel. In parallel mode data transfer is fast and uses more number of lines.

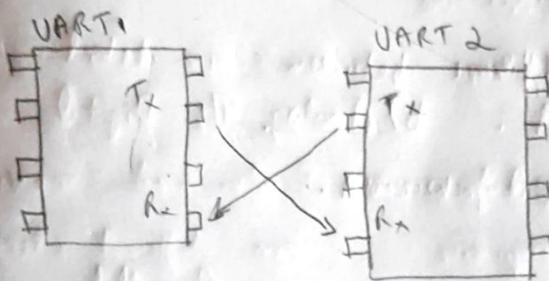
. Serial communication on the other hand, uses only one or two data lines to transfer data and is generally used for long distance communication.

In serial communication the data is sent as one bit at a time.

. An important parameter considered while interfacing serial port is the Band rate which is the speed at which data is transmitted serially. microcontroller can be used to transfer and receive signed data at different band rate using several instructions.

### 30.) Explain The Frame In UART Communication.

Ans In UART communication, two UART's communicate directly with each other. The transmitting UART converts Parallel data from a controlling device like a CPU into Serial form. Transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving device.

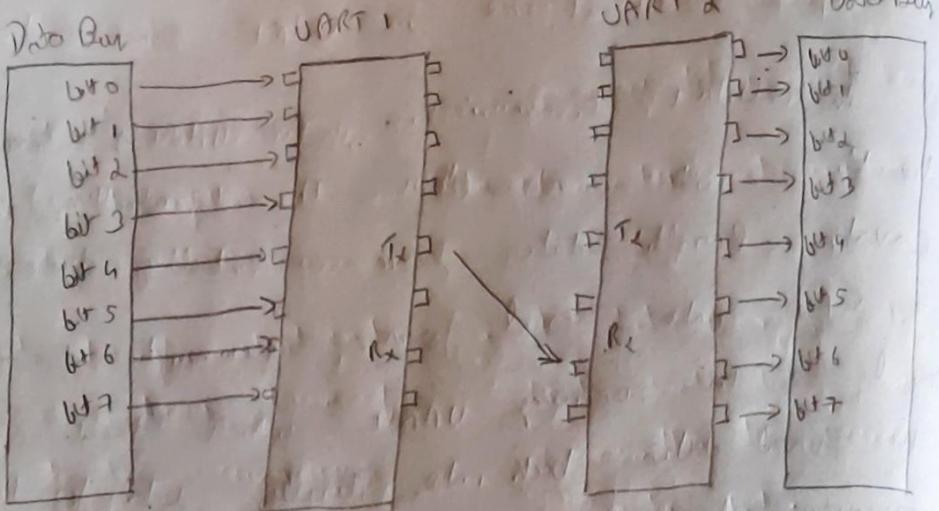


UART transmit data asynchronously, which means there is no clock signal to synchronize the output of bits from the transmitting UART to the Sampling of bits by the receiving UART.

#### How UART Works:

The UART that is going to transmit data receive the data from a data bus. The data bus is used to send data to the UART by another device like a CPU, memory or micro-controller.

Data is transferred from the data bus to the transmitting UART in parallel form.



- 3) Explain the difference between in detail  
 a) Serial v/s Parallel.      b) Analog v/s Digital  
 c) Synchronous v/s Asynchronous.

### Serial

- Data is transmitted bit after the bit in a single line.
- Data Congestion takes place.
- Low Speed transmission.
- Implementation of Serial links is not an easy task.
- No. Cross talk Problem.
- The Bandwidth of Serial wire is much higher.

### Parallel

- \* Data is transmitted simultaneously through group of lines (Bus).
- \* No Data Congestion.
- \* High Speed Transmission.
- \* Parallel data links are costly implemented in hardware.
- \* Cross talk creates interference b/w parallel bus.
- \* The bandwidth of Parallel wires is much lower.

## Analog

transmitted modulated signal  
by analog is nature

Amplitude, frequency or phase  
variations in the transmitted  
signal represent the information  
or message.

Noise immunity is poor  
for Am, but improved  
for Fm and Pm.

Coding is not possible

Fm is used for multiplexing

Analog modulation systems  
are A.M., F.M., P.M., PAM, PAM  
etc.

## Digital

\* Transmitted signal is digital  
is train of digital pulses.

- Amplitude width, or position  
of the transmitted pulses  
is constant. The message is  
transmitted in the form of code  
words.

- Noise immunity is excellent.

- Coding techniques can be used  
to detect and correct the errors.

- TDM is used for multiplexing

- Digital modulation system  
are Pcm, Dm, ADm, Dpm etc.

## Synchronous

- Communicated in real-time.
- Creates interruption in work day.
- A data transfer method that sends a continuous stream of data to the receiver using regular timing signals that ensure both transmitter and receiver are synchronized with each other.

## Asynchronous

- Communicated in well timed.
- Eliminates interruption.
- A data transfer method that sends data from transmitter to receiver with parity bit.
- Sender and receiver operate on the same clock frequencies.
- Slower.
- Uses Start and Stop bit.
- After Random or irregular time interval.
- Used in email.
- Used in chat rooms and video Conferencing.