Project-III

EE619A

31/Oct/2022

- This is a group project.
- This project involves the design, layout and characterization of the commonly used logic gates.
- Please divide the work between the designers, such that the roles/responsibilities of the two members can be clearly identified.

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1 Introduction

The following standard cells are to be designed in complementary static CMOS logic. The number of standard cells to be designed is same as the number of designers in your team. For e.g., a two-member team has to choose any of the two standard cells listed below.

- 2-input NAND gate
- 2-input NOR gate
- 2-input XOR gate
- 2-input XNOR gate

LTspice and Electric tools are recommended for this project. If you are using a different tool, the TAs may not be able to help you with the inclusion of the technology files, DRC rules and LVS files.

2 Requirements

The following needs to be completed for each gate that you have chosen.

1. Design the gates at schematic level. Clearly, explain how the sizes of the NMOS and PMOS transistors were chosen.
2. Simulate the propagation delay of the gates for both rise and fall output edges for a fanout capacitance of 5 fF and 50 fF at schematic level. For the input signal, use rise time and fall time as 20 ps.
3. Estimate the power consumption for 5 fF and 50 fF fanout capacitance. Assume that both inputs are shorted and a 1 GHz clock is given as input.
4. Complete the layout adhering to the following guidelines. The fanout capacitance is not part of the layout.
   (a) All gates should have the same height. The widths can vary across the designs.
   (b) The VDD rail should be at the top. The width of the VDD rail should be same for all gates.
   (c) The GND rail should be at the bottom. The width of the GND rail should be same for all gates.
5. Clear the design rule check (DRC). This ensures that your design can be fabricated by the foundry.
6. Clear the layout vs schematic (LVS) check. This ensures that your schematic and layout have the same underlying netlist (except for the interconnect parasitics).
7. Repeat step 2 and step 3 with the layout-extracted simulations.

3 Model files

Please use the model file available at https://home.iitk.ac.in/~imon/HighFreqAnalog/assignments/45nm_HP.pm

4 Tool Details

- Please refer to the attached PDF **ElectricGuidelines.pdf**.
- You may also refer to https://www.youtube.com/watch?v=ErLhlCKonE0 for a tutorial on tool installation.

5 Report format

Please include the following details in the report.

- Information about the team, standard cells designed and details on who designed each standard cell.

First standard cell

- Screenshot of the schematic.
- Explanation on how the transistor sizes were chosen.
- Screenshot of the layout with the DRC log. Mark the height and width of the layout in the screenshot.
- Screenshot of the layout with the LVS log.
- Table with the propagation delay values from the schematic and the layout for 5 fF and 50 fF fanout loads.
- Tabulate the power consumption from the schematic and layout-extracted simulations.
- Waveform from transient analysis of input and output transitions of the gate for one of the input conditions. Mention the input conditions clearly in the figure caption. Give the waveforms from both schematic and layout-extracted simulations for both 5 fF and 50 fF fanout.

Second standard cell Repeat the same as the above.