National Institute of Technology Karnataka, Surathkal

Department of Information Technology

Evaluation Plan

1st Semester B.Tech 2018-19

1	Code of the subject	IT110
2	Title of the subject	Theory and Lab
3	LTP (Lecture – Tutorial – Practical) and Credits Structure	4 Credits (3-0-2)
4	Name of the Course Instructor	Prof. Ram Mohana Reddy Guddeti
5	Evaluation Scheme	1 Mid Term: 25M (Theory – 20; Lab - 5) 2 End Term: 50M (Theory – 40; Lab - 10) 3 Continuous Lab Evaluation: 10M (Record + Observation) 4 Tests: 15M (5 + 10)
	Extra Test/Exam	No extra test will be given under any circumstances except medical reasons with duly attached certificate from Residential Medical Officer, HCC, NITK.
6	List of Text Books	1. M. Morris Mano: Logic and Computer Design Fundamentals. 2. M. Morris Mano and Michael D. Ciletti: Digital Design with VERILOG HDL. 3. B Holdsworth and R C Woods: Digital Logic Design , 4th Ed., Elsevier, 2003.

Course Instructor

Prof. Ram Mohana Reddy Guddeti

Digital System Design Lab (IT110) Experiments list

Experiment No	Title of experiments	Laboratory work
1	Design a Digital Circuit for half adder as well as full adder. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
2	Design circuits for half subtractor as well as full subtractor. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
3	Design a circuit for 3-to-8 line decoder using NOT gates and AND gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
4	Design a circuit for 2-to-4 line decoder with enable inputs using NOT gates and NAND gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
5	Design a circuit for Octal-to-Binary encoder using OR gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
6	Design a circuit or 4-to-1 line multiplexer using only NOT gates, AND gates and OR gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
7	Design a circuit or quadruple 2-to-1 line multiplexer using NOT gates, AND gates, and OR gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
8	Design a circuit for the Boolean equation $(A,B,C)= \sum(1,3,5,6)$ using multiplexer circuit. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	

Digital System Design Lab (IT110) Experiments list

Experiment No	Title of experiments	Laboratory work
9	Design a circuit for SR Latch using only NOR gates. Repeat the experiment using only NAND gates. Verify the truth table as well as Boolean equation of the same circuits by conducting the experiment.	
10	Design a JK Latch using NOR gates and AND gates. Verify the truth table (Characteristics table) of the same circuits by conducting the experiment).	
11	Design a T Latch using NOR gates and AND gates. Verify the truth table (Characteristics table of the same circuits by conducting the experiment).	
12	Design a D Latch using NAND gates. Verify the truth table (Characteristics table of the same circuits by conducting the experiment).	
13	Design a circuit for SR Flip-Flop using only NOR gates with clock pulse. Verify the truth table (Characteristics table) of the same circuits by conducting the experiment).	
14	Design a JK Flip-Flop with clock pulse. Verify the truth table (Characteristics table) of the same circuits by conducting the experiment).	
15	Design a D Flip-Flop with clock pulse. Verify the truth table (Characteristics table) of the same circuits by conducting the experiment).	
16	Design a T Flip-Flop with clock pulse. Verify the truth table (Characteristics table of the same circuits by conducting the experiments).	
17	Design a Clocked Master-Salve SR Flip-Flop (using only NOR gates and NOT gates). Verify the truth table as well as Boolean equation of the same circuits by conducting the experiments	
18	. Design a Clocked Master-Salve JK Flip-Flop (using NAND gates and NOT gates. Verify the truth table (Characteristics table) of the same circuits by conducting the experiments	
19	Design a Three Bit Binary counter using T Flip-Flop. Verify the Excitation table of the same by conducting the experiments.	
20	Design a Counter using JK Flip-Flop that has a repeated sequence of 000-001-010-100-101-110. Verify the Excitation table of the same circuits by conducting the experiments.	