Chapter 18

Sequential Circuits: Flip-flops and Counters

1. Design a counter that has the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, 7. Use RS flip-flops.

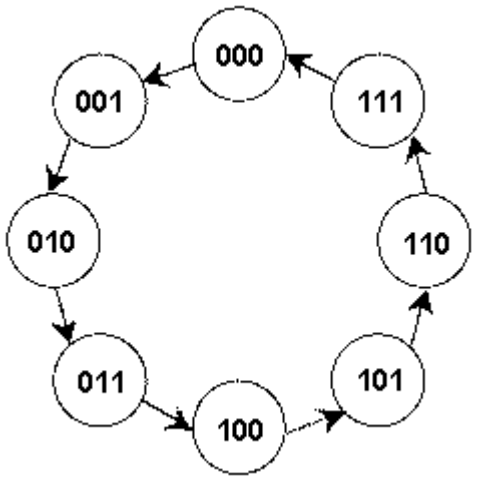


Fig. 1.1 State diagram of a 3-bit binary counter

Solution:

Step 1: Since it is a 3-bit counter, the number of flip-flops required is 3.

Step 2: Let the type of flip-flops be RS flip-flops.

Step 3: Let the three flip-flops be A, B, C.

Step 4: The state table is as shown in Table 1.1.

Table 1.1 State table

Present State	Next State
A B C	*A B C*
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

Step 5: The next step is to develop an excitation table from the state table, which is shown in Table 1.2.

Table 1.2 Excitation table

Output State Transitions		Flip-flop inputs		
Present State	Next State			
A B C	*A B C*	RA SA	RB SB	RC SC

0 0 0	0 0 1	X 0	X 0	0 1
0 0 1	0 1 0	X 0	0 1	1 0
0 1 0	0 1 1	X 0	0 X	0 1
0 1 1	1 0 0	0 1	1 0	1 0
1 0 0	1 0 1	0 X	X 0	0 1
1 0 1	1 1 0	0 X	0 1	1 0
1 1 0	1 1 1	0 X	0 X	0 1
1 1 1	0 0 0	1 0	1 0	1 0

Step 6: Now transfer the RS states of the flip-flop inputs from the excitation table to Karnaugh maps in Tables 1.3–1.8 to derive a simplified Boolean expression for each flip-flop input.

Table 1.3 K-map for RA

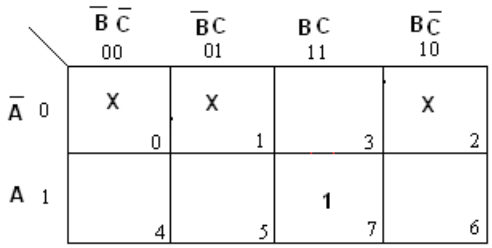


Table 1.4 K-map for SA

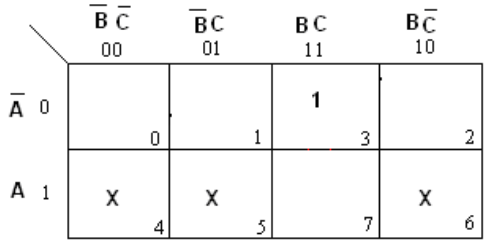


Table 1.5 K-map for RB

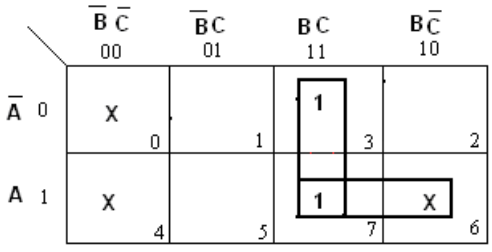


Table 1.6 K-map for SB

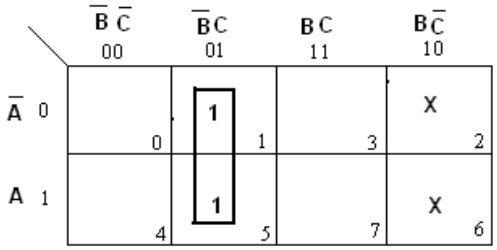


Table 1.7 K-map for RC

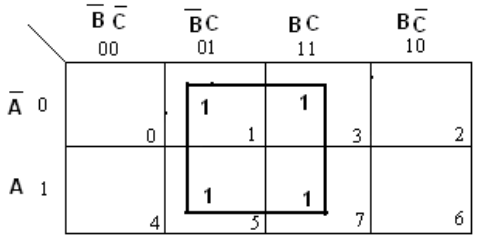
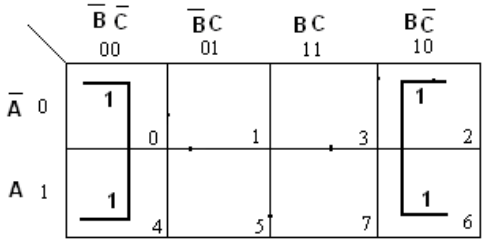


Table 1.8 K-map for SC



From the K-maps, the following expressions for the *R* and *S* inputs of each flip-flop are obtained:

$RA = ABC$

$SA = \overline{A}BC$

$RB = AB + BC = B(A+C)$

$SB = \overline{B}C$

$RC = C$

$SC = \overline{C}$

Step 7: The final step is to implement the combinational logic from the equations and connect the flip-flops to form the sequential circuit. The complete logic of a 3-bit binary counter is shown in Fig 1.2.

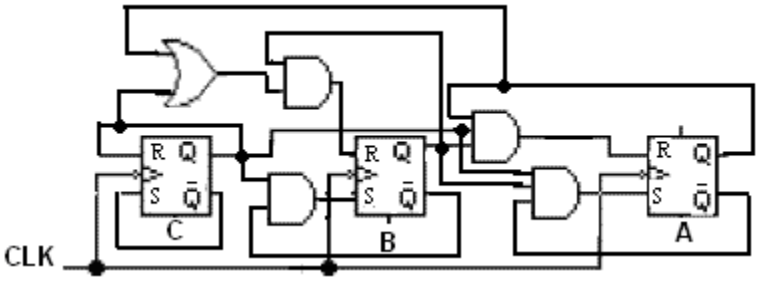


Fig. 1.2 Logic diagram of a 3-bit binary counter

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2. Design a counter with the following binary sequence: 1, 2, 5, 7 and repeat. Use JK flip-flops.

Solution:

Step 1: Since it is a 3-bit counter, the number of flip-flops required is three.
Step 2: Let the type of flip-flops be RS flip-flops.
Step 3: Let the three flip-flops be A,B,C.
Step 4: The state table is as shown in Table 2.1.

Table 2.1: State table

Present State	Next State
A B C	*A B C*
0 0 1	0 1 0
0 1 0	1 0 1
1 0 1	1 1 1
1 1 1	0 0 1

Step 5: The next step is to develop an excitation table from the state table, which is shown in Table 2.2.

Table 2.2: Excitation table

Output State Transitions		Flip-flop Inputs		
Present State	Next State			
A B C	*A B C*	JA KA	JB KB	JC KC
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	1 0 1	1 X	X 1	1 X
1 0 1	1 1 1	X 0	1 X	X 0
1 1 1	0 0 1	X 1	X 1	X 0

Step 6: Now transfer the JK states of the flip-flop inputs from the excitation table to Karnaugh maps in Tables 2.3–2.8 to derive a simplified Boolean expression for each flip-flop input.

Table 2.3 K-map for JA

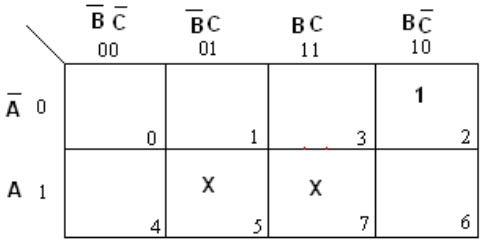


Table 2.4 K-map for KA

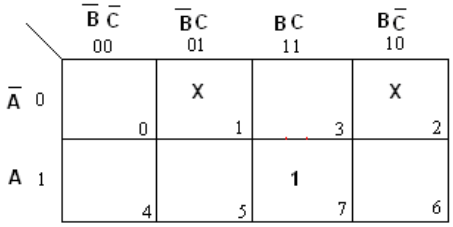


Table 2.5 K-map for JB

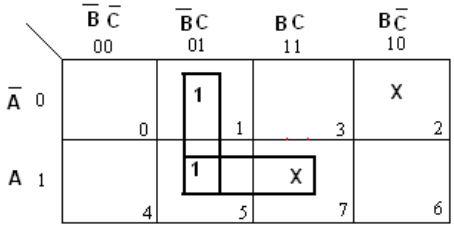


Table 2.6 K-map for KB

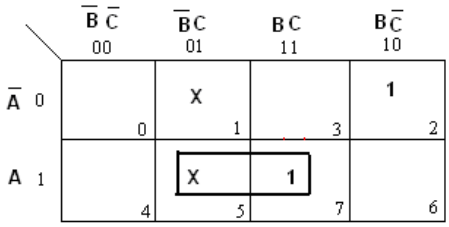


Table 2.7 K-map for JC

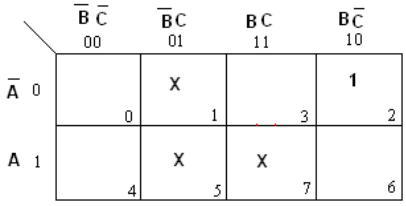


Table 2.8 K-map for KC

A \ $\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	1 (1)	(3)	X (2)
A 1 (4)	(5)	(7)	(6)

From the K-maps, the following expressions for the J and K inputs of each flip-flop are obtained:

$JA = JC = \bar{A}B\bar{C}$

$KA = ABC$

$JB = \bar{B}C + AC$

$KB = AC$

$KC = \bar{A}\bar{B}C$

Step 7: The final step is to implement the combinational logic from the equations and connect the flip-flops to form the sequential circuit. The complete logic of a counter is shown in Fig. 2.1.

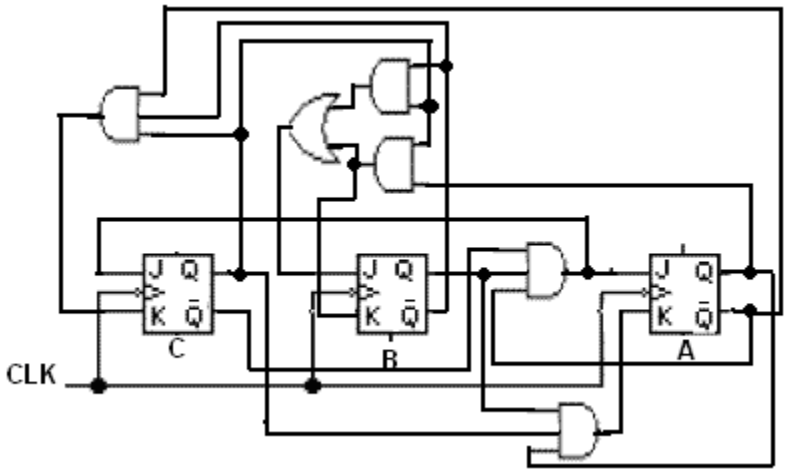


Fig. 2.1 Logic diagram of a counter

3. Design a counter with the following repeated binary sequence: 0, 4, 2, 1, 6. Use T flip-flops.

Solution:

Step 1: Since it is a 3-bit counter, the number of flip-flops required is three.
Step 2: Let the type of flip-flops be RS flip-flops.
Step 3: Let the three flip-flops be *A*, *B* and *C*.
Step 4: The state table is as shown in Table 3.1.

Table 3.1 State table

Present State	Next State
A B C	*A B C*
0 0 0	1 0 0
1 0 0	0 1 0
0 1 0	0 0 1
0 0 1	1 1 0
1 1 0	0 0 0

Step 5: The next step is to develop an excitation table from the state table, which is shown in Table 3.2.

Table 3.2 Excitation table

Output State Transitions		Flip-flop Inputs		
Present State	Next State			
A B C	*A B C*	TA	TB	TC
0 0 0	1 0 0	1	0	0
1 0 0	0 1 0	1	1	0
0 1 0	0 0 1	0	1	1
0 0 1	1 1 0	1	1	1
1 1 0	0 0 0	1	1	0

Step 6: Now transfer the T states of the flip-flop inputs from the excitation table to Karnaugh maps in Tables 3.3–3.5 to derive a simplified Boolean expression for each flip-flop input.

Table 3.3 K-map for TA

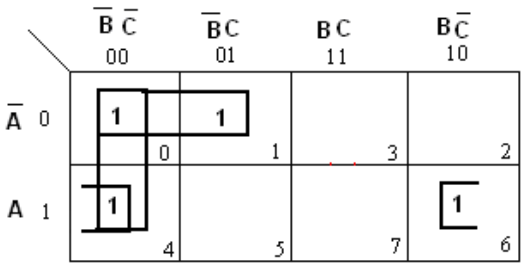


Table 3.4 K-map for TB

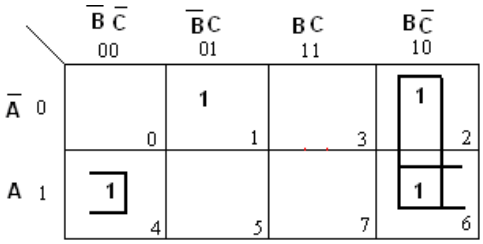
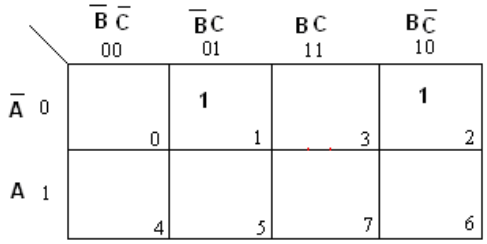


Table 3.5 K-map for TC



From the K-maps, the following expressions for the T input of each flip-flop are obtained:

$$TA = \overline{A}\overline{B} + \overline{B}\overline{C} + A\overline{C}$$

$$TB = \overline{A}\overline{B}C + A\overline{C} + B\overline{C}$$

$$TC = \overline{A}\overline{B}C + \overline{A}B\overline{C}$$

Step 7: The final step is to implement the combinational logic from the equations and connect the flip-flops to form the sequential circuit. The complete logic of a counter is shown in Fig 3.1.

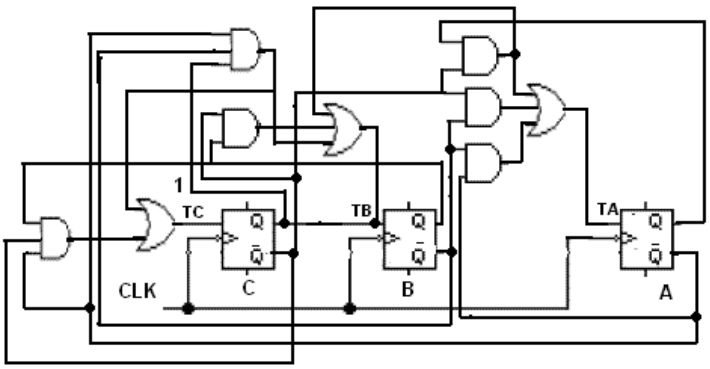


Fig. 3.1 Logic diagram of a counter

4. Design a sequential circuit whose state tables are specified in Table 18p.36, using *D* flip-flops.

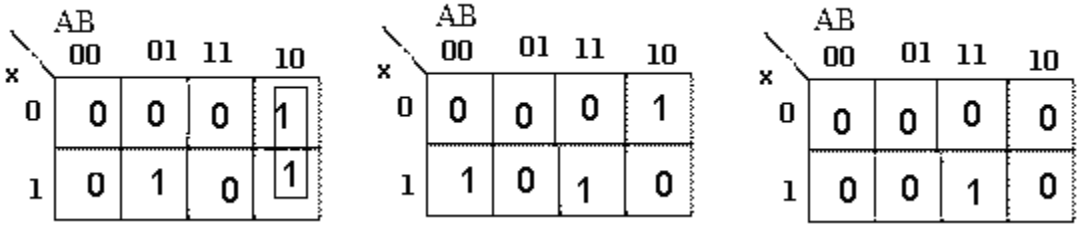
Solution:

First, we make the stable state and the next step is to derive the excitation table for the design circuit, which is shown in Table 4.1. The output of the circuit is labelled Z.

Table 4.1 Excitation table

Present State *A B*	Next State *A B*	Input *x*	Flip-flop Inputs DA DB	Output Z
0 0	0 0	0	0 0	0
0 0	0 1	1	0 1	0
0 1	0 0	0	0 0	0
0 1	1 0	1	1 0	0
1 0	1 1	0	1 1	0
1 0	1 0	1	1 0	0
1 1	0 0	0	0 0	0
1 1	0 1	1	0 1	1

Table 4.2 K-maps for DA, DB and Z



The simplified Boolean expressions are:

$$DA = A\overline{B} + \overline{A}Bx$$
$$DB = \overline{A}\overline{B}x + ABx + A\overline{B}\overline{x}$$
$$Z = ABx$$

Finally, the logic diagram is as shown in Fig.4.1.

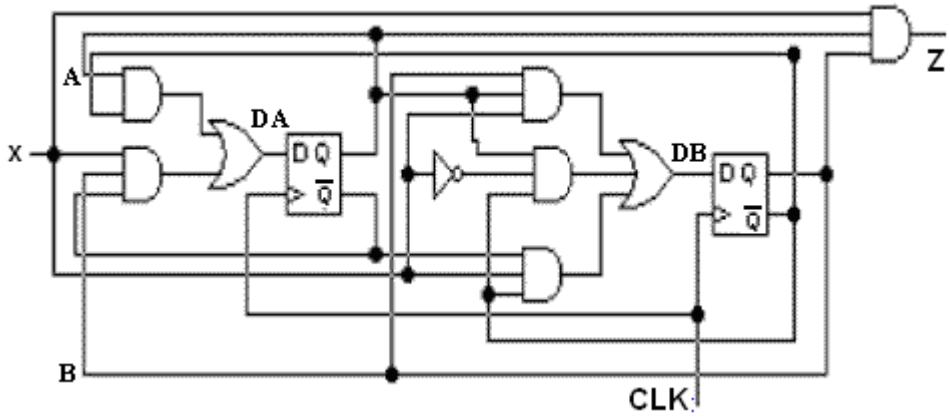


Fig. 4.1 Logic diagram