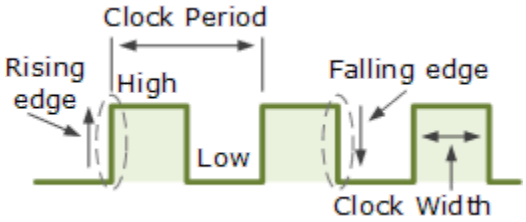


Multivibrators

Multivibrators are sequential logic circuits that operate continuously between two distinct states of HIGH and LOW

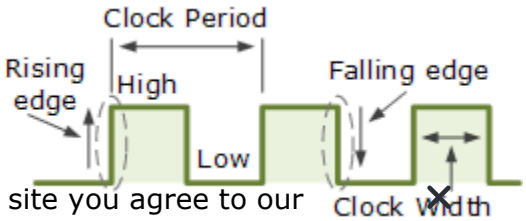
Individual **Sequential Logic** circuits can be used to build more complex circuits such as Multivibrators, Counters, Shift Registers, Latches and Memories.

But for these types of circuits to operate in a "sequential" way, they require the addition of a clock pulse or timing signal to cause them to change their state. Clock pulses are generally continuous square or rectangular shaped waveform that is produced by a single pulse generator circuit such as a **Multivibrator**.

A *multivibrator* circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. Astable multivibrators generally have an even 50% duty cycle, that is that 50% of the cycle time the output is "HIGH" and the remaining 50% of the cycle time the output is "OFF". In other words, the duty cycle for an astable timing pulse is 1:1.

Sequential logic circuits that use the clock signal for synchronization are dependent upon the frequency and and clock pulse width to activate there switching action. Sequential circuits may also change their state on either the rising or falling edge, or both of the actual clock signal as we have seen previously with the basic flip-flop circuits. The following list are terms associated with a timing pulse or waveform.

- Active HIGH – if the state change occurs from a "LOW" to a "HIGH" at the clock's pulse rising edge or during the clock width.



- Active LOW – if the state change occurs from a "HIGH" to a "LOW" at the clock's pulses falling edge.
- Duty Cycle – this is the ratio of the clock width to the clock period.
- Clock Width – this is the time during which the value of the clock signal is equal to a logic "1", or HIGH.
- Clock Period – this is the time between successive transitions in the same direction, ie, between two rising or two falling edges.
- Clock Frequency – the clock frequency is the reciprocal of the clock period, frequency = 1/clock period. ($f = 1/T$)

Clock Signal Waveform

Clock pulse generation circuits can be a combination of analogue and digital circuits that produce a continuous series of pulses (these are called astable multivibrators) or a pulse of a specific duration (these are called monostable multivibrators). Combining two or more of multivibrators provides generation of a desired pattern of pulses (including pulse width, time between pulses and frequency of pulses).

There are basically three types of clock pulse generation circuits:

Astable – A *free-running multivibrator* that has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.

Monostable – A *one-shot multivibrator* that has only **ONE** stable state and is triggered externally with it returning back to its first stable state.

Bistable – A *flip-flop* that has **TWO** stable states that produces a single pulse either positive or negative in value.

One way of producing a very simple clock signal is by the interconnection of logic gates. As NAND gates contains amplification, they can also be used to provide a clock signal or timing pulse with the aid of a single Capacitor and a single Resistor to provide the feedback and timing function.

These timing circuits are often used because of there simplicity and are also useful if a logic circuit is designed that has unused gates which can be utilised to create the monostable or astable oscillator. This simple type of RC Oscillator network is sometimes called a "Relaxation Oscillator".

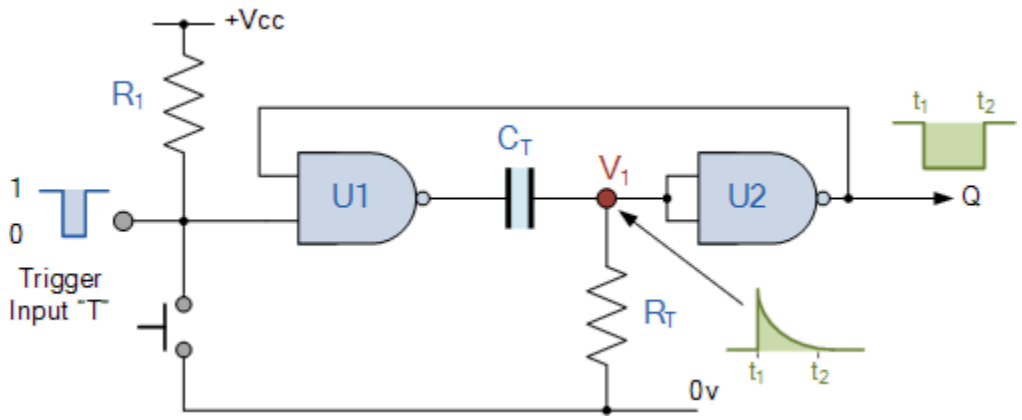
Monostable Multivibrator Circuits

Monostable Multivibrators or "one-shot" pulse generators are generally used to convert short sharp pulses into wider ones for timing applications. Monostable multivibrators generate a single output pulse, either "HIGH" or "LOW", when a suitable external trigger signal or pulse T is applied.

This trigger pulse signal initiates a timing cycle which causes the output of the monostable to change state at the start of the timing cycle, (t_1) and remain in this second state until the end of the timing period, (t_2) which is determined by the time constant of the timing capacitor, C_T and the resistor, R_T.

The monostable multivibrator now stays in this second timing state until the end of the RC time constant and automatically resets or returns itself back to its original (stable) state. Then, a monostable circuit has only one stable state. A more common name for this type of circuit is simply a "Flip-Flop" as it can be made from two cross-coupled NAND gates (or NOR gates) as we have seen previously. Consider the circuit below.

Simple NAND Gate Monostable Circuit



Suppose that initially the trigger input T is held HIGH at logic level "1" by the resistor R_1 so that the output from the first NAND gate U1 is LOW at logic level "0", (NAND gate principals). The timing resistor, R_T is connected to a voltage level equal to logic level "0", which will cause the capacitor, C_T to be discharged. The output of U1 is LOW, timing capacitor C_T is completely discharged therefore junction V1 is also equal to "0" resulting in the output from the second NAND gate U2, which is connected as an inverting NOT gate will therefore be HIGH.

The output from the second NAND gate, (U2) is fed back to one input of U1 to provide the necessary positive feedback. Since the junction V1 and the output of U1 are both at logic "0" no current flows in the capacitor C_T. This results in the circuit being **Stable** and it will remain in this state until the trigger input T changes.

If a negative pulse is now applied either externally or by the action of the push-button to the trigger input of the NAND gate U1, the output of U1 will go HIGH to logic "1" (NAND gate principles).

Since the voltage across the capacitor cannot change instantaneously (capacitor charging principals) this will cause the junction at V1 and also the input to U2 to also go HIGH, which in turn will make the output of the NAND gate U2 change LOW to logic "0" The circuit will now remain in this second state even if the trigger input pulse T is removed. This is known as the **Meta-stable** state.

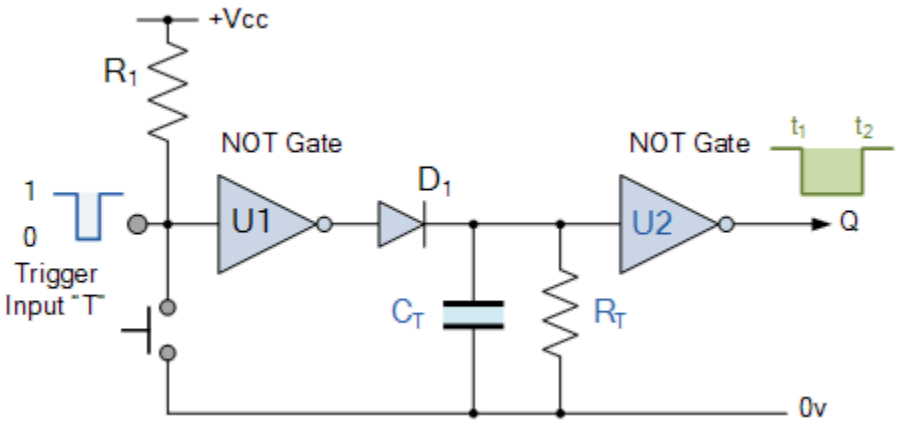
The voltage across the capacitor will now increase as the capacitor C_T starts to charge up from the output of U1 at a time constant determined by the resistor/capacitor combination. This charging process continues until the charging current is unable to hold the input of U2 and therefore junction V1 HIGH.

When this happens, the output of U2 switches HIGH again, logic "1", which in turn causes the output of U1 to go LOW and the capacitor discharges into the output of U1 under the influence of resistor R_T. The circuit has now switched back to its original stable state.

Thus for each negative going trigger pulse, the monostable multivibrator circuit produces a LOW going output pulse. The length of the output time period is determined by the capacitor/resistor combination (**RC Network**) and is given as the **Time Constant** T = 0.69RC of the circuit in seconds. Since the input impedance of the NAND gates is very high, large timing periods can be achieved.

As well as the NAND gate monostable type circuit above, it is also possible to build simple monostable timing circuits that start their timing sequence from the rising-edge of the trigger pulse using NOT gates, NAND gates and NOR gates connected as inverters as shown below.

NOT Gate Monostable Multivibrator



As with the NAND gate circuit above, initially the trigger input T is HIGH at a logic level "1" so that the output from the first NOT gate U1 is LOW at logic level "0". The timing resistor, R_T and the capacitor, C_T are connected together in parallel and also to the input of the second NOT gate U2. As the input to U2 is LOW at logic "0" its output at Q is HIGH at logic "1".

When a logic level "0" pulse is applied to the trigger input T of the first NOT gate it changes state and produces a logic level "1" output. The diode D1 passes this logic "1" voltage level to the RC timing network. The voltage across the capacitor, C_T increases rapidly to this new voltage level, which is also connected to the input of the second NOT gate. This in turn outputs a logic "0" at Q and the circuit stays in this **Meta-stable** state as long as the trigger input T applied to the circuit remains LOW.

When the trigger signal returns HIGH, the output from the first NOT gate goes LOW to logic "0" (NOT gate principals) and the fully charged capacitor, C_T starts to discharge itself through the parallel resistor, R_T connected across it. When the voltage across the capacitor drops below the lower threshold value of the input

to the second NOT gate, its output switches back again producing a logic level "1" at Q. The diode D1 prevents the timing capacitor from discharging itself back through the first NOT gates output.

Then, the **Time Constant** for a NOT gate **Monostable Multivibrator** is given as T = 0.8RC + Trigger in seconds.

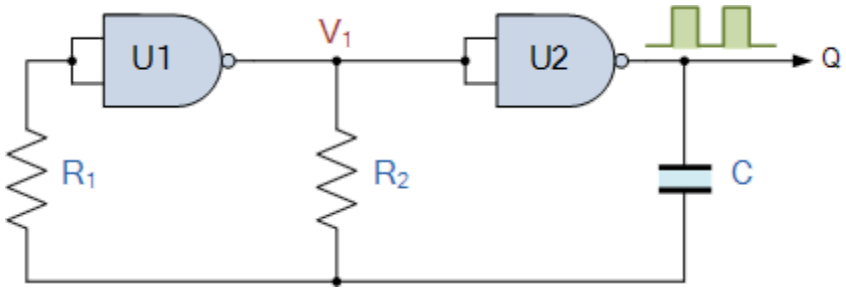
One main disadvantage of **Monostable Multivibrators** is that the time between the application of the next trigger pulse T has to be greater than the RC time constant of the circuit.

Astable Multivibrator Circuits

Astable Multivibrators are the most commonly used type of multivibrator circuit. An astable multivibrator is a free running oscillator that have no permanent "meta" or "steady" state but are continually changing there output from one state (LOW) to the other state (HIGH) and then back again. This continual switching action from "HIGH" to "LOW" and "LOW" to "HIGH" produces a continuous and stable square wave output that switches abruptly between the two logic levels making it ideal for timing and clock pulse applications.

As with the previous monostable multivibrator circuit above, the timing cycle is determined by the RC time constant of the resistor-capacitor, RC Network. Then the output frequency can be varied by changing the value(s) of the resistors and capacitor in the circuit.

NAND Gate Astable Multivibrator



The **astable multivibrator** circuit uses two CMOS NOT gates such as the CD4069 or the 74HC04 hex inverter ICs, or as in our simple circuit below a pair of CMOS NAND such as the CD4011 or the 74LS132 and an RC timing network. The two NAND gates are connected as inverting NOT gates.

Suppose that initially the output from the NAND gate U2 is HIGH at logic level "1", then the input must therefore be LOW at logic level "0" (NAND gate principles) as will be the output from the first NAND gate U1. Capacitor, C is connected between the output of the second NAND gate U2 and its input via the timing resistor, R_2. The capacitor now charges up at a rate determined by the time constant of R_2 and C.

As the capacitor, C charges up, the junction between the resistor R_2 and the capacitor, C, which is also connected to the input of the NAND gate U1 via the stabilizing resistor, R_2 decreases until the lower threshold value of U1 is reached at which point U1 changes state and the output of U1 now becomes HIGH. This causes

NAND gate U2 to also change state as its input has now changed from logic "0" to logic "1" resulting in the output of NAND gate U2 becoming LOW, logic level "0".

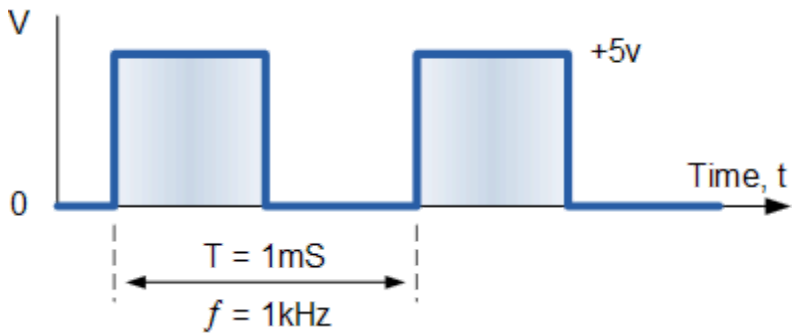
Capacitor C is now reverse biased and discharges itself through the input of NAND gate U1. Capacitor, C charges up again in the opposite direction determined by the time constant of both R_2 and C as before until it reaches the upper threshold value of NAND gate U1. This causes U1 to change state and the cycle repeats itself over again.

Then, the time constant for a NAND gate **Astable Multivibrator** is given as T = 2.2RC in seconds with the output frequency given as f = 1/T.

For example: if the resistor R_2 = 10kΩ and the capacitor C = 45nF, the oscillation frequency of the circuit would be given as:

$$f = \frac{1}{T} = \frac{1}{2.2RC} = \frac{1}{2.2 \times 10k\Omega \times 45nF} = 1kHz$$

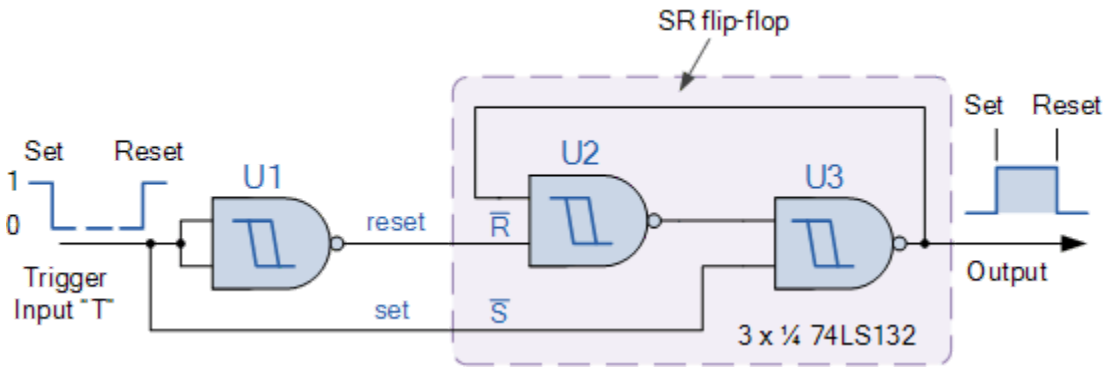
Then the output frequency is calculated as being 1kHz, which equates to a time constant of 1mS so the output waveform would look like:



Bistable Multivibrator Circuits

The **Bistable Multivibrators** circuit is basically a SR flip-flop that we look at in the previous tutorials with the addition of an inverter or NOT gate to provide the necessary switching function. As with flip-flops, both states of a bistable multivibrator are stable, and the circuit will remain in either state indefinitely. This type of multivibrator circuit passes from one state to the other "only" when a suitable external trigger pulse T is applied and to go through a full "SET-RESET" cycle **two** triggering pulses are required. This type of circuit is also known as a "**Bistable Latch**", "**Toggle Latch**" or simply "**T-latch**".

NAND Gate Bistable Multivibrator



The simplest way to make a **Bistable Latch** is to connect together a pair of Schmitt NAND gates to form a SR latch as shown above. The two NAND gates, U2 and U3 form the bistable which is triggered by the input NAND gate, U1. This U1 NAND gate can be omitted and replaced by a single toggle switch to make a switch debounce circuit as seen previously in the SR Flip-flop tutorial.

When the input pulse goes "LOW" the bistable latches into its "SET" state, with its output at logic level "1", until the input goes "HIGH" causing the bistable to latch into its "RESET" state, with its output at logic level "0". The output of a bistable multivibrator will stay in this "RESET" state until another input pulse is applied and the whole sequence will start again.

Then a **Bistable Latch** or "Toggle Latch" is a two-state device in which both states either positive or negative, (logic "1" or logic "0") are stable.

Bistable Multivibrators have many applications such as frequency dividers, counters or as a storage device in computer memories but they are best used in circuits such as *Latches* and *Counters*.

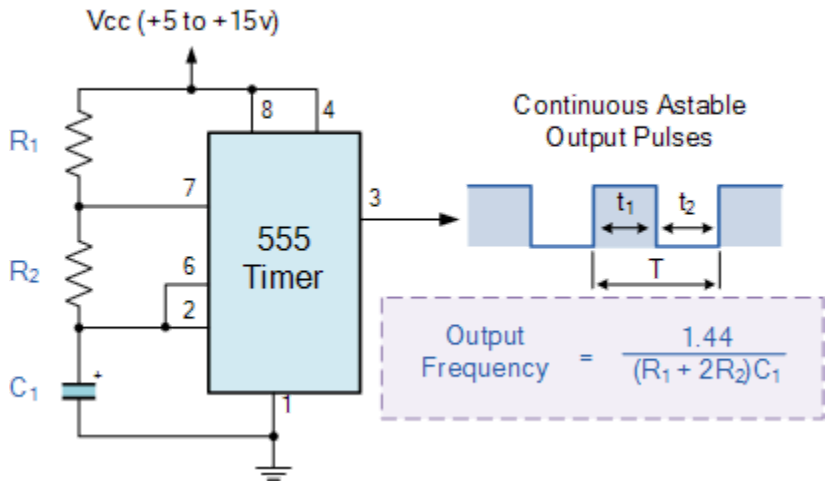
555 Timer Circuit.

Simple Monostable or Astable multivibrators can now be easily made using standard commonly available waveform generator IC's specially design to create timing and oscillator circuits. Relaxation oscillators can be constructed simply by connecting a few passive components to their input pins with the most commonly used waveform generator type IC being the classic 555 timer.

The **555 Timer** is a very versatile low cost timing IC that can produce a very accurate timing periods with good stability of around 1% and which has a variable timing period from between a few micro-seconds to many hours with the timing period being controlled by a single RC network connected to a single positive supply of between 4.5 and 16 volts.

The NE555 timer and its successors, ICM7555, CMOS LM1455, DUAL NE556 etc, are covered in the **555 Oscillator** tutorial and other good electronics based websites, so are only included here for reference purposes as a clock pulse generator. The 555 connected as an Astable Multivibrator is shown below.

NE555 Astable Multivibrator.



Here the 555 timer is connected as a basic Astable Multivibrator producing a continuous output waveform. Pins 2 and 6 are connected together so that it will re-trigger itself on each timing cycle, thereby functioning as an Astable oscillator. Capacitor, C1 charges up through resistor, R1 and resistor, R2 but discharges only through resistor, R2 as the other side of R2 is connected to the discharge terminal, pin 7. Then the timing period of t_1 and t_2 is given as:

$$t_1 = 0.693\,(R_1 + R_2)\,C_1$$

$$t_2 = 0.693\,(R_2)\,C_1$$

$$T = t_1 + t_2 = 0.693\,(R_1 + 2R_2)\,C_1$$

The voltage across the capacitor, C1 ranges from between 1/3 Vcc to approximately 2/3 Vcc depending upon the RC timing period. This type of circuit is very stable as it operates from a single supply rail resulting in an oscillation frequency which is independent of the supply voltage Vcc.

In the next tutorial about **Sequential Logic Circuits**, we will look another type of clock controlled flop-flop called a Data Latch. Data latches are very useful sequential circuits which can be made from any standard gated SR flip-flop and used for frequency division to produce various ripple counters, frequency dividers and latches.

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