Code No: RT21053 **R13** SET - 1

II B. Tech I Semester Regular Examinations, Jan - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What are the characteristics of 2's complement numbers?
   b) State the purpose of reducing the switching functions to minimal form.
   c) Define half adder.
   d) What are the basic operations in Boolean algebra?
   e) How do you convert one type of flip-flop into another?
   f) What are shift registers?
   g) What is the basic architecture of a PLA?
   h) Compare a decoder with a Demultiplexer. (3M+3M+2M+3M+3M+2M+3M+3M)

PART-B

2. a) The solution to the quadratic equation $x^2 - 11x + 22 = 0$ is x = 3 and x = 6. What is the base of numbers.
   b) Using 10's complement, subtract
   i) 72532_{10}-3250_{10} ii) 3250_{10}-72532_{10}. What do you infer from the results. (8M+8M)

3. Using K-map method determine the prime implicant and obtain the possible minimal expression for the following function
   F(A,B,C,D) = Σm(8,12,13) + d(1,2,4,6,7,11) (16M)

4. a) Implement the following switching function using a Four input multiplexer
   F(A, B, C, D) = Σm (0, 1, 2, 4, 6, 9, 10, 13, 14)
   b) A Combinational circuit is defined by the following three Boolean functions
   $F_1 = x'y'z' + xz$ $F_2 = xy'z' + x'y$ $F_3 = x'y'z + xy$
   Design the circuit with a decoder and external gates. (8M+8M)

5. a) Define the following terms related to flip-flops.
   i) set-up time ii) hold time iii) propagation delay iv) preset and v) clear.
   b) Discuss D-type edge- triggered flip-flop in detail? (9M+7M)

6. Design a resister to perform left shift and right shift for the following data 10110101 ? (16M)

7. a) Implement the following Boolean function using PAL
   i) $F_1(x, y, z) = \sum m(0, 1, 3, 6, 7)$ ii) $F_2(x, y, z) = \sum m(0, 2, 3, 5)$
   b) Compare PLA with PROM? (8M+8M)
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Code No: RT21053 **R13** SET - 2

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) How are negative numbers represented?
   b) What is a cell of a K-map?
   c) Define full Subtractor.
   d) Write the Boolean algebraic laws.
   e) What is meant by race around condition in flip-flops?
   f) What is the basic difference between a shift register and a counter?
   g) Give the comparison between PROM, PLA, and PAL.
   h) What is a standard SOP form? (2M+3M+2M+3M+3M+2M+3M+3M)

PART-B

2. a) What is the advantage of 1's and 2's complement in computers. Represent +45 and -45 in sign-magnitude, sign-1's complement and sign-2's complement representation.
   b) Explain about Weighted and non-weighted codes (8M+8M)

3. a) Prove that AND - OR network is equivalent to NAND-NAND network
   b) Define the following terms with respect to K-Map with an example.
   i) Prime implicant ii) Redundant terms
   iii) Essential Prime implicant iv) Octet (8M+8M)

4. a) Implement a full adder with two 4×1 multiplexers.
   b) Implement Half adder using 5 NAND gates (8M+8M)

5. a) Convert a T flip flop to D type flip flop.
   b) Explain the working of a master-slave JK flip flop. State its advantages. (8M+8M)

6. a) Draw and explain 4-bit universal shift register.
   b) Explain different types of shift registers. (8M+8M)

7. List the PLA programming table and draw the PLA structure for the BCD-to-Excess-3-code converter. (16M)

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Time: 3 hours Max. Marks: 70

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2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What do you mean by end around carry? When does it come into picture?
   b) What is the importance of Universal Gates?
   c) Define Encoder.
   d) What is a prime implicant in K-map?
   e) Distinguish between synchronous and asynchronous latches?
   f) What are the applications of shift registers?
   g) Is it possible to share the product terms between different outputs in a PLA? If yes, how?
   h) What is the advantage of SOP and POS forms of realization?

(2M+3M+2M+3M+3M+2M+3M+3M)

PART-B

2. a) The binary numbers listed have a sign bit in the left most position and, if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers.
   i) 101011 + 111000 ii) 001110 + 110010 iii) 111001 – 001010 iv) 101011 – 100110
   b) Explain about Weighted and non-weighted codes (8M+8M)

3. List out the Basic Theorems and Properties of Boolean Algebra. Justify with Proof. (16M)

4. a) Implement the following functions on decoder logic
   $Y_1 = \Sigma(0,1,3,6,7)$, $Y_2 = \Pi(0,2,4,7)$, $Y_3 = \Pi(1,3,6,7)$
   b) Realize a full sub tractor using MUX. (8M+8M)
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5. a) Determine how the circuit shown in Fig. 1 functions as a T-type flip-flop. What problem would there be when T= 1 and how could it be resolved.

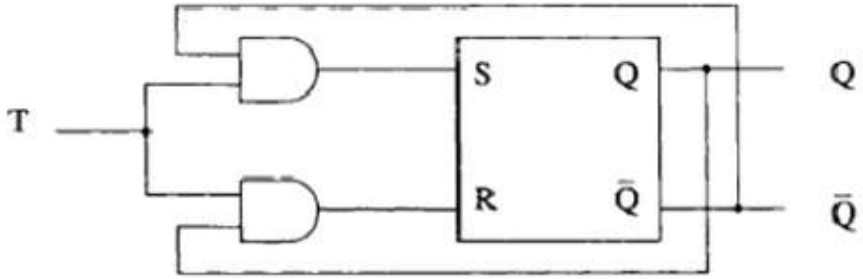

Figure 1

b) Convert a SR flip-flop to D type flip flop? (8M+8M)

6. a) Draw the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops.

b) Explain different types of shift registers. (8M+8M)

7. a) Draw and explain the block diagram of PLA.

b) Tabulate the PLA programmable table for the four Boolean functions given below:

$F_1(x,y,z) = \Sigma m\ (1,2,4,6)$

$F_2(x,y,z) = \Sigma m\ (0,1,6,7)$

$F_3(x,y,z) = \Sigma m\ (2,6)$

$F_4(x,y,z) = \Sigma m\ (1,2,3,5,7)$. (8M+8M)

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PART-A

1. a) Why is the binary number system used in digital systems?
b) State the Duality principle with example.
c) Define Demultiplexer.
d) What are the limitations of K-maps?
e) What are the various methods used for triggering flip-flops?
f) What are the advantages and disadvantages of ripple counters?
g) How is the capacity of a PLA specified?
h) How do you convert a decimal number into a number in any other system with base b?
(2M+3M+3M+3M+3M+2M+3M+3M)

PART-B

2. a) Explain how 1's complement and 2's complement of a binary number is obtained? Illustrate by an example.
b) What is gray code? What are the rules to construct gray code? Develop the 4 bit gray code for the decimal 0 to 15. (8M+8M)

3. a) List the universal gates? Implement XOR & XNOR gates using universal gates?
b) Implement the following functions in canonical Sop and Pos forms
i) $f(A, B, C, D) = A'B + BC + CD' + ACD$
ii) $f(A, B, C, D) = (A + B' + C)(A + D)(B' + C')(A + B + C)$ (8M+8M)

4. a) Design an octal to binary encoder.
b) Design a full subtractor and implement it using NAND gates. Explain its operation with the help of truth table? (8M+8M)

5. a) Distinguish between combinational logic and sequential logic.
b) How could:
i) a JK flip-flop be used as a D-type? ii) a JK flip-flop be used as a T-type?
iii) a D-type flip-flop be used as a T-type? (8M+8M)

6. a) Explain synchronous ripple counters. Compare their merits and demerits.
b) Design a modulo -12 up synchronous counter using T- flip flops and draw circuit diagram.
(8M+8M)

7. a) Realize the following Boolean function using PROM $f(x, y, z, w) = \Sigma m$ (0, 1, 3, 6, 8, 9, 15).
b) Implement the following Boolean function using PLA
i) $F_1(x,y,z) = \Sigma m$ (0, 1, 2, 6, 7), $F_2(x,y,z) = \Sigma m$ (0, 2, 3, 5) (8M+8M)
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