Code No: RT21053 **R13** SET - 1

II B. Tech I Semester Supplementary Examinations, June - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	Convert the decimal number 46 to binary number system also explain the steps of conversion	4M
	b)	Realize Ex-OR gate operation with minimal number of NAND gates	4M
	c)	Compare serial adder and parallel adder	4M
	d)	List the basic flip flop applications	3M
	e)	Explain the concept of bidirectional shift register	4M
	f)	What is programmable logic array? How it differs from ROM?	3M

PART –B

2	a)	Perform the following arithmetic operation using l's complement method : i) Add $(-19)_{10}$ and $(29)_{10}$ ii) Add $(21)_{10}$ and $(37)_{10}$	8M
	b)	The Hamming code 010110110 is received at the receiving end. Correct the received data if there is any error.	8M
3		Using Quine-Mc Cluskey method,obtain minimal expression for the following Boolean function $F(A,B,C,D,E) = \sum m(8,12,13,18,19,21,22,24,25,28,30,31) + \sum \varphi(2,6,9,20,26,29)$	16M
4	a)	Implement the following using a multiplexer $F(w,x,y,z) = \sum m(0,1,2,3,4,9,13,14,15)$	8M
	b)	Draw the logic diagram of 8:1 MUX with active low enable input using NAND gates	8M
5	a)	Draw the circuit diagram of J-K flip flop with NAND gates with positive edge triggering and explain its operation with the help of a truth table.	10M
	b)	What is race around condition and how is it eliminated.	6M
6	a)	What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?	8M
	b)	Draw the logic diagram of a MOD-10 count up ripple counter using count reset and explain its operation.	8M
7	a)	Draw the internal logic construction of 32X4 ROM and explain how an Boolean expression is implemented using it.	8M
	b)	Implement the following Boolean expressions using ROM $F_1(A,B,C) = \sum m(0,2,4,7)$ $F_2(A,B,C) = \sum m(1,3,5,7)$	8M

|''|'''||''||'''||||
~~~~~~

Code No: RT21053 **R13** SET - 2

II B. Tech I Semester Supplementary Examinations, June - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	$(25.75)_{10}$ to binary number	4M
	b)	Find the compliment of the following expression (AB’ + C) D’ + E	4M
	c)	Implement 1:8 demultiplexer using two 1:4 demultiplexer	4M
	d)	Compare combinational circuits and sequential circuits	4M
	e)	Write the applications of shift register	3M
	f)	What are the programmable logic devices	3M

PART –B

2	a)	Perform the following using BCD arithmetic. i)$1263_{10} + 9687_{10}$ ii)$7672_{10} + 3378_{10}$	8M
	b)	Perform the following subtraction: i) $(11010)_2 – (10000)_2$ using 1’s complement ii) $(1000100)_2$ - $(1010100)_2$ using 2’s complement	8M
3	a)	Using K-map determine SOP realization of the following $F(w,x,y,z) = \sum m(1,4,8,9,13,14,15) + \sum \varphi(2,3,11,12)$.	8M
	b)	Realize a two level NAND-NAND circuit for the following F=(w.x.y) +(y.z)	8M
4	a)	Implement the following using 4 to 16 line decoder $F(A,B,C,D) = \sum(0,1,4,7,9,12,14)$	8M
	b)	Design 4X1 MUX using 2X4 decoder and basic logic gates	8M
5	a)	Define the following terms of a flip flop.(i) Hold time (ii) Set up time (iii) Propagation delay time.	6M
	b)	Draw the circuit diagram of master-slave J-K flip flop and explain its operation with the help of a truth table. How is it different from edge trigged flip flop? Explain.	10M
6	a)	Draw the logic diagram of a four bit binary ripple counter and explain its operation.	8M
	b)	Explain the working of serial in parallel out shift register with logic diagram and waveforms.	8M
7	a)	Draw and explain the block diagram of PLA	8M
	b)	Implement following Boolean functions using PLA $F_1 (A,B,C) = \sum m(0,1,3,5)$ and $F_2 (A,B,C) = \sum m(0,3,5,7)$	8M

|''|'''||''||'''||||
~~~~~~

Code No: RT21053 **R13** SET - 3

II B. Tech I Semester Supplementary Examinations, June - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	Decimal number 86 to octal number system also explain the steps of conversion	(4M)
	b)	State and prove consensus theorem	(3M)
	c)	Realize f(x,y,z) = ∑ (0,1,5,7) using AND , OR and inverter gates	(4M)
	d)	Explain the difference between racing and toggling	(4M)
	e)	What is the difference between synchronous and asynchronous counter	(3M)
	f)	List the applications of PLA	(4M)

PART –B

2	a)	Briefly explain error detecting and error correcting codes with examples.	(8M)
	b)	Convert the following to Decimal and then to Hexadecimal. i) 1267_8 ii) 11011101_2 iii) 786_{10}	(8M)
3	a)	Find the prime implicants, essential prime implicants and number of minimal expressions for the given function using K -map f(A,B,C,D) = ∑m(1,3,5,7,8,10,12,13)	(8M)
	b)	Realize a two level OR-AND circuit for the following F = (x+y').z + (x'.y.z')	(8M)
4	a)	Design and realize the combinational logic circuit for converting a BCD number to a seven segment display	(10M)
	b)	Design a full adder with two half adders and other logic gates and explain its operation.	(6M)
5	a)	Compare latch and flip flop	(6M)
	b)	Realize D-latch using S-R latch. How is it different from D-flip flop? Draw the circuit using NAND gates and explain.	(10M)
6	a)	Explain the operation of universal shift register with suitable examples.	(8M)
	b)	Explain operation of Johnson counter with a diagram	(8M)
7	a)	Give the comparison between PROM, PLA and PAL	(6M)
	b)	Realize the BCD to EXCESS-3 code converter using PLA	(10M)
~~~~~~

Code No: RT21053 **R13** SET - 4

II B. Tech I Semester Supplementary Examinations, June - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1	a)	Convert 6ABC.2A to decimal number system	4M
	b)	Convert the following expression to POS from (A+B+C) (AB+AC)	3M
	c)	Realize the functionality of NAND gate using 2X1 multiplexer	4M
	d)	Explain the difference between edge triggering and level triggering	4M
	e)	Define counter? Write the classification of counter	4M
	f)	What are the advantages of PLD	3M

PART –B

2	a)	Using 2's complement perform the following: i) $(42)_{10}$ - $(68)_{10}$ ii) $(78)_{16}$ – $(56)_{16}$	8M
	b)	Perform each of the following decimal subtraction in excess-3 code i) 29 – 14 ii) 205 – 196 iii) 471 – 352	8M
3	a)	Using Boolean algebra rules simplify the following Boolean expression and implement in NAND logic f(A,B,C,D) = ∑m(10,11,14,15)	8M
	b)	Find the minimal expression using K- map for given function F F(w,x,y,z) = $\sum(0,2,3,5,7,9)+\sum_d(1,6,10,11)$	8M
4	a)	Construct a 4X16 decoder using 2X4 decoder. Show the schematic diagram neatly.	8M
	b)	Realize full adder circuit using multiplexer.	8M
5	a)	Draw the truth table, logic diagrams of J-K, R-S, D and T type flip flops	10M
	b)	Convert a T flip flop to D flip flop and write characteristic equations of T and D flip flops.	6M
6	a)	What is the procedure for designing a synchronous counter?	8M
	b)	The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?	8M
7	a)	Draw the internal construction of PLA having three inputs, three product terms and two outputs	8M
	b)	Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the number of product terms i) A(x,y,z) = ∑ (1,2,4,6) ii) B(x,y,z) = ∑ (0,1,6,7) iii) C(x,y,z) = ∑ (2,6) iv) D(x,y,z) = ∑ (1,2,3,5,7)	8M

|''|'''||''||'''||||
~~~~~~