Code No: RT21053 **R13** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2016
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Convert the following numbers with the given radix to decimal. (4M)
   i) $(4433)_5$ ii) $(1199)_{12}$
   b) State and prove De Morgan's theorem. (4M)
   c) Define encoder? List out the applications of it? (3M)
   d) Explain the operation of a SR flip-flop? (3M)
   e) Discuss about a serial-in, serial-out shift registers? (4M)
   f) What are the advantages of PLDs over fixed function ICs? (4M)

PART –B

2. a) Perform the subtraction using 1's complement and 2's complement methods. (8M)
   i) 11010 – 10000 ii) 11010 – 1101 iii) 100 - 110000
   b) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation. (8M)

3. a) Reduce using mapping the following expression and implement the real minimal expression in Universal logic. F= ∑m (0, 2, 4, 6, 7, 8, 10, 12, 13, 15) (8M)
   b) State and prove consensus theorem? Solve the given expression using consensus theorem. (i) $\overline{AB} + AC + \overline{BC} + \overline{BC} + AB$ (ii) $(A+B)(\overline{A}+C)(B+C)(\overline{A}+D)(B+D)$ (8M)

4. a) Perform the realization of half adder and full adder using decoders and logic gates. (8M)
   b) Design a 4 bit combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR Gates. (8M)

5. a) Draw the circuit diagram of a positive edge triggered JK flip flop and explain its operation with the help of a truth table? (8M)
   b) Convert a D flip flop into SR flip flop and JK flip flop? (8M)

6. a) Design a 4-bit universal shift register using D flip flops and multiplexers? (8M)
   b) Explain the operation of 4-bit ring counter with circuit diagram, state transition diagram and state table. Draw the corresponding timing diagrams? (8M)

7. a) Discuss how PROM, EPROM and EEPROM technologies differ from each other. (8M)
   b) Implement the following multiple output functions using PROM (8M)
   F_1= ∑m (0, 1, 4, 7, 12, 14, 15) F_3= ∑m (2, 3, 7, 8, 10)
   F_2= ∑m (1, 3, 6, 9, 12) F_4= ∑m (1, 3, 5)

*****

|''|'''||''||'''||||
~~~~~~

Code No: RT21053 **R13** SET - 2

II B. Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2016
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Why is hexadecimal code widely used in digital systems? List out the digits used to represent the hexadecimal codes? (4M)
   b) What is two-level logic? What is its advantage? (4M)
   c) Why a multiplexer is called a data selector? Draw the 2x1 MUX. (4M)
   d) What are the various methods used for triggering flip-flops? Explain with examples. (3M)
   e) Explain the basic types of shift registers? (3M)
   f) Draw the basic architecture of a PAL? (4M)

PART –B

2. a) Subtract the following decimal numbers by the 9's and 10's complement methods. (8M)
   274 - 86 ii) 93 - 615 iii) 574.6 - 297.7 iv) 376.3 - 765.6
   b) What is a Gray code? Obtain a 3-bit and 4-bit gray code from a 2-bit gray code by reflection. (8M)

3. a) Without reducing, implement the following expressions in AOI logic and then convert them into NAND logic and NOR logic (8M)
   A + BC + (A + B'C) + D ii) A + B'C + (B + C)' + B'C'
   b) Reduce the following expression to the simplest possible POS and SOP forms. (8M)
   F= ∑m (6,8,13,18,19,25,27,29,31) + d (2,3,11,15,17,24,28)

4. a) Implement the following multiple output combinational logic circuit using a 4 line to 16 line decoder: (8M)
   F_1= ∑m (0, 1, 4, 7, 12, 14, 15) F_3= ∑m (2, 3, 7, 8, 10)
   F_2= ∑m (1, 3, 6, 9, 12) F_4= ∑m (1, 3, 5)
   b) Discuss a few applications of multiplexers and distinguish between a multiplexer and a decoder. (8M)

5. a) Draw the schematic circuit of an edge-triggered JK flip flop with active low preset and active low clear using NAND gates and explain its operation? (8M)
   b) Define the following terms with relation to flip flop: (8M)
   i) Set-up time ii) Hold time iii) Propagation delay time iv) Preset v) Clear

6. a) Design a type-D counter that goes through states 0, 2, 4, 6, 0…….. The undesired states must always go to a 0 on the next clock pulse. (8M)
   b) With suitable logic diagram explain a 4-bit bidirectional shift register? (8M)

7. a) What is a PLD? Compare the three combinational PLDs? (8M)
   b) Design an Excess-3 to BCD code converter using a PLA? (8M)

*****

|''|'''||''||'''||||
~~~~~~

Code No: RT21053 **R13** SET - 3

II B. Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2016
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) What are the three methods of obtaining the 2's complement of a given binary number? (4M)
   b) How can a NOR gate be used as an inverter, AND gate and OR gate? (4M)
   c) Distinguish between a half-adder and a full-adder? (3M)
   d) Draw the circuit of J – K master slave flip-flop with active high clear and active low preset. (3M)
   e) Draw the state diagram of modulo-4 up/down counter. (4M)
   f) What is a PLD? What is the principal advantage of a PLD? (4M)

PART -B

2. a) How are binary codes classified? Briefly explain each code with suitable examples? (8M)
   b) Convert the following numbers into Gray code numbers (8M)
   i) $(96)_{10}$ ii) $(45)_{16}$ iii) $(235)_{8}$ iv) $(85)_{12}$

3. a) Simplify the following using K- map and implement the same using NAND gates. (8M)
   $Y(A, B, C) = \sum (0, 2, 4, 5, 6, 7)$
   b) Simplify the following Boolean expression. (8M)
   $T(x, y, z) = (x + y)\{[x'(y' + z')]'\} + x'y' + x'z'$
   $X(A, B, C, D) = A^1B^1C^1 + (A+B+C^1)^1 + A^1B^1C^1D$

4. a) Draw the logic diagram of a 2 to 4 line decoder using NOR gates including an enable input. (8M)
   b) Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method. (8M)

5. a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation? (8M)
   b) Give the transition table for SR, JK, D and T flip flops. Convert an SR flip flop into D flip flop. (8M)

6. a) Write the design steps of synchronous counters with suitable examples? (8M)
   b) What is a register? Discuss the applications of shift registers? (8M)

7. a) Design an arithmetic circuit that adds 2 binary digits. The circuit should have 2 outputs, one for the sum and the other for the carry. Implement the same in a PAL. (8M)
   b) Show how the PLA circuit can be programmed to implement the binary to gray conversion. (8M)

*****

|''|'''||''||'''||||
~~~~~~

Code No: RT21053 **R13** SET - 4

II B. Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2016
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Express the Decimal Digits 0-9 in 2421 and 84-2-1. (4M)
   b) What do you mean by K-map? Name it advantages and disadvantages. (4M)
   c) Realize a single bit comparator? (3M)
   d) Draw and explain active low S-R latch. (3M)
   e) Draw the state diagram of synchronous mod-10 up-down counter. (4M)
   f) What are the advantages and disadvantages of using a PROM as a PLD? (4M)

PART -B

2. a) Convert the following to Decimal and then to octal (8M)
   (i) $(125F)_{16}$ (ii) $(10111111)_2$ (iii) $(392)_{10}$
   b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property? (8M)

3. a) Simplify the following using K- map and implement the same using NAND gates. (8M)
   Y (A, B, C) = ∑ (0, 2, 4, 5, 6, 7)
   b) Represent and draw the following Boolean function using minimum number of basic gates. i) (AB + AB') (AB)' (8M)
   ii) [(ABD(C + D + E)) + (A +DBC)'] (ABC + (CAD)')

4. a) Realize the function f(A,B,C,D) = ∑ (1,2,5,8,10,14)+d (6,7,15) using (8M)
   i) 8:1 MUX ii) 4:1 MUX
   b) Design and draw the logic circuit diagram for full adder/subtractor. Let us consider a control variable w and the designed circuit that functions as a full adder when w=0, as a full subtractor when w= 1. (8M)

5. a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation. Explain the Race around condition and also explain how to eliminate it. (8M)
   b) Draw the circuit diagram of clocked D-flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram. (8M)

6. a) Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table. (8M)
   b) With suitable logic diagrams explain about Buffer register and Controlled buffer register? (8M)

7. a) Design a PAL for the following logical functions. (8M)
   Y1=AB+A'CB', Y2=AB'C+AB+AC', Y3=AB+BC+CA
   b) Design a combinational circuit using ROM. The circuit accepts a 3 bit no and generates an O/p binary number equal to square of input number. (8M)

*****
~~~~~~