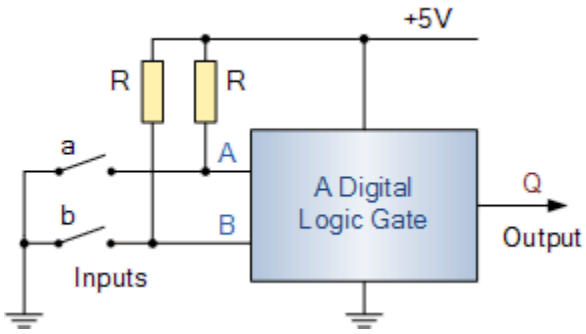


Pull-up Resistors

Pull-up and Pull-down resistors are used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition

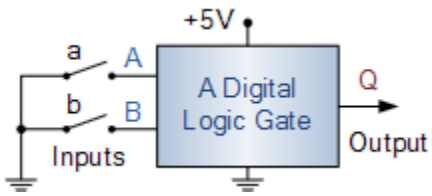
Digital logic gates can be used for connection to external circuits or devices but care must be taken to ensure that their inputs or outputs function correctly and provide the expected switching condition.

Modern digital logic gates, IC's and micro-controllers contain many inputs, called "pins" as well as one or more outputs, and these inputs and outputs need to be correctly set, either HIGH or LOW for the digital circuit to function correctly.

We know that logic gates are the most basic building block of any digital logic circuit and that by using combinations of the three basic gates, the AND gate, the OR gate and NOT gate, we can construct quite complex combinational circuits. But being digital, these circuits can only have one of two logic states, called the logic "0" state or the logic "1" state.

These logic states are represented by two different voltage levels with any voltage below one level regarded as a logic "0", and any voltage above another level regarded as logic "1". So for example, if the two voltage levels are 0V and +5V, then the 0V represents a logic "0" and the +5V represents a logic "1".

If the inputs to a digital logic gate or circuit are not within the range by which it can be sensed as either a logic "0" or a logic "1" input, then the digital circuit may false trigger as the gate or circuit does not recognise the correct input value, as the HIGH may not be high enough or the LOW may not be low enough.



For example, consider the digital circuit on the left. The two switches, “a” and “b”, represent the inputs to a generic logic gate. When switch “a” is closed (ON), input “A” is connected to ground, (0v) or logic level “0” (LOW) and likewise, when switch “b” is closed (ON), input “B” is also connected to ground, logic level “0” (LOW) and this is the correct condition we require.

However, when switch “a” is opened (OFF), what will be the value of the voltage applied to input “A”, HIGH or LOW? We assume it will be +5V (HIGH) as switch “a” is open-circuited and therefore input “A” is not shorted to ground, but this may not be the case. As the input is now effectively unconnected from either a defined HIGH or LOW condition, it has the potential to “float” about between 0V and +5V (Vcc) allowing the input to self–bias at any voltage level whether that represents a HIGH or a LOW condition.

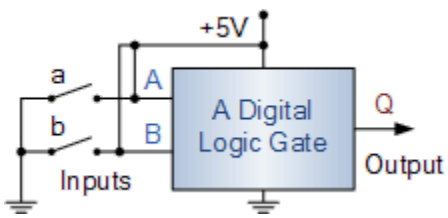
This uncertain situation may cause the digital input at “A” to stay at a logic level “0” (LOW) when the switch is open, when we actually need a logic “1”, (HIGH) causing the logic gate to falsely switch the output at “Q”. Also once there, this floating and weak input signal could easily change value at the slightest of interference or noise from its neighbouring inputs or could even cause it to go into oscillation, rendering the gate practically unusable. The same situation is also true with regards to the switching of input “B”.

Then to prevent accidental switching of digital circuits, any unconnected inputs called “floating inputs” should be tied to a logic “1” or logic “0” as appropriate for the circuit. We can easily do this by using what are commonly called **Pull-up Resistors** and **Pull-down Resistors** to give the input pin a defined default state, even if the switch is open, closed or there is nothing is connected to it.

When building digital electronic circuits, generally you will have some spare gates or latches within a single IC package left over, or the design of the circuit results in not all of a multi-input gates inputs being used. These unused logic inputs can be tied together or connected to a fixed voltage, using a high value resistor to either the Vcc voltage, known as pull-up or via a low value resistor to 0V (GND), known as pull-down. These unused inputs should never be left just floating about.

Pull-up Resistors

The most common method of ensuring that the inputs of digital logic gates and circuits can not self-bias and float about is to either connect the unused pins directly to ground (0V) for a constant low “0” input, (OR and NOR gates) or directly to Vcc (+5V) for a constant high “1” input (AND and NAND gates). Ok, lets look again at our two switched inputs from above.

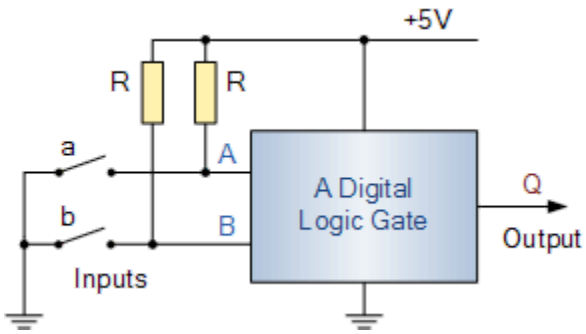


This time, to stop the two inputs, A and B, from “floating” about when the corresponding switches, “a” and “b” are open (OFF), the two inputs are connected to +5V supply.

You may think that this would work fine as when switch “a” is open (OFF), the input is connected to Vcc (+5V) and when the switch is closed (ON), the input is connected to ground as before, then inputs “A” or “B” always have a default state regardless of the position of the switch.

However, this is a bad condition because when either of the switches are closed (ON), there will be a direct short circuit between the +5V supply and ground, resulting in excessive current flow either blowing a fuse or damaging the circuit which is not good news. One way to overcome this issue is to use a pull-up resistor connected between the input pin and the +5V supply rail as shown.

Pull-up Resistor Application



By using these two pull-up resistors, one for each input, when switch "A" or "B" is open (OFF), the input is effectively connected to the +5V supply rail via the pull-up resistor. The result is that as there is very little input current into the input of the logic gate, very little voltage is dropped across the pull-up resistor so nearly all the +5V supply voltage is applied to the input pin creating a HIGH, logic "1" condition.

When switches "A", or "B" are closed, (OFF) the input is shorted to ground (LOW) creating a logic "0" condition as before at the input. However, this time we are not shorting out the supply rail as the pull-up resistor only passes a small current (as determined by Ohms law) through the closed switch to ground.

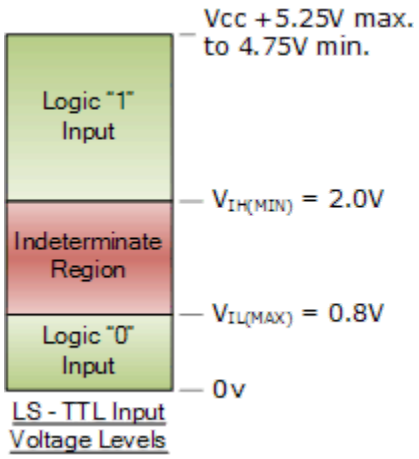
By using a *pull-up resistor* in this way, the input always has a default logic state, either "1" or "0", high or low, depending on the position of the switch, thus achieving the proper output function of the gate at "Q" and therefore preventing the input from floating about or self-biasing giving us exactly the switching condition we require.

While the connection between Vcc and an input (or output) is the preferred method for using a pull-up resistor, the question arises as how do we calculate the value of the resistance require to ensure the correct operation of the input.

Calculating Pull-up Resistor Value

All digital logic gates, circuits and micro-controllers are limited not only by their operating voltage, but in the current sinking and sourcing ability of each input pin. Digital logic circuits operate using two binary states which are normally represented by two distinct voltages: a high voltage V_H for logic "1" and low voltage V_L for logic "0". But within each of these two voltage states, there is a range of voltages which define the upper and lower voltages of these two binary states.

So for example, for the TTL 74LSxxx series of digital logic gates, the voltage ranges representing a logic level "1" and a logic level "0" are shown.



LS - TTL Input Voltage Levels

Where: $V_{IH(min)}$ = 2.0V is the minimum input voltage guaranteed to be recognized as a logic "1" (high) input and $V_{IL(max)}$ = 0.8V is the maximum input voltage guaranteed to be recognized as a logic "0" (low) input.

In other words, TTL 74LSxxx input signals between 0 and 0.8V are considered "LOW", and input signals between 2.0 and 5.0V are considered "HIGH". Any voltage inbetween 0.8 and 2.0 volts is not recognised as a logic "1" or logic "0".

When logic gates are connected together, the current flows between the output of one logic gate and the input of another. The amount of current required by a basic TTL logic gate input depends on whether the input is a logic "0" (LOW) or a logic "1" (HIGH) as this creates a current-sourcing action for a logic "0" and a current-sinking action for a logic "1".

When the input of the logic gate is HIGH, a current flows into the TTL input as the input acts basically as a path connected directly to ground. This input current, $I_{IH(max)}$ is positive in value as it flows "into" the gate and for most TTL 74LSxxx inputs have a value of 20μA.

Likewise, when the input of the logic gate is LOW, the current flows out of the TTL input as the input acts basically as a path connected directly to Vcc. This input current, $I_{IL(max)}$ is negative in value as it flows "out-of" the gate and for most TTL 74LSxxx inputs, has a value of -400μA, (-0.4mA).

Note that the values of HIGH and LOW voltages and currents differ between TTL logic families and is also much, much lower for CMOS logic families. Also the input voltage and current requirements for micro-controllers, PIC, Arduino, Raspberry Pie, etc will also be different so please consult their data sheets first.

By knowing the information above, we can calculate the maximum pull-up resistor value required for a single TTL 74LS series logic gate as:

Single Gate Pull-up Resistor Value

$$R_{MAX} = \frac{V_{CC} - V_{IH(MIN)}}{I_{IH}} = \frac{5 - 2}{20 \times 10^{-6}} = 150K\Omega$$

Then using Ohms Law, the maximum pull-up resistance required to drop 3 volts for a single TTL 74LS series logic gate would be 150kΩ. While this calculated value would work, it leaves no room for error as the voltage drop across the resistor is at its maximum while the input current is at its minimum.

Ideally we would want a logic "1" to be as close to Vcc as possible to guarantee 100% that the gate see's a HIGH (logic-1) input through the pull-up resistor. Reducing the resistive value of this pull-up resistor would give us a greater error margin should the tolerance of the resistor or the supply voltage not be as calculated. However, we do not want the resistor value to be too low as this would increases current flow into the gate increasing power dissipation.

So if we assume a voltage drop of only one volt, (1.0V) across the resistor giving double the input voltage at 4 volts, a quick calculation would give us a single pull-up resistor value of 50kΩ. Reducing the resistive value further, will produce a smaller voltage drop but increase the current. Then we can see that while there may be a maximum allowable resistive value, the resistance value for pull-up resistors is not usually that critical with resistance values ranging from between 10k to 100k ohms acceptable.

This simple example above gives us the maximum value of the pull-up resistor required to bias a single TTL gate. But we can also use the same resistor to bias multiple inputs to a logic "1" value. For example, lets assume we have constructed a digital circuit and that there are ten unused logic gate inputs. As a single standard TTL 74LS gate, has an input current, $I_{IH(max)}$ of 20μA (also called a fan-in of 1), then ten TTL logic gates would require a total current of: 10 x 20μA = 200μA representing a fan-in of 10.

So the maximum resistive value of the pull-up resistor required to supply ten unused inputs would be calculated as follows:

Multiple Gate Pull-up Resistor Value

$$R_{MAX} = \frac{V_{CC} - V_{IH(MIN)}}{10 \times I_{IH}} = \frac{5 - 2}{10 \times 20 \times 10^{-6}} = 15K\Omega$$

Here the fan-in is given as 10, but if "n" TTL inputs are connected together then the current through the resistance would be "n" times $I_{IH(max)}$. Again as before, this 15kΩ resistance may be the exact calculated value, but leaves no room for error so reducing the voltage drop to one volt (or any value you want) gives a resistive value of only 5kΩ.

Pull-up Resistor Example No1

Two TTL 74LS00 NAND Gates along with a single-pole double-throw switch are to be used to make a simple Set-Rest bistable flip-flop. Calculate: 1). The maximum pull-up resistor values if the voltage representing a logic HIGH input is to be held at 4.5 volts when the switch is open, and 2). The current flowing through the resistor when the switch is closed (assume zero contact resistance). Also draw the circuit.

Data given: Vcc = 5V, V_{IH} = 4.5V, and $I_{IH(max)}$ = 20μA

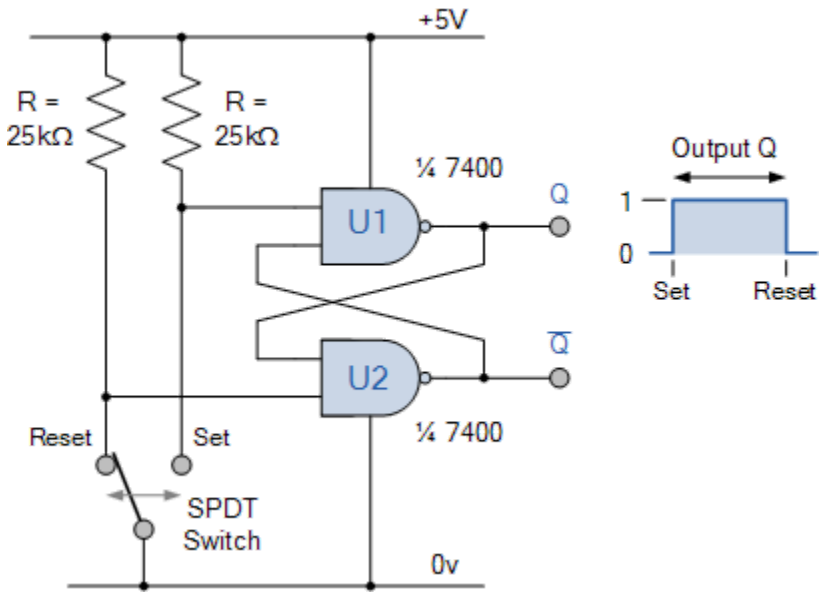
1). Pull-up Resistor value, R_{MAX}

$$R_{MAX} = \frac{V_{CC} - V_{IH}}{I_{IH}} = \frac{5 - 4.5}{20 \times 10^{-6}} = 25K\Omega$$

2). Resistor Current, I_R

$$I_R = \frac{V_{CC}}{R} = \frac{5V}{25k\Omega} = 200\mu A \text{ or } 0.2mA$$

Set-Reset Bistable Circuit



Pull-down Resistors

A *Pull-down resistor* works in the same way as the previous pull-up resistor, except this time the logic gates input is tied to ground, logic level "0" (LOW) or it may go HIGH by the operation of a mechanical switch. This pull-down resistor configuration is particularly useful for digital circuits like latches, counters and flip-flops that require a positive one-shot trigger when a switch is momentarily closed to cause a state change.

While they may seem to operate in the same way as the pull-up resistor, the resistive value of a passive pull-down resistor is more critical with TTL logic gates than with similar CMOS gates. This is because a TTL input sources much more current out of its input in its LOW state.

From above we saw that the maximum voltage level that represents a logic "0" (low) for a TTL 74LSxxx series logic gate is between 0 and 0.8 volts, ($V_{IL(MAX)}$ = 0.8V). Also when LOW, the gate sources current to the value of 400μA, (I_{IL} = 400μA). The maximum pull-down resistor value for a single TTL logic gate is therefore calculated as:

Single Gate Pull-down Resistor Value

$$R_{MAX} = \frac{V_{IL(MAX)} - 0}{I_{IL}} = \frac{0.8 - 0}{400 \times 10^{-6}} = 2K\Omega$$

Then the maximum pull-down resistor value is calculated as 2kΩ. Again, as with the pull-up resistor calculations, this 2kΩ resistor value leaves no room for error as the voltage drop is at maximum. So if the resistance is too large, the voltage drop across the pull-down resistor may result in a gate input voltage beyond the normal LOW voltage range, so to ensure correct switching it is better to have an input voltage of 0.5 volts or less.

Therefore if we assume a voltage drop of only 0.4 volts across the resistor, a quick calculation would give us a single pull-down resistor value of 1kΩ. Reducing the resistive value further, will produce a smaller voltage drop tying the input further to ground (low). This datasheet value of 400μA or 0.4mA (I_{IL}) is the minimum LOW current value but it may be higher.

Also, connecting inputs together will result in a larger current through the resistor. For example, a fan-in of 10 will result in 10 x 400μA = 4.0mA requiring a pull-down resistance of 100Ω.

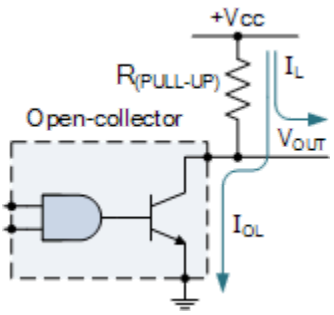
But you might be thinking, why use a pull-down resistor at all when a direct connection to ground (0V) would produce the required LOW?. A direct connection to ground without the pull-down resistor would certainly work in most cases, but as the gates input is permanently tied to ground, the use of a resistor limits the current flowing out of the input thereby reducing power loss while still maintaining a logic "0" condition.

Open-collector Outputs

Thus far we have seen that we can use either a pull-up resistor or a pull-down resistor to control the voltage level of a logic gate. But we can also use pull-up resistors on the output of a gate to allow different gate technologies to be connected, for example TTL to CMOS or for transmission line driving applications that require higher currents and voltages.

In order to overcome this some logic gates are manufactured with the collector of the gates internal output circuitry left open meaning that the logic gate does not actually drive the output HIGH, only LOW as its the job of the external pull-up resistor to do this. One example of this is the TTL 74LS01, Quad 2-input NAND gate which has open collector outputs, as opposed the the standard TTL 74LS00, Quad 2-input NAND gate.

Open-collector, (OC) or open-drain for CMOS, outputs are commonly used in buffer/inverter/driver IC's (TTL 74LS06, 74LS07) allowing for a greater output current and/or voltage capability than you would get with ordinary logic gates. For example to drive a large load such as an LED indicator, a small relay or dc motor. Either way, the principle and use of the pull-up resistor is pretty much the same as for the input.



Logic gates, micro-controllers and other such digital circuits that have open-collector outputs, are incapable of pulling their outputs HIGH as there is no internal path to the supply voltage, (Vcc). This condition means that their output is either grounded when LOW, or floating when HIGH, so an external pull-up resistor, (Rp) needs to be connected from the open-collector terminal of the pull-down transistor to the Vcc supply.

With a pull-up resistor connected, the output still works in the same way as a normal logic gate in that when the output transistor is OFF (open), the output is HIGH, and when the transistor is ON (closed), the output is LOW. Thus the transistor turns ON to pull the output to a LOW level.

The size of the pull-up resistor depends on the connected load and the voltage drop across the resistor when the transistor is OFF. When the output is LOW, the transistor must be able to sink the load current through the pull-up resistor. Likewise, when the output is HIGH, the current through the pull-up resistor must be high enough for whatever is connected to it.

As we saw before with the input, the output of a digital logic gate operates using two binary states which are represented by two distinct voltages: a high voltage V_H for logic "1" and low voltage V_L for logic "0". Within each of these two voltage states, there is a range of voltages which define their upper and lower voltages.

$V_{OH(min)}$ is the minimum output voltage guaranteed to be recognized as a logic "1" (HIGH) output and for TTL this is given at 2.7 volts. $V_{OL(max)}$ is the maximum output voltage guaranteed to be recognized as a logic "0" (LOW) output and for TTL this is given as 0.5 volts. In other words, TTL 74LSxxx output voltages between 0 and 0.5V are considered "LOW", and output voltages between 2.7 and 5.0V are considered "HIGH".

So when using open-collector logic gates, the value of the pull-up resistor required is determined from the following equation:

Open-collector Pull-up Resistor Value

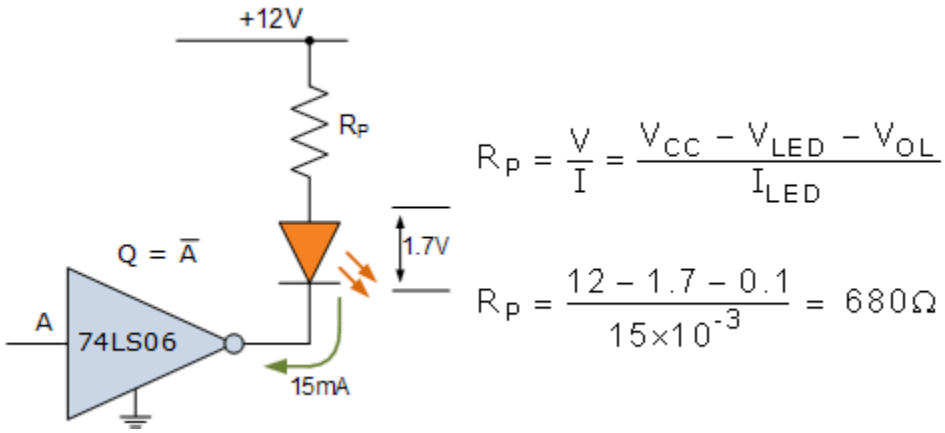
$$R_{MIN} = \frac{V_{CC} - V_{OL(MAX)}}{I_{OL}} = \frac{5 - 0.5}{8 \times 10^{-3}} = 562\Omega$$

Where the values for a 7401 open-collector NAND are given as: Vcc = 5V, V_{OL} = 0.5V, and $I_{OL(max)}$ = 8mA. Note that it is important to calculate a suitable pull-up resistor Rp as the current through the resistor must not exceed $I_{OL(max)}$.

We said earlier that open-collector logic gates are ideal for driving loads that require higher voltage and current levels, such as an LED indicator. The TTL 74LS06 Hex Inverter Buffer/Driver has an $I_{OL(max)}$ rating of 40 mA (instead of 8mA for the 74LS01) and a $V_{OH(max)}$ rating of 30 volts instead of the usual 5 volts (but the IC itself MUST use a 5V supply). Then the 74LS06 will allow us to drive a load up to 40mA of current.

Pull-up Resistor Example No2

A 74LS06 Hex Inverter Driver is required to control a single red LED indicator from a 12 volt supply. If the LED requires 15mA at 1.7V voltage drop and the V_{OL} of the HEX Inverter when fully ON is 0.1 volts, calculate the value of the current limiting resistor required to drive the LED.



We can use open-collector drivers in a similar way to drive small electromechanical relays, lamps or dc motors as these devices typically require 5V or 12V or more, at a current of about 10 to 20 mA's to operate correctly.

Two or more open-collector outputs of TTL gates can be directly connected together and tied through a single external pull-up resistor. The result is that the outputs are effectively AND'ed together as the combination behaves as if the gates were connected to an AND gate. This type of configuration is called wired AND logic.

Pull-up Resistor Summary

We have seen here in this tutorial about passive pull-up and pull-down resistors that when left open–circuited, the inputs of digital logic gates may self–bias or float about to whatever logic level they choose and many switching errors can be traced back to unconnected and floating input pins.

A pull-up resistor connects unused input pins (AND and NAND gates) to the dc supply voltage, (Vcc) to keep the given input HIGH. A pull-down resistor connects unused input pins (OR and NOR gates) to ground, (0V) to keep the given input LOW. The resistance value for a pull-up resistor is not usually that critical but must maintain the input pin voltage above V_{IH}. The use of 10kΩ pull-up resistors are common but values can range from 1k to 100k ohms.

Pull-down resistors are a little more critical because of the low input voltage level, $V_{IL(max)}$ and the higher I_{IL} current. The use of 100Ω pull-down resistors are the most common but they can range in resistive value from 50 up to 1k ohms.

Digital logic gates with open-collector (in the case of the TTL logic) outputs or open-drain (in the case of the CMOS logic) outputs need to connect to an external pull-up resistor between their output pin and the dc power supply to make the logic gate perform the intended logic function.

The advantage of using open collector/open drain gates is in their capability to switch higher voltages and currents or their ability of provide wired ANDing operation. Some open-collector gates, such as the 74LS06 are capable of driving larger loads because their outputs can be connected to supplies of up to 30 volts via an external pull-up resistor.

21 Comments

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SUBMIT

K Kenneth Gwara

Very Good Notes

Posted on September 18th 2018 | 7:18 pm

Reply

O Osayande Charles Owen

I really love your write up , it was very explanatory.God bless . I am a 400 level electronics student from an African university, I have the burning in me to really indulge in full flared electronics design, I needed assistance as to how I can get resources and materials to study the major IC's in electrons , as in a very detailed piece of work.

Posted on August 19th 2018 | 11:36 pm

Reply

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j jw lee

Get a wonderful insight here, Thanks a lot!

Posted on August 08th 2018 | 1:38 am

Reply

E Easy E

What is the difference between using a SPDT switch that directly connects the inputs of the Logic IC to the 5v and the ground, and the use of a pull up/pull down?

Posted on July 24th 2018 | 6:04 am

Reply

N Nick

I think I know what my problem is – I was thinking of MOSFETs when reading this and not of transistor logic and reverse biasing.

Posted on July 16th 2018 | 11:22 am

Reply

N Nick

I completely lost you when you said (without any diagram reference):
“When logic gates are connected together, the current flows between the output of one logic gate and the input of another. The amount of current required by a basic TTL logic gate input depends on whether the input is a logic “0” (low) or a logic “1” (high) as this creates a current-sourcing action for a logic “0” and a current-sinking action for a logic “1”.

When the input of the logic gate is HIGH, a current flows into the TTL input as the input acts basically as a path connected directly to ground. This input current, IIH(max) is positive in value as it flows “into” the gate and for most TTL 74LSxxx inputs have a value of 20μA.

Likewise, when the input of the logic gate is LOW, the current flows out of the TTL input as the input acts basically as a path connected directly to Vcc. This input current, IIL(max) is negative in value as it flows “out-of” the gate and for most TTL 74LSxxx inputs, has a value of -400uA, (-0.4mA).”
I thought “what?” why am I trying to think of 2 logic gates all of a sudden? And current flows out of the TTL input – how? …fried grey matter followed but I sort of rebalanced my mind when you started on “Single Gate Pull-up Resistor Value”.

Then when you start on “Pull-down Resistors” it gets confusing again, as you talk “a TTL input sources much more current out of its input in its LOW state” whereas I think of a TTL input gate sinking current i.e., current flows into the device.
So when you then go on about “Single Gate Pull-down Resistor Value” and say “This datasheet value of 400uA or 0.4mA (IIL) is the minimum LOW current value but it may be higher.” I’m thinking what? – a low minimum current would be zero input? I think it needs a figure annotated to explain this.

Posted on July 16th 2018 | 10:54 am

Reply

S Scotty Bob

Phenomenal! Now, if you could explain Bode diagrams, Kalman filters, and PID controllers in a similarly simple and clear, yet useful and understandable – that’d be great.

Posted on June 28th 2018 | 2:47 am

Reply

J Juzzy

Nice, was really helpful

Posted on April 15th 2018 | 1:04 pm

Reply

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j joffrey

How to deside pull up resistor is needed for circuit. some time we will not use pull up or pull down resitor for some MCU

Posted on April 09th 2018 | 8:02 am

Reply

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m mart

The Set-Reset Bistable Circuit diagram has the labels ‘set’ and ‘reset’ reversed.

Posted on April 08th 2018 | 2:04 pm

Reply

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