

Name:

MINI TEST (Feb-2025)

Sub: Computer System Organization
Time: 1 hourSch. No
Sub Code: CS 222
Max. Marks: 10

Q.No	Questions	Marks																					
1	<p>Consider the following binary code, processed on an addition hardware</p> <pre> 10110110 01101010 </pre> <p>a) What is the status of carry overflow flag in the register. b) Find the result when data is in the unsigned format (in decimal). c) Find the result when data is in the signed format.</p>	2																					
2	<p>A machine support 16-bit instruction format, the size of address field is 4-bit. The computer support expanding opcode technique and has 55000 Zero-address instruction and 100 One-address instructions. Find out the Number of two-address instructions supported by this machine.</p>	2																					
3	<p>Consider 32-bit hypothetical CPU used to execute the following code:</p> <table border="1"> <thead> <tr> <th>Instruction</th><th>Size in Words</th><th>In bytes(B)</th></tr> </thead> <tbody> <tr> <td>I1</td><td>2</td><td>8B</td></tr> <tr> <td>I2</td><td>1</td><td>4B</td></tr> <tr> <td>I3</td><td>2</td><td>8B</td></tr> <tr> <td>I4</td><td>2</td><td>8B</td></tr> <tr> <td>I5</td><td>1</td><td>4B</td></tr> <tr> <td>I6</td><td>2</td><td>8B</td></tr> </tbody> </table> <p>(a) Assume that program is stored in the memory with a starting address of 1000 decimal onwards. What would be the value present in the PC during the execution of a I5 instruction? (b) Assume that memory is word addressable and word size = 32 bit. Program is stored in the memory with starting address of (ABC)H. What could be the value present in the PC during the execution of I5 instruction?</p>	Instruction	Size in Words	In bytes(B)	I1	2	8B	I2	1	4B	I3	2	8B	I4	2	8B	I5	1	4B	I6	2	8B	2
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4	<p>A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then determine the maximum number of distinct R-type opcodes?</p>	2																					
5	<p>Consider 16-bit hypothetical CPU which supports one-word long instructions. Instruction contains 8-bit opcode and 8-bit address field. Instruction is stored in the memory with a starting address of 800 decimal onwards. Processor supports register R0, which contains 200. When the instruction is designed with a memory reference instruction then the address field contain 100. Memory content of 100 is 300. Calculate the Effective Address (EA) if the addressing mode of instruction is:</p> <p>i. Immediate ii. Register iii. Direct iv. Indirect v. Register Indirect vi. Indexed with R0 as an index register. vii. PC Relative viii. Base Register</p>	2																					