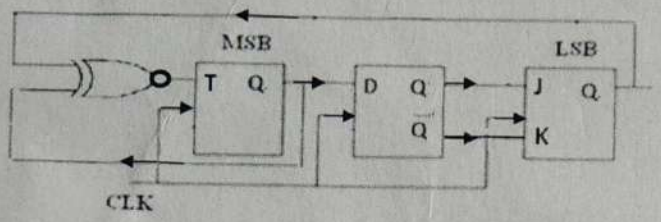
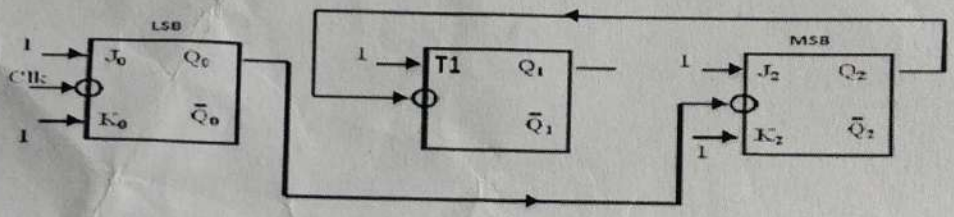
(b) Design a 4-bit counter for prime number sequences using T flipflop. (5)

Q. 4 (a) Consider the following Counter Circuit. The F/Fs are positive edge triggered FFs with initial state 111. Find the correct state sequence of the circuit. (5)



(b) Consider the following Ripple Counter. The F/Fs are negative edge triggered FFs with initial state 000.



Find the correct state sequence of the circuit.

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MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

EXAMINATION: END TERM EXAM **MONTH & YEAR:** NOV 2025

Course: B. Tech Semester: III Branch: CSE

Subject Name: Digital Circuit Design Subject Code: CSE24 213

Time: 120 minutes Max Marks: 40

NOTE: Answer all Questions. Attempt all the parts of a Question in continuation.

Q. 1 (a) Given function F (A, B, C, D) = ∑m (0, 1, 2, 4, 5, 6, 7, 15) is orthogonal or not. Also find possible number of orthogonal functions with four variables. (5)

(b) Consider realization of 1 X 64 Demux from 1 X 4 Demux if input at select line is 100110. Find Demux number and its output line number at last stage which shows the input and draw the circuit. (5)

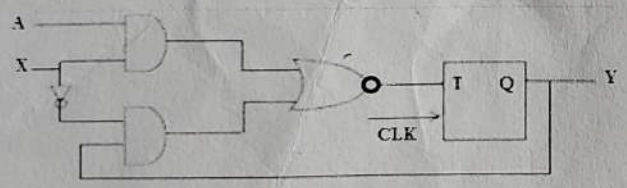
Q. 2 (a) Two researchers Mohan and Sohan have got an assignment to perform parallel subtraction of two 100-bit binary numbers. Mohan proposes an approach to perform subtraction with the help of parallel adder circuit which of constructed with the help of full adders and NOT gates, while Sohan Proposes an approach to perform subtraction with the help of parallel subtractor circuit which of constructed with the help of full subtractors.

(i) Draw logical circuits of both the approaches. (2)

(ii) Compute the overall time delay to perform subtraction of two 100-bit binary numbers using both the approaches when the time delay of a NOT gate, an XOR gate, an AND gate and an OR gate is 1, 3, 2, and 2 time units respectively. (3)

(b) Amount of time needed to generate sum and carry by 4bit lookahead carry adder if delay of X-OR, AND, OR GATE is 5n, 2n, n respectively, where n is no. of input to these gates. (5)

Q. 3 (a) Consider the following CKT involving a positive edge triggered T F/F (initially zero). (5)



Consider the following timing diagram. Find the timing diagram for output Y.