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MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

EXAMINATION: MIDTERM EXAM **MONTH & YEAR:** OCT 2024

Course: B. Tech	Semester: III	Branch: CSE
Subject Name: Digital Circuit Design		Subject Code: CS 214
Time: 90 minutes		Max Marks: 20

NOTE: Answer all Questions. Attempt all the parts of a Question in continuation. All question carry equal marks.

Q. 1 Consider radix-27 number system where digits range from 0 to 26. The digits representation in radix-27 number system is divided into two parts, First part has range from 0 to 9 and its representation is in normal decimal representation, means 0 – 0, 1 – 1, ..., 9 – 9 and Second part has range from 10 to 26 and its representation is detonated by alphabet codes, means 10 – A, 11 – B, 12 – C, ..., 24 – O, 25 – P, 26 – Q. Find an equality **(4)(CO1)**

(i) $(727058.347108)_9 = (?)_{27}$

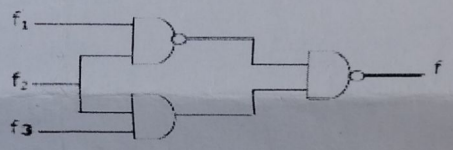
(ii) $(A\$J\$.\$2\$H)_{27} = (\$34\$57.66\$54\$)_9$ Find rigits at the location of $.

Q. 2 Consider the logic circuit shown in the figure below. The function f_1, f_2 and f_3 are

$f_1(w, x, y, z) = \Sigma 1, 3, 6, 8, 9, 10, 15$

$f_2(w, x, y, z) = \Sigma 1, 2, 5, 6, 9, 12, 14$

$f_3(w, x, y, z) = \Sigma 0, 1, 3, 5, 8, 12, 15$



Find f (w, x, y, z) in standard SOP. **(4) (CO2)**

Q. 3 Consider a 16 bit floting point format form MSB to LSB with 1 Sign bit, 7 bit biased Exponent and 8 bit fraction Mantissa with implicit 1 after radix point. **(4)(CO1)**

(i) Find the range of the floating point format

(ii) Find the real number represented as hexadecimal in the given format

(a) FFF0 (b) EAD9

Q. 4 Consider the design of a circuit in the form of levels inorder to minimize the time delay of boolean function f. All the logic gates present at any i^{th} level:

1. Receive inputs from the outputs of logic gates present at $(i-1)^{th}$ level.
2. Supply their outputs as inputs to logic gates present at $(i+1)^{th}$ level.
3. Work parallely to minimize time delay.

The circuit of boolean function f can be designed by either two inputs NAND or two inputs NOR but not both. The time delay of each of the logic gate is 2 time unit. Find the minimum time delay for the implentation of boolean function f ? **(4)(CO2)**

$f(w, x, y, z) = \sum m(1, 2, 5, 12) + \sum d(0, 7, 8, 10, 13, 15)$

PTO...

Q. 5 The literal count of a Boolean expression is the number of times each literal apprears in the expression. For example, the literal count of $(xy + x z')$ is 4. What are the minimum possible literal counts of the POS and SOP representations respectively of the function given by the following map? (Note: the map contains minterms) **(4)(CO2)**

cd \ ab	00	01	10	11
00				1
01	X	X	X	1
10		1		1
11		1		1