MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY BHOPAL

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

EXAMINATION: END TERM | MONTH and YEAR: May 2025

Name of the Student: Tanish | **Scholar Number**: 231120122 9

Course: B.Tech | Semester: Fourth | Subject Code: CSE 222

Subject Name: Computer System Organization | Maximum Marks: 50

Duration: 3: 00 Hours | Date: 08/05/2025 | Time: 3:00 PM to 6:00PM

Note: All questions are compulsory. Write all necessary steps clearly.
Write your subsection answers in one place for each question.

Q. No		Questions	Marks	COs
1	a)	While browsing at Hari's computer shop, you overhear a customer asking Hari what the fastest computer in the store is that he can buy. Hari replies, "You're looking at our MacBooks. The fastest Mac we have runs an Apple M2 chip at 3.2 GHz. If you really want the fastest machine, you should buy our Intel Core i9-13900K, which runs at 5.8 GHz." Is Hari correct? What would you say to help this customer?	2	CO 1
	b)	Given sign number representation, perform the following operations using 16-bit representation and calculate the result in hexadecimal number. Note: write each step clearly. i. $(99)_{10} + (-511)_{10}$ ii. $(-99)_{10} - (-511)_{10}$ iii. $(0FEA)_{16} * (32)_{10}$ iv. $(FFE0)_{16} / (16)_{10}$	4	
	c)	The IEEE single precision floating point standard allows us to represent less than 2^{32} different numbers. Calculate the following: i. How many numbers are strictly between 2^{-5} and 2^{-4} ii. How many numbers are strictly between 2^{47} and 2^{50}	4	
2	a)	Write an assembly language 8086 program to calculate factorial of given number.	2	CO 2
	b)	A digital computer has a common bus system for 8 registers of 4 bits each. The bus is constructed with multiplexers. Draw the neat and clean diagram to configure the circuit. Also, calculate the following: i. How many selection inputs are there in each multiplexer? ii. What sizes of multiplexers are needed? iii. How many multiplexers are there in the bus?	4	
	c)	Consider a hypothetical CPU that supports 256 distinct instructions, with each instruction requiring 10 micro-operations (cycles) to execute. The CPU uses a horizontal micro- programmed control unit with 200 control signals to orchestrate operations. Additionally, the CPU hardware includes 8 status flags and supports 16 distinct branch conditions. The control unit uses Control Address Register (CAR) and Control Data Register (CDR) to manage micro-instruction sequencing. The CPU follows a 1-address micro-instruction format by default for handling control flow and branching logic. Answer the following: i. What should be the size (in bits) of the Control Address Register (CAR) to support the microprogram memory addressing? ii. What should be the size (in bits) of the Control Data Register (CDR) to encode the horizontal micro-instruction?	4	
3	a)	A legacy sequential application is to be parallelized for execution on a shared-memory multiprocessor system comprising eight homogeneous processing cores. Assuming the parallelizable portion of the program can be evenly distributed across the available processors with negligible overhead, determine the minimum required fraction of the program (P) that must be parallelized to achieve an overall execution speedup of 5, as predicted by Amdahl's Law.	2	CO 3
	b)	Consider four stage pipelines (IF, ID, EX, WB) used to execute the program where all the instructions are spending one cycles on all the stages, but "MUL" and "DIV" instructions takes 4 and 5 cycles, respectively on EX stage. Pipeline uses operant forwarding as an optimization technique to handle the stalls (Data Dependency) Program: I1: DIV r0, r1, r2 I2: MUL r3, r1, r2 I3: ADD r4, r3, r1 I4: SUB r5, r4, r2 i. How many cycles are required to execute the program? ii. How many cycles are saved using optimization over unoptimized (no operand forwarding) execution of the data?	4	
	c)	Consider a four stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below: Note: CPU uses optimization techniques to make effective pipeline: there is no need to wait for completion of i^{th} iteration, it may start to execute $i^{th}+1$ iteration simultaneously.	4	

	S1	S2	S3	S4
I1	1	2	2	1
I2	2	1	1	2
I3	2	2	1	1
I4	2	2	1	2

Calculate the following:

i. How many cycles are required to complete the following loop:
`For (i=1 to 2) {I1; I2; I3; I4;}`

ii. How much time is required if the program executes with a processor speed of 5MHZ?

iii. Calculate MIPS

iv. How much time is required to execute the same code with 100 iterations?

4	a)	What is the distinction between spatial locality and temporal locality? Write which types of localities of the following cases with proper explanation: i. Using CPU cache to store recently accessed data ii. Structuring data fields together in memory (e.g., structs) iii. Loop fusion iv. Sequential file reading or memory scanning	2	CO 4
	b)	The access time of a cache memory is 100ns and that of main memory 1000ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write operation. The hit ratio for read access is 0.8. A write-through procedure is used. i. What is the average access time of the system considering only memory read cycle? ii. What is the average access time of the system considering only memory write cycle? iii. What is the average access time of the system for both read and write requests? iv. What is the average hit ratio?	4	
	c)	A computer system uses 32-bit memory addresses for main memory access. It has a 4K-byte cache organized in the block-set-associative manner, with 4 blocks per set and 64 bytes per block. i. Calculate the number of bits in each of the Tag, Set, and Word fields of the memory address. ii. Assume that the cache is initially empty. Suppose that the processor fetches 1088 words of four bytes each from successive word locations starting at location 0. It then repeats this fetch sequence nine more times. Calculate hit ratio of cache, If FIFO block replacement policy is used for block transfer from cache to main memory.	1+3	
5	a)	Why is the daisy chain method of priority interrupt not scalable for systems with many devices? Justify the statement.	2	CO 5
	b)	Consider three different machines—Machine A, Machine B, and Machine C—each using a different method to handle I/O operations with an attached I/O device. • Machine A has a 200 MHz processor and uses polling to interact with the I/O device. By default, the processor polls every 0.5 ms. It takes 500 CPU cycles per poll, and takes 10,000 cycles to resolve once the handler has been started. • Machine B has a 250 MHz processor and uses interrupt-driven I/O. It takes 1,000 cycles to perform a context switch and start the interrupt handler, and another 1,000 cycles to return to the original program. The device processing time is 10,000 cycles after the handler is initiated. • Machine C has a 300 MHz processor and supports cycle-stealing DMA. Whenever 10-Byte data block is available in the buffer, then it is transferred to the main memory. It takes 1,000 cycles to initiate a DMA transaction and 1,500 cycles to handle the interrupt upon completion. Calculate the fraction of the CPU's time spent handling the data transfer for Machine A, Machine B, and Machine C, assuming that in each case an I/O device attached to each machine transfers 150 bytes/Sec.	4	
	c)	A system uses daisy chain priority interrupt for four devices: P, Q, R, S. The priority order is: P (highest) → Q → R → S (lowest) Each device, once acknowledged only and takes 2 ms to service. At time t = 0 ms, all devices are idle. Interrupt requests come in at the following times: Device Q: at t = 1 ms, Device S: at t = 5.5 ms Device P: at t = 8.5 ms, Device R: at t = 6.5 ms. The CPU checks for interrupts every 1 ms, and services one interrupt at a time using daisy chain priority. There is no preemption of servicing begins, it must finish before moving to the next. Find out the following i. In what order will the devices be serviced? ii. Calculate average waiting time and average completion time to all devices.	4	

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Faculty Coordinators: 1. Dr. Rajesh Wadhwani (डॉ. राजेश वाधवानी)

2. Dr. Ashish Kumar Sahu (डॉ. आशीष कुमार साहू)