MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY BHOPAL

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

EXAMINATION: MID TERM MONTH and YEAR: March 2025

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Course: B.Tech Semester: Fourth Subject Code: CSE 222

Subject Name: Computer System Organization Maximum Marks: 20

Duration: 1: 30 Hrs Date:17/03/2025 Time:3:30 PM to 5:00PM

Note: All questions are compulsory.

Q. No	Questions	Marks	COs
1	Draw the table that contains binary value from 00000 to 11111and the equivalent decimal values of IEEE 5-bit floating point representation. The size of sign, exponent, and mantissa is 1 bit, 2 bit, and 2 bit, respectively. The special values are shown in the following table:	3	CO1

Sign Bit	Exponent Bit	Mantissa Bit	Value
0/1	All Zero	All Zero	{-0,+0}
0/1	All One	All Zero	{-∞, +∞}
0/1	All Zero	Non Zero	Denormal floating values
0/1	All One	Non Zero	NaN

2	Consider two different machines, with two different instruction sets, both of which have a clock rate of 400 MHz, 500 MHZ, respectively. The following measurements are recorded on the two machines running a given set of benchmark programs:	4	CO3

	Machine A		Machine B	
Instruction Type	Instruction Count (millions)	Cycles per Instruction	Instruction Count (millions)	Cycles per Instruction
Arithmetic and logic	8	1	10	1
Load and store	4	3	8	2
Branch	2	4	2	3
Others	4	3	4	2

Machine A uses 10-stage pipeline. The target address of the instruction is available on the 5th stage. Similarly, machine B uses 12-stage pipeline and the target address is available on the 8th stage. Only the branch instruction creates extra stalls, the remaining types of instructions do not have any stalls.

i. Determine the effective *CPI*, MIPS rate, and execution time for each machine.
ii. Find out which machine is faster?

3	Assume an instruction set that uses a fixed 16-bit instruction length. The operand specifiers are 6 bits in length. There are K two- operand instructions and L zero-operand instructions. What is the maximum number of one- operand instructions that can be supported?	2	CO2
4	Consider 32-bit hypothetical CPU which supports lw instructions with opcode, 3-register operands, and immediate fields. CPU contain 24 registers with a register size of 32 bit, and supports 256 kB memory space. CPU instruction set size is 240. What is the largest unsigned constant possible in the instruction.	2	CO2
5	A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. The Register R contains the value P. State how Z is calculated from the other addresses if the addressing mode of the instruction is i) direct ii) indirect iii) immediate iv)indexed v) register vi) register indirect	3	CO2
6	Design a 4-bit arithmetic unit which performs the following arithmetic operations on three registers A, B and C. After designing, draw the truth table. The components are available: Full adder, half adder, multiplexer, NOT gate. The number of control signals are two $\{s_0, s_1\}$and c_{in} for the carry. The operations are: A+B, A+B+1, ~A+B, B-A, ~C+B, B-C, A+B+(~C), A+B-C Note: ignore the c_{out}, if occurs.	3	CO1
7	Consider 5 stage pipelines, operating with 2ns clock which allows all the instructions accept the branch instruction, means Processor stop the fetching of following instructions after the JMP instructions in the program, until the target address is available. In the Pipeline, the target address	3	CO3

	is available, when the instructions is completed.program contain 40% branch instruction among them 60% are conditional in which 40% instructions does not satisfy the condition when the condition is false, then the following instruction are overlapped i) What is the average instruction execution time? ii) What is the performance gain (s)?		

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