Name of the Student Rahul Agrawal Roll No. 23112c1268

MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

EXAMINATION: END TERM EXAM **MONTH & YEAR:** NOV 2024

Course: B. Tech Semester: III Branch: CSE

Subject Name: Digital Electronics Subject Code: CSE 214

Time: 180 minutes Max Marks: 50

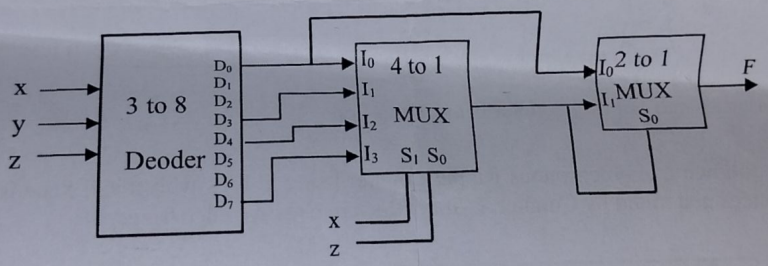
Note: Answer all Questions. Attempt all the parts of a Question in continuation.

Q. 1 (a) Check whether the given function f(A, B, C, D) = Σm (1, 2, 15, 0, 6, 5, 4, 7) is an orthogonal function or not. If yes, then find the number of orthogonal functions? (5) CO1

(b) In a prime implicant chart representing a Boolean expression f(w, x, y, z). Columns represent minterms and rows represent prime implicants. Identify P, Q, R, S, a, b. (5) CO2

	0	4	5	7	8	a	b
P	✓	✓					
Q	✓				✓		
R		✓	✓				
S			✓	✓		✓	✓

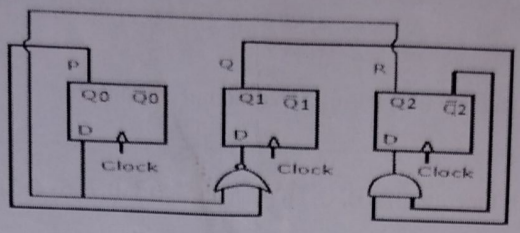
Q. 2 (a) Consider the following combinational circuit implemented using 3 to 8 decoder, 4 to 1 MUX and 2 to 1 MUX. Find the output F in standard sum of product (SOP) form. *(5) CO3*



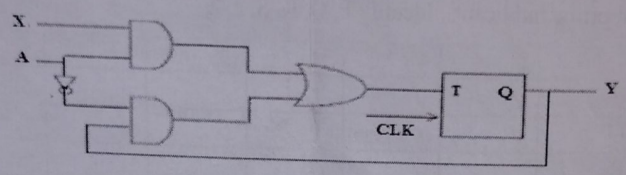
(b) Consider a 100-bit parallel adder and subtractor circuit that is designed with the help of NOT, OR, AND, NAND and NOR gates only. The cost and time delay of each gate is 1 rupee and 1 time unit respectively. What will be the total time delay and total cost to implement the subtractraction operation of two 100-bit numbers? Compare the delay and cost of this system with a 100-bit look-ahead carry subtractor circuit. (5) CO3

Q. 3 (a) Consider realization of **64 X 1** MUX from **4 X 1**. If input given at select lines is 100110. Find MUX number and its input line number at stage1 which is shown as output.? (5) CO3

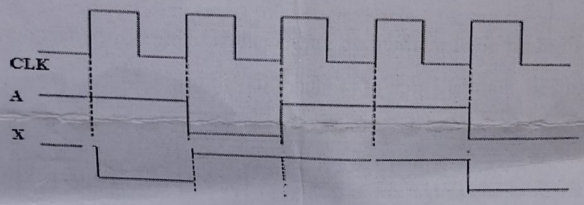
(b) Consider the following sequential synchronous circuit with initial state $Q_0 = Q_1 = Q_2 = 0$. The state of the circuit is given by the equation $4R + 2Q + P$. What will be the counting sequence of the circuit? (5)CO4



Q. 4 (a) Consider the following CKT involving a positive edge triggered T F/F (initially zero). (5)

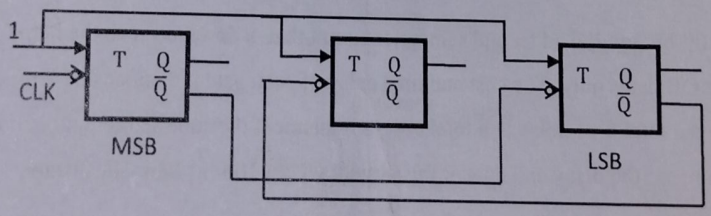


Consider the following timing diagram. Find the timing diagram for output Y.



(b) Construct 4 bit switch tail ring counter using T flip flop. (5)CO4

Q. 5 (a) Consider the following Asynchronous Ripple Counter using T F/Fs with initial State is 000. Find the counting sequences generated by Counter. (All the f/fs are negative edge triggered) (5)CO4



(b) Consider a serial in Serial out register with initial state $Q0 = Q1 = Q2 = 0$. The following data: 1011011 is supplied to the data terminal from LSB one bir per clock. What will be the content of shift register after 7^{th} clock cycle? (5)CO4