Mahbod Afarin

Rooms 2132, CSE Department, UC San Diego, CA

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Professional Summary

Postdoctoral Scholar at UC San Diego with over 5 years of experience in hardware accelerators, compiler design, and graph analytics, working across architecture, runtime, and LLVM/MLIR-based compiler stacks. Demonstrated ability to deliver high-impact research results, with successful technology deployment at Google and publications in top-tier conferences.

Technical Skills

Languages: C/C++, Python, CUDA, OpenMP, OpenCL, SQL
Compiler Design: LLVM, MLIR, LLVM-BOLT, LLVM Machine Outliner
Hardware Design: VHDL, Verilog HDL, SystemC, Xilinx ISE, Altera Quartus, Synopsys Design Compiler
Simulation & Modeling: Multi2Sim, GPGPU-Sim, Mentor Graphics Modelsim, HSPICE, PSPICE, IC Encounter, HSIM, Cadence SoC Encounter, Structural Simulation Toolkit

Education

University of California Riverside   Jan. 2020 – Jun. 2025
Doctor of Philosophy (Ph.D.) in Computer Science   *Riverside, California*

- *Thesis: "Redundancy Removal for Accelerating Graph Processing Workloads"*
- *Advisors: Professor Rajiv Gupta & Professor Nael Abu-Ghazaleh*
- *GPA: **3.86**/4*

Sharif University of Technology   Sep. 2015 – Jan. 2018
Master of Science (M.Sc.) in Computer Engineering   *Tehran, Iran*

- *Thesis: "Improving Life Cycle of SIMT Processors for Approximate Computing" (Thesis Grade: Excellent)*
- *Advisors: Professor Shaahin Hessabi*
- *GPA: 4/4 (**19.03**/20) (ranked **7th** among 83 computer engineering students)*

Research Experience

University of California San Diego   Jun. 2025 – Present
Postdoctoral Scholar   *San Diego, California*

- Member of the *System Energy Efficiency (SEE) Lab* and the *Processing with Intelligence Storage & Memory (PRISM)* Research Center at UC San Diego, under the supervision of Professor *Tajana Rosing*.
- Developing MLIR-based compiler support targeting *Dynamic Programming Processing in Memory Hardware Accelerators*.

Google   Sep. 2024 – Dec. 2024
Student Researcher   *Sunnyvale, California*

- Member of the *Compiler Optimization* team at **Google** working on *Inter-procedural Identical Basic Block Folding*.
- Developed scalable post-link and inter-procedural identical basic block folding techniques to eliminate redundant basic blocks, reduce binary code size, and maintain performance using profiling-guided analysis.

University of California Riverside   Jan. 2020 – Jun. 2025
Graduate Research Assistant   *Riverside, California*

- Member of the *Graph Analytics with Scalability and Performance (GRASP)* and the *RIverside Programming Language & Software Engineering (RIPLE)* centers, supervised by Professor *Rajiv Gupta* & Professor *Nael Abu-Ghazaleh*.
- Developed HW/SW approaches to accelerate dynamic graph workloads, along with designing hardware accelerators.

Sharif University of Technology   Dec. 2015 – Jan. 2018
Graduate Research Assistant   *Tehran, Iran*

- Member of the Very Large Scale Integration Laboratory (VLSI-Lab), supervised by Professor *Shaahin Hessabi*.
- Improved SIMT processor life cycle for approximate computing through techniques that extend hardware longevity.

Publications

C1. [**_EuroSys'24_**] X. Jiang, **M. Afarin**, Z. Zhao, N. Abu-Ghazaleh, R. Gupta, "Core Graph: Exploiting Edge Centrality to Speedup the Evaluation of Iterative Graph Queries," *2024 Proceedings of the Nineteenth European Conference on Computer Systems (Acceptance rate: 15.99%)* (Contributed Equally with the First Author).

C2. [**_MICRO'23_**] C. Gao, **M. Afarin**, S. Rahman, N. Abu-Ghazaleh, R. Gupta, "MEGA Evolving Graph Accelerator," *2023 56th Annual IEEE/ACM International Symposium on Microarchitecture (Aacceptance Rate: 22%)* (Contributed Equally with the First Author).

C3. [**_ASPLOS'23_**] **M. Afarin**, C. Gao, S. Rahman, N. Abu-Ghazaleh, R. Gupta, "CommonGraph: Graph Analytics on Evolving Data," *International Conference on Architectural Support for Programming Languages and Operating Systems. (Acceptance rate: 26.66%)*

C4. [**_MICRO'21_**] S. Rahman, **M. Afarin**, N. Abu-Ghazaleh, R. Gupta, "JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator," *2021 54th Annual IEEE/ACM International Symposium on Microarchitecture. (Acceptance rate: 21.74%)*

C5. [**_HOPC'23_**] **M. Afarin** et al., "CommonGraph: Graph Analytics on Evolving Data (Abstract)," *In Proceedings of the 2023 ACM Workshop on Highlights of Parallel Computing.*

C6. [**_BigData'23_**] A. Mazloumi, **M. Afarin**, R. Gupta, "Expressway: Prioritizing Edges for Distributed Evaluation of Graph Queries," *2023 IEEE International Conference on Big Data.*

C7. [**_Under Review_**] C. Mamatha, **M. Afarin**, R. Gupta, S. Tallam, H. Shen, and X. D. Li., "DeduBB: Binary Code Size Reduction via Post-Link Basic Block De-duplication," *ACM 2026 International Conference on Compiler Construction.*

C8. [**_Under Review_**] **M. Afarin** et al., "UVVs: Identifying Unchanged Vertex Values in Evolving Graphs via Intersection-Union Analysis," *40th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2026).*

C9. [**_Under Review_**] C. Gao, **M. Afarin**, X. Yin, N. Abu-Ghazaleh, R. Gupta, "Sagas: Temporally Consistent Sampling of Evolving Graphs," *IEEE International Conference on Big Data.*

C10. [**_Under Review_**] C. Gao, X. Yin, **M. Afarin**, N. Abu-Ghazaleh, R. Gupta, "Indexing Evolving Graphs via Query Evolution Prediction," *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2026).*

Awards & Achievements

- Won **_UCR Dissertation Completion Fellowship Award_** at UC Riverside, 2024.
- Received the **_Excellent Service_** badge in all three cycles of ASPLOS'24 Artifact Evaluation, 2024 (Certificate).
- Won **_UCR GSA Travel Grant Award_** at University of California, Riverside, 2023.
- Won **_Dean's Distinguished Fellowship Award_** at University of California, Riverside, 2019.
- **_Ranked 7th_** among 83 Computer Engineering students at Sharif University of Technology (**_Top 8%_**), 2018.
- Admitted as an **_Exceptional Talent_** at Sharif University of Technology for M.Sc, 2015.
- **_1st Rank_**, highest B.Sc GPA among all Computer Engineering graduates at Shahed University, 2015.

Teaching Experience

- Teaching Assistant, **_Compiler Design_** (Summer'21/22/23 and Spring'21/22), UC Riverside, CS Dept., Prof. Rajiv Gupta
- Teaching Assistant, **_System on Chip_** (Spring'18) **Testability** (Fall'17) **_Advanced VLSI_** (Spring'17) **_VLSI_** (Fall'16), Sharif University of Technology, CE Dept., Prof. Shaahin Hessabi.
- Lab Instructor, **_Logic Design Lab_** (Summer 2017), and **_Digital System Design Lab_** (Summer 2016), Sharif University of Technology, Department of Computer Engineering, Prof. Maziar Goudarzi.

Professional Services

Audio/Video Chair: ASPLOS'24 Conference
Reviewer: CAL'23, TACO'23, IEEE Transactions on Computers'23, Parallel Computing'23 & 25
Talks: HOPC'23, Society of Women Engineers (UCR, Winter'24), Tulane Uni. (Winter'25), & Binghamton Uni. (Spring'25)
Artifact Evaluation Committee: ASPLOS'25, ASPLOS'24, ISCA'24

References

Professor Tajana Rosing, My Postdoc Supervisor – (Email | Homepage)
Professor Rajiv Gupta, My Ph.D. Supervisor – (Email | Homepage)
Professor Nael Abu-Ghazaleh, My Ph.D. Supervisor – (Email | Homepage)