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Sr. No.	Experiment Description	Experiment Date	Submission Date	Remarks / Signature
1.	A non-pipelined ---------- of instructions is?			
2.	A processor can ---------- at least ___ bits.			
3.	A processor has 40 ---------- operand field is?			
4.	The instruction pipelined ---- sequence of instruction is?			

Q1: A Non-pipeline Single Cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with 5 stages, requiring 1.5, 2.5 ns, 2.0 nsec. 1.5 ns and 2.5 nsec. respectively. The delay of latches is 0.5 nsec. The speed of pipelined processor for a larger no. of instruction?

Sol: For non-pipelined System time required = $2.5+1.5+2.0+1.5+2.5 = 10$

For pipelined System = Max (Stage delay) + Max (latch delay)
$= 2.5 + 0.5 = 3.0$

Speed up = $\frac{\text{time in non-pipelined System}}{\text{time in pipelined System}} = \frac{10}{3}$

$= 3.33$ Ans

Q2: A processor can support a memory of 4 GB where the memory is addressable (a word = 2 bytes). The size of address bus of processor is atleast 31 bits?

Sol: Maximum Memory = 4 GB = 2^{32} bytes
Size of a word = 2 bytes
Therefore, Number of words = $\frac{2^{32}}{2} = 2^{31}$

So, we required 31 bytes of the address bus of the processor.

Q3: A processor has 40 distinct instruction and 24 general purpose registers. A 32 bit instruction word has an op-code, 2-register operands and an immediate operand. The number of bits available for immediate operand. The number of bits available for immediate operand field is?

Sol. 6 bits are needed for 40 distinct Instruction

5 bits are needed for 24 general purpose registers

32 bits instruction word has an op-code (6 bits); two register operand (total 10 bits) and an immediate operands (x-bits). The number of bits available for, the immediate operand fields

$\Rightarrow x = 32 - (6 + 10)$ bits

$\boxed{x = 16 \text{ bits}}$ Ans.

Q4: The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and write back (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instruction. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles

each and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instruction is ____

Sol: Given total no. of instructions (n) = 100
Number of stages (K) = 5

Since, if 'n' instructions take C cycles, so (C-1) stalls will occur for these instructions.

Therefore, the number of clock cycle required = Total no. of cycle required in general case + extra cycle required in paths.

$= (n+k-1) + \text{Extra cycle}$
$= (100+5-1) + 40*(3-1) + 35*(2-1) + 20*(1-1)$
$= (100+4) + 40*2 + 35*1 + 20*0$
$= 104 + 80 + 35$
$= \boxed{219 \text{ cycles}}$ Ans.