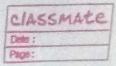
Name	ROHINI SHARMA			Com-801
Subject	t Ad. comp. Arch		Brend	CSE-AI
Semester 8th		ROII NO. 2015/ les/18		
	IN	DE	×	
Sr. No.	Experiment Description	Experiment Date	Submission Date	Remarks / Signature
1.	A non-pipelined		<u> </u>	
	of instructions is?		1	
2	A processor can			
	at least _ bits.			
3.	A processor has 40			
	operand field is?			
4,	The instruction bibelined			
	The instruction pipelined sequence of enstruction is?			



	Page:
Øi:	A Nen-pipeline Single Cycle processor operating at 100 MHz is converted ento a synchronous pipelined processor with 5 stages, requiring 1.5, 2.5 ns 20 Mec. 1.5 ns and 2.5 nsec. respectively the delay of latches is 0.5 nsec. The speed of pipelined processor for a larger no. of instruction?
· Sol:	For non-pipelined System time required = 8.5+1.5+2.0+1.5+2.5 = 10 For pipelined System = Max (Stage delay) + Max (Statch delay) = 2.5+0.5=3.0
	Speed up = time in non-pipelined lystem = 10 time in pipelined system 3 = 3.33 Dry
• <u>da</u> :	A processor can support a memory of 498 where the memory is addressable for word = 2 bytest. The size of address bus of processor is atleast 31 bits?
Asl:	Maximum Memoly = 4GB = 232 bytes Size of a word = 2 bytes Therefore, Number of words = 232 = 231 So, we required 31 bytes of the address bus of the processor.
	of the processor.

CIASSMATE Dele: Page:

A processor has 40 distinct instruction and or general purpose registers. A 32 bit instruction word has an op-code, & registere operands and an immediate operand, The number of bits available for immediate operand The number of bits available for immediate operand field is? al 6 bits are needed for 40 distinct Instruction 5 bits are needed for de general purpose 32 bits einstruction world has an operand (total to bits) and an immediate operands
(n-bits). The number of bits available
for, the immediate operand fields

> 2 32-6+10) bits

[n = 16 bits] Ans. Dy: The instruction pipeline of a RISC processor has The following stages: Instruction Fetch (IF)
Instruction Decode (ID), Operand Fetch (OF),

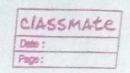
each, 35 instructions take 2 clock cycles

Perform Operation (PO) and write back (WB)

The IF, I'D, OF and WB stages take I clock

eycle each for every instruction, Consider

a sequence of 100 instruction. In the PO stage, 40 instructions take 3 clock cycles



	each and the remaining as inthructions take I clock cycle each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instruction is
100	
fol	men wal no, of institutions (n) = 600
	Given Italal no. of instructions(n) = 600 Number of stoges (K) = 5
	0 0
	Lince, ef 'n' instructions take Caycles, so (C-1) stalls evill occur for these instructions.
	Total no. of cycle required in seneral case
	Therefore, the number of elock cycle required = Total no. of cycle required in general case + extra cycle required cin path.
	= (m+k-1) + Extracycle $= (100+5-1) + 400 + (3-1) + 35 + (3-1) + 200 + (1-1)$
	=(100+5-1)+40+(5-1)+35+(6-1)
	= (100+4) +40+2+35*1+20+0
	= 104 + 80 + 35
	= 104 + 80 + 35 = 219 cycles ons.