UCSB ECE 594BB – Fall 2019

Assignment 3: Verilog Design and Simulation of a Small Neural Network with LIF Neurons

Total Points: 80

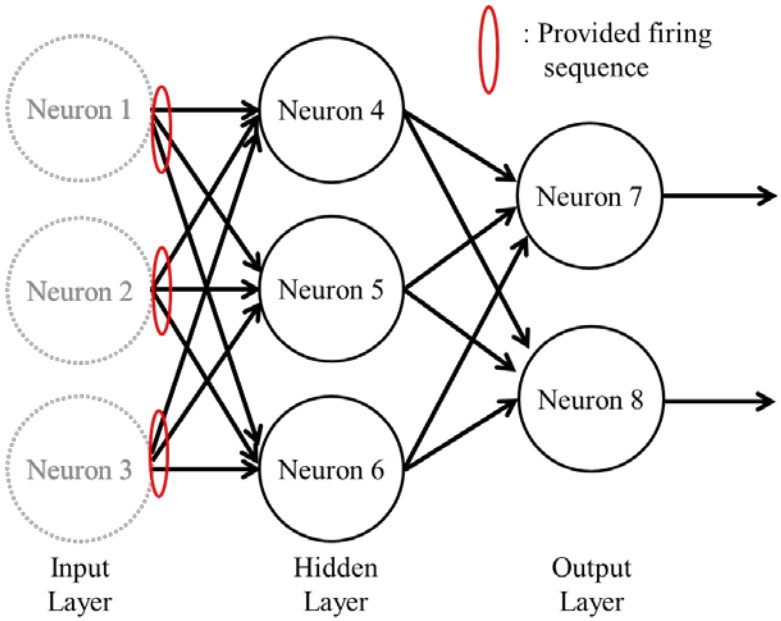
Thursday, November 14

Before the class: softcopy of the report and Verilog code and testbench;
During the class: submit a hardcopy of the report to the Instructor

1. Background

In this assignment, you will build a small neural network using Verilog with the LIF (Leaky Integrated-and-Fire) neurons that you have implemented in previous assignment. Most of the settings are similar to the previous assignment.

Suppose that the network consists of three layers (Input, Hidden, Output) as shown below. The 'input layer' and 'Hidden layer' consists of three neurons. 'Output layer' consists of two neurons. Suppose that the output spikes of the neurons in the 'input layer' is given, which means you will only need to build the 'Hidden layer' and 'Output layer'. (Firing sequence of 'Input layer' neurons will be given later)



You will use the discretized zero-th order synaptic model just like in the previous assignment:

$$V_i[t_k] = V_i[t_{k-1}] + K_{syn} \sum_{j=1}^{M} w_{ji} \cdot S_j[t_{k-1}] - V_{Leak}$$

where V_i is the membrane potential of neuron *i*, *M* is the number of pre-synaptic neurons connected to neuron *i*, K_{syn} is the synaptic weight parameter, w_{ji} is the synaptic weight between neurons *j* and *i* (neuron j is the pre-synaptic neuron connected to neuron *i*), S_j is the indicator function that indicates

whether neuron j fired (S_j will be 1 if neuron j fired and otherwise 0), and V_{Leak} is the leaky parameter.

In this assignment, use the parameters given below:

$V_i[t_0] = V_{rest}$(*resting membrane potential*) = 6, V_{Leak} = 1, K_{syn} = 1, V_θ(*threshold voltage*) = 14.

W_{ji}	Neuron 1	Neuron 2	Neuron 3
Neuron 4	$W_{14} = 3$	$W_{24} = 3$	$W_{34} = 2$
Neuron 5	$W_{15} = 1$	$W_{25} = 2$	$W_{35} = 3$
Neuron 6	$W_{16} = 4$	$W_{26} = 3$	$W_{36} = 4$

W_{ji}	Neuron 4	Neuron 5	Neuron 6
Neuron 7	$W_{47} = 3$	$W_{57} = 2$	$W_{67} = 3$
Neuron 8	$W_{48} = 2$	$W_{58} = 4$	$W_{68} = 2$

(All parameters are normalized and ready-to-use)

**In this assignment, the membrane potential shall not be allowed to go below zero. ($V_i[t_k] \geq 0$)

**If the membrane potential exceeds the threshold voltage at a rising clock edge, it will be immediately set back to the resting membrane potential and produce an output spike. (Don't wait for the next rising clock edge i.e. membrane voltage will change at the same exact rising clock edge while producing an output spike at the same time)

2. The Problem and Credit Breakdown

For the following experiments, set your clock cycle to 10ns (i.e. $t_k - t_{k-1}$ = 10ns = one clock cycle). Each discretized time point occurs at every rising edge of the clock.

For each of the four following sets of provided firing sequences of 'Input layer' neurons, you shall generate the corresponding **waveforms** of :

1) $'V_i[t]'$ of all neurons (neuron 4, 5, 6, 7, and 8)

2) Output spike trains of all neurons.

3) Number of firing of all neurons.

and report the above in your report.

Bit resolutions for some parameters: (You can use less bits if you want)

$V_i[t]$: 5 bits / time-step: 7 bits / firing sequences of Input layer neurons : 40 bits

(1) Firing sequence of Input layer neurons:

The 1st neuron : 00000000001111100000000001111100000000000

The 2nd neuron : 00000111110000000000111110000000000000000

The 3rd neuron : 11111000000000011111000000000011111000000

(2) Firing sequence of Input layer neurons:

The 1st neuron : 11111001111100111110011111001111100011111

The 2nd neuron : 00000110000011000001100000110000011000000

The 3rd neuron : 11111000000000011111000000000011111000000

(3) Firing sequence of Input layer neurons:

The 1st neuron : 00000110000011000001100000110000011000000

The 2nd neuron : 11000000001100000000011000000001100000000

The 3rd neuron : 00000110000011000001100000110000011000000

(4) Firing sequence of Input layer neurons:

The 1st neuron : 10101010101010101010101010101010101010101010

The 2nd neuron : 01010101010101010101010101010101010101010101

The 3rd neuron : 00000110000011000001100000110000011000000

****Firing sequences are starting from the left.**

What to submit:

Report (hardcopy & softcopy): including:

1) The waveform of '$V_i[t]$' of neuron 4, 5, 6, 7 and 8. (All neurons in hidden & output layer)
2) The waveform of output spike trains of all neurons. (output spike trains of neuron 4, 5, 6, 7 and 8)
3) Number of the firing for all neurons.
4) A detailed description of your design

Verilog code and testbench

****For the waveform of '$V_i[t]$', you can just show the value of membrane voltage. This can be**

done by right-click a parameter and set the radix as 'Unsigned Decimal'

Ex) 

Credit Breakdown

- Quality of the report & Verilog code, test bench: 20 points
- Correctness of each simulation: 15 points each; 60 points total

Submission Note

Make a folder and include three contents: 1. report (softcopy) / 2. Verilog file / 3. Testbench file

****Please name the folder as "HW3_yourname".**

Zip your folder and upload it in Google drive (under the folder named HW3).

You shall encrypt your folder so that other students can't see yours.

(You can do this by 1. Right-click the folder >> 2. Click 'Add to archive' >> 3. Set password)

****Please include the password in the hardcopy of your report so that we can access your uploaded files.**