Product Specification

Part Name: OLED Display Module Customer Part ID:

ZJY Part ID: ZJY-6428TSWCG02

Ver: A

Approved by

Customer:

D

Approved by

Notes:

1. Please contact ZHONGJY technology Inc. before agsnsini g your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Limito technology Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

# Revised History

|  |  |  |  |
| --- | --- | --- | --- |
| **Part Number** | **Revision** | **Revision Content** | **Revised on** |
| ZJY-6428TSWCG02 | ANew | 20200929 |  |
|  |  |  |  |
|  |  |  |  |

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# Basic Specifications

### Display Specifications

* + 1. Display Mode: Passive Matrix
    2. Display Color: Monochrome (White)
    3. Drive Duty: 1/128 Duty

### Mechanical Specifications

* + 1. Outline Drawing: According to the annexed outline drawing
    2. Number of Pixels: 64  128

3) Panel Size: 14  28  1.22 (mm)

4) Active Area: 10.86  21.74 (mm)

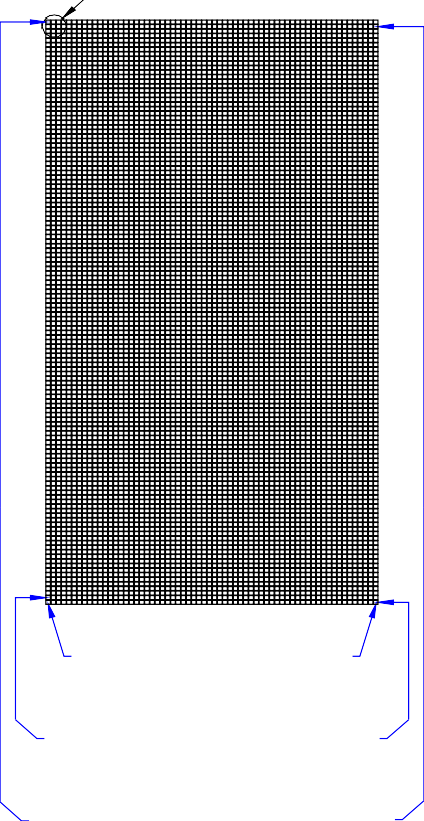
5) Pixel Pitch: 0.17  0.17 (mm)

6) Pixel Size: 0.15  0.15 (mm)

7) Weight: TBD

* 1. **Active Area / Memory Mapping & Pixel Construction**

Detail "A" Scale (10:1)



"A"

C63

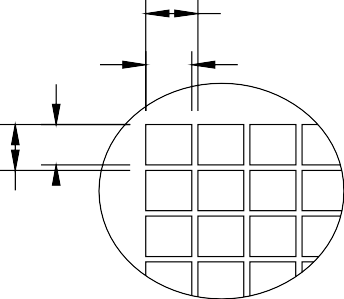
C0

S64

S0

S127

S63



0.17

0.15

0.17

0.15



1

Active Area 0.96"

28±0.2 (Panel Size) 25.2±0.2 (Cap Size)

24.44±0.5 (Polarizer)

22.74 (V/A)

21.74 (A/A)

8

64 x 128 Pixels

"A"

Ver:B

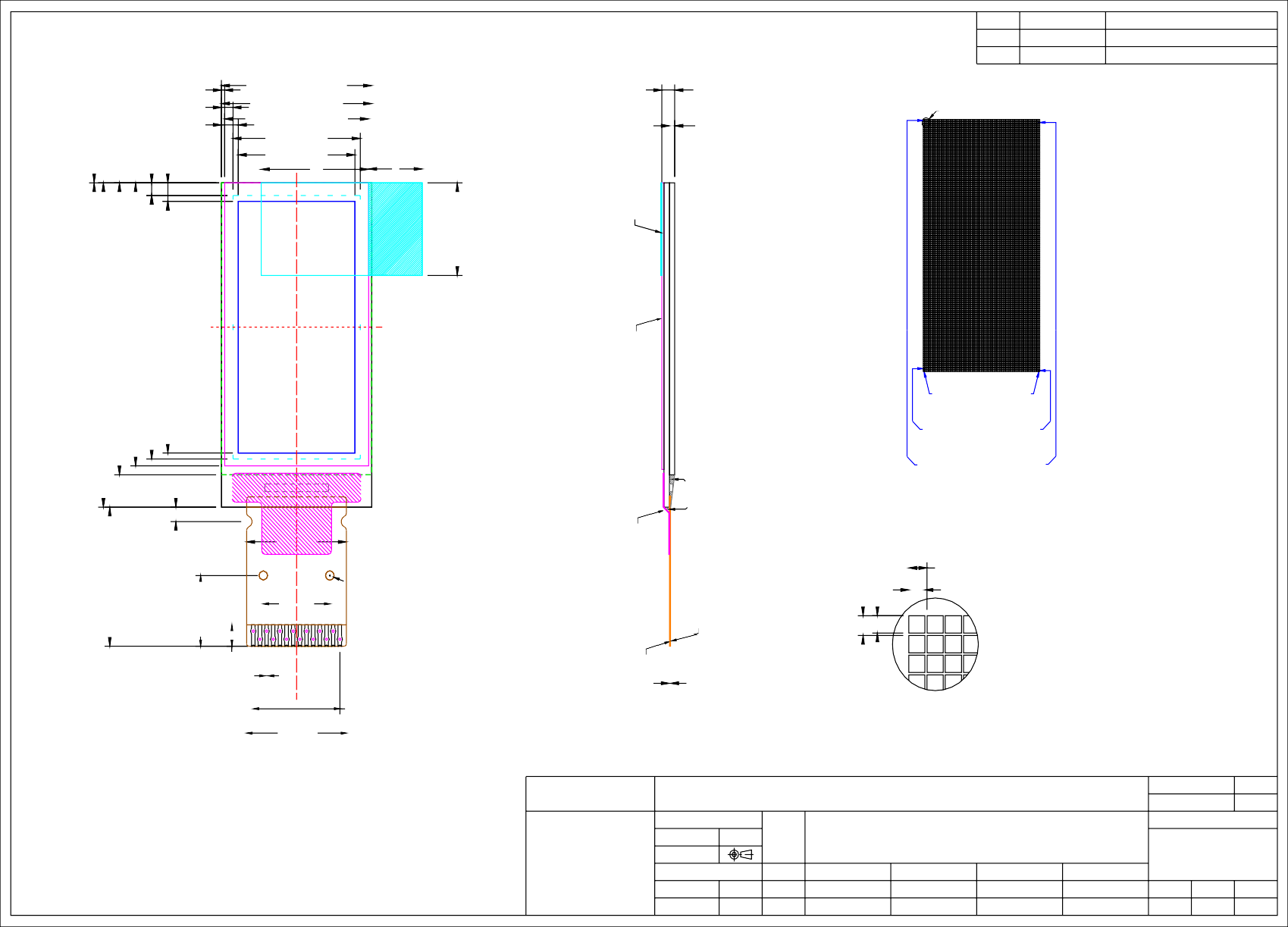
C63 S64

3M #1318B

12x7x0.063mm

Item A

C0 S0



Glue

Contact Side

Date 20200820

0+0.4

-0

(1.1)

(1.6)

Remove Tape t=0.15mm Max

Remark Original Drawing

1 14

**Mechanical Drawing**

12±0.2

1.25

6.1±0.2

1.85±0.2

C2P

C2N

C1P

C1N

VBAT

NC

VSS

VDD

RES#

SCL

SDA

IREF

VCOMH

VC C

Contact Side

S127

Detail "A" Scale (10:1)

0.17

0.15

S63

Notes:

1. Color: White
2. Driver IC: SSD1312

*Customer Approval Signature*

|  |  |
| --- | --- |
| Pin | Symbol |
| 1 | C2P |
| 2 | C2N |
| 3 | C1P |
| 4 | C1N |
| 5 | VBAT |
| 6 | NC |
| 7 | VSS |
| 8 | VDD |
| 9 | RES# |
| 10 | SCL |
| 11 | SDA |
| 12 | IREF |
| 13 | VCOMH |
| 14 | VCC |

Unless Otherwise Specified

ZJY Electronic Technology Co. LTD

ZJY-6428TSWCG02 Folding Type OEL Display Module

Drawing Number QG-6428TSWCG02

Material

Rev. A

1. FPC Number: LT1312P11
2. Interface:

Unit mm

General Roughness

Title

Pixel Number:64 x 128, Monochrome, COG Package

Soda Lime / Polyimide

IIC

**1.4**

Tolerance

Drawn

E.E.

Panel / E.

P.M.

1. General Tolerance: ±0.30

Dimension Angle

±0.3

±1

By Date

HONG 20200820

Scale 1:1

Sheet 1 of 1

Size A3

Polarizer t=0.2mm

2

### 1.5 Pin Definition

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Number** | **Symbol** | **I/O** | **Function** |
| **Power Supply** | | | |
| 8 | VDD | P | **Power Supply for Logic**  This is a voltage supply pin. It must be connected to external source.    **Ground of Logic Circuit**  This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.    **Power Supply for OEL Panel**  This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used. |
|  |  |  |
| 7 | VSS | P |
|  |  |  |
| 14 | VCC | P |
| **Driver** | | | |
| 12 | IREF | I | **Current Reference for Brightness Adjustment**  This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 12.5A maximum.    **Voltage Output High Level for COM Signal**  This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS. |
|  |  |  |
| 13 | VCOMH | O |
| **DC/DC Converter** | | | |
| 5    3 / 4  1 / 2 | VBAT    C1P / C1N C2P / C2N | P    I | **Power Supply for DC/DC Converter Circuit**  This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.    **Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor**  The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used. |
| **Interface** | | | |
| 9 | RES# | I | **Power Reset for Controller and Driver**  This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation. |

**1.5 Pin Definition (Continued)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Number** | **Symbol** | **I/O** | **Function** |
| **Interface (Continued)** | | | |
| 10 | SCL | I | **IIC Bus Clock Signal**  The transmission if information in the I2C bus is following a clock sigmal. Each transmission of data bit is taken place during a single clock period of this pin.    **I2C Bus Data Signal**  This pin acts as a communication channel between the transmitter and the receiver. |
|  |  |  |
| 11 | SDA | I/O |
| **Reserve** | | | |
| 6 | NC | - | NC |

# Absolute Maximum Ratings

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Supply Voltage for Logic | VDD | -0.3 | 4 | V | 1, 2 |
|  |  |  |  |  |  |
| Supply Voltage for Display | VCC | 0 | 11 | V | 1, 2 |
| Supply Voltage for DC/DC  （Internal DC/DC Enable） | Vbat | -0.3 | 4.3 | V | 1, 2 |
| Operating Temperature | TOP | -40 | 70 | C |  |
|  |  |  |  |  |  |
| Storage Temperature | TSTG | -40 | 85 | C | 3 |
|  |  |  |  |  |  |
| Life Time (250 cd/m2) |  | 6,000 | - | hour | 4 |
|  |  |  |  |  |  |
| Life Time (120 cd/m2) |  | 10,000 | - | hour | 4 |
|  |  |  |  |  |  |
| Life Time (80 cd/m2) |  | 30,000 | - | hour | 4 |

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80C.

Note 4: VCC = 9.0V, Ta = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

# Optics & Electrical Characteristics

### Optics Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Characteristics** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Brightness  (VCC Supplied Externally)    Brightness  (VCC Generated by Internal DC/DC)    C.I.E. (White) | Lbr    Lbr    (x)  (y) CR | Note 5  Note 6  C.I.E. 1931 | 200    180    0.23  0.26 | 250    230    0.27  0.30 | -    -    0.31  0.34 | cd/m2    cd/m2 |
| Dark Room Contrast |  | - | 2000:1 | - |  |
|  |  |  |  |  |  |
| Viewing Angle |  | - | Free | - | degree |

* + - Optical measurement taken at VDD = 2.8V, VCC = 9V&3.6v. Software configuration follows Section 4.4 Initialization.

### DC Characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Characteristics** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Supply Voltage for Logic | VDD |  | 1.65 | 2.8 | 3.3 | V |
| Supply Voltage for Display (Supplied Externally) | VCC | Note 5 (Internal DC/DC Disable) | 8.5 | 9 | 9.5 | V |
| Supply Voltage for DC/DC | VBAT | Internal DC/DC Enable | 3.5 | - | 4.2 | V |
| Supply Voltage for Display  (Generated by Internal DC/DC) | VCC | Note 6  (Internal DC/DC Enable) | 8 | 9 | 9.5 | V |
| High Level Input | VIH | IOUT = 100μA, 3.3MHz | 0.8VDD | - | VDD | V |
|  |  |  |  |  |  |  |
| Low Level Input | VIL | IOUT = 100μA, 3.3MHz | 0 | - | 0.2VDD | V |
|  |  |  |  |  |  |  |
| High Level Output | VOH | IOUT = 100μA, 3.3MHz | 0.9VDD | - | VDD | V |
|  |  |  |  |  |  |  |
| Low Level Output | VOL | IOUT = 100μA, 3.3MHz | 0 | - | 0.1VDD | V |
|  |  |  |  |  |  |  |
| Operating Current for VDD | IDD |  | - | 180 | 300 | μA |
|  |  |  |  |  |  |  |
| Operating Current for VCC (VCC Supplied Externally) | ICC | Note 7 | - | 15 | 19.5 | mA |
| Operating Current for VBAT  (VCC Generated by Internal DC/DC) | IBAT | Note 8 | - | 40 | 45 | mA |
| Sleep Mode Current for VDD | IDD, SLEEP |  | - | 1 | 5 | μA |
|  |  |  |  |  |  |  |
| Sleep Mode Current for VCC | ICC, SLEEP |  | - | 2 | 10 | μA |

Note 5 & 6: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer’s request.

Note 7: VDD = 2.8V, VCC = 9V, 100% Display Area Turn on.

Note 8: VDD = 2.8V, VCC = 3.6V, 100% Display Area Turn on.

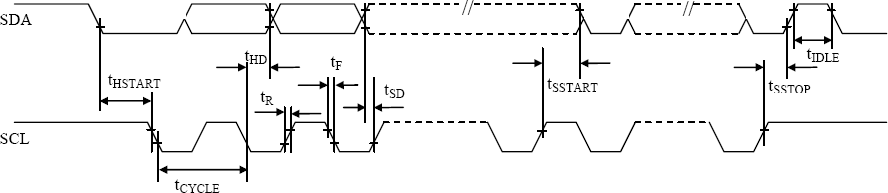
* + - Software configuration follows Section 4.4 Initialization.

### AC Characteristics

3.3. 1 I2C Interface Timing Characteristics:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
| tcycle | Clock Cycle Time | 2.5 | - | μs |
|  |  |  |  |  |
| tHSTART | Start Condition Hold Time | 0.6 | - | μs |
|  |  |  |  |  |
| tHD | Data Hold Time (for “SDAOUT” Pin)    Data Hold Time (for “SDAIN” Pin) | 0    300 | - | ns |
|  |  |  |  |  |
| tSD | Data Setup Time | 100 | - | ns |
| tSSTART | Start Condition Setup Time  (Only relevant for a repeated Start condition) | 0.6 | - | μs |
| tSSTOP | Stop Condition Setup Time | 0.6 | - | μs |
|  |  |  |  |  |
| tR | Rise Time for Data and Clock Pin |  | 300 | ns |
|  |  |  |  |  |
| tF | Fall Time for Data and Clock Pin |  | 300 | ns |
|  |  |  |  |  |
| tIDLE | Idle Time before a New Transmission can Start | 1.3 | - | μs |

\* (VDD - VSS = 1.65V to 3.3V, Ta = 25°C)



### I2C Interface with Internal Charge Pump

特别提醒**(Special Tips):**主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)

C2N

C1N

C6 CAP

R4

C2P

C7 CAP

SCL

C1P

VDD

R5

SDA

VBAT\_IN

R1

Q1

GPIO

Q2

VBAT

VDD

C2P C2N C1P C1N VBAT

R2

C1

C2

IREF VCOMH VCC

VSS VDD RES SCL SDA IREF VCOMH VCC

R3

C3

C4

C5

J?

1

2

3

4

5

6

7

8

9

10

11

12

13

14

CON14

### Recommended Components:

C1,: 0.1μF / 6.3V, X5R

C2: 4.7μF / 6.3V, X5R

C3: 2.2μF/ 16V, X7R

C4: 4.7μF / 16V, X7R

C5: 0.1μF / 16V, X7R C6,C7: 1μF / 16V, X7R

R3: 510KΩ, R3 = (Voltage at IREF - VSS) / IREF R2, R1: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

### Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. VBAT\_in: 3.5~4.2V

### I2C Interface with External VCC

特别提醒**(Special Tips):**主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)

R4

SCL

VDD

R5

SDA

VCC\_IN

R1

Q1

J?

GPIO

Q2

VCC

VDD

R2

C1

C2

IREF

~~VCOMH~~

~~VCC~~

VSS

~~VD~~D

~~RE~~S

~~SCL~~

~~SD~~A

~~IRE~~F

~~VCO~~MH

~~VC~~C

R3

C3

C4

C5

1

2

3

4

5

6

7

8

9

10

11

12

13

14

CON14

### Recommended Components:

C1,: 0.1μF / 6.3V, X5R

C2: 4.7μF / 6.3V, X5R

C3: 2.2μF/ 16V, X7R

C4: 4.7μF / 16V, X7R

C5: 0.1μF / 16V, X7R

R3: 510KΩ, R3 = (Voltage at IREF - VSS) / IREF R2, R1: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

### Notes:

VDD: 1.65~3.5V, it should be equal to MPU I/O voltage. VCC\_in: 8.5~9.5V

# Functional Specification

### Commands

Refer to the Technical Manual for the SSD1312

### Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

* + 1. Power up Sequence:
       1. Power up V

**V**B**DD**B **on**

DD

* + - 1. Send Display off command
      2. Initialization
      3. Clear Screen
      4. Power up VCC/ VBAT
      5. Delay 100ms (When VCC is stable)

VBAT/VCB C

VBDD

**V**B**CC**B**/ V**B**BAT on**

**Display on**

VBSS/B Ground

* + - 1. Send Display on command
    1. Power down Sequence:
       1. Send Display off command
       2. Power down VCC / VBAT
       3. Delay 100ms

(When VCC / VBAT is reach 0 and panel is completely discharges)

* + - 1. Power down VDD

VBCC/VBATTAB VDB D

VBSS/B Ground

**Display off**

**V**B**CC**B **/ VB**B**BAT off**

**VD**B**DD**B **off**

Note 13:

1. Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2. VCC / VBAT should be kept float (disable) when it is OFF.
3. Power Pins (VDD, VCC, VBAT) can never be pulled to ground under any circumstance.
4. VDD should not be power down before VCC / VBAT power down.

### Reset Circuit

When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128´128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line

of the display).

1. Shift register data clear in serial interface
2. Column address counter is set at 0
3. Normal scan direction of the COM outputs
4. Contrast control register is set at 80h
5. Internal DC-DC is selected

### Actual Application Example

Command usage and explanation of an actual example

* + 1. VCC Supplied Externally

**VDD/Vpp off State**

Set Seg Pins Configuration 0xD3, 0x60

Power up VPP & Stabilized (Delay Recommended)

Power up VDD (RES# as Low State)

Set Display Start Line 0xDA, 0x10

Set Display On 0xAF

Power Stabilized (Delay Recommended)

Set Segment Re-Map 0Xa0

(100ms Delay Recommended)

Set RES# as High (3μs Delay Minimum)

Set COM Output Scan Direction 0Xc0

**Display Data Sent**

Initialized State (Parameters as Default)

Set Contrast Control 0x81, 0x5F

Set Display Off 0xAE

Set Pre-Charge Period 0xD9, 0x22

**Clear Screen**

Set Multiplex Ratio 0xA8, 0x3F

Set Entire Display On/Off 0xA4

Set Display Clock Divide Ratio/Oscillator Frequency 0xD5, 0x80

Set VCOMH Deselect Level 0xDB, 0x30

**Initial Settings Configuration**

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

**Normal Operation**

Power down VBCC (100ms Delay Recommended)

**V /V off State**

**DD CC**

Set Display Off 0xAE

Power down VDD

<Entering Sleep Mode>

**Normal Operation**

Power down VCC

Set Display Off 0xAE

**Sleep Mode**

<Exiting Sleep Mode>

**Sleep Mode**

Set Display On 0xAF

**Normal Operation**

Power up VCC & Stabilized (Delay Recommended)

(100ms Delay Recommended)

External setting void ssd1312()

{

RES=1;

delay(1000);

RES=0;

delay(1000);

RES=1;

delay(1000);

write\_i(0xAE); /\*display off\*/

write\_i(0x00); /\*set lower column address\*/ write\_i(0x10); /\*set higher column address\*/

write\_i(0xB0); /\*set page address\*/

write\_i(0x81); /\*contract control\*/ write\_i(0x5f); /\*128\*/

write\_i(0x20); /\* Set Memory addressing mode (0x20/0x21) \*/ write\_i(0x02); /\* 0X09（90 度） \*/

write\_i(0xA0); /\*set segment remap 0XA1 \*/ write\_i(0xC8); /\*Com scan direction 0Xc0 \*/

write\_i(0xA4); /\*Disable Entire Display On (0xA4/0xA5)\*/

write\_i(0xA6); /\* 0XA7 normal / reverse \*/

write\_i(0xA8); /\* multiplex ratio \*/ write\_i(0x3F); /\*duty = 1/64\*/

write\_i(0xD3); /\*set display offset\*/ write\_i(0x00); /\* 0x20 \*/

write\_i(0xD5); /\*set osc division\*/ write\_i(0x80);

write\_i(0xD9); /\*set pre-charge period\*/ write\_i(0x22);

write\_i(0xDA); /\* Set SEG Pins Hardware Configuration \*/ write\_i(0x10);

write\_i(0xdb); /\*set vcomh\*/ write\_i(0x30);

write\_i(0x8d); /\*set charge pump enable\*/ write\_i(0x10); /\*Set DC-DC disable \*/

clear(); /\* Clear Screen \*/

write\_i(0xAF); /\*display ON\*/

}

void write\_w(unsigned char dat)

{

unsigned char m,da; unsigned char j; da=dat; for(j=0;j<8;j++)

{

m=da; SCL=0;

m=m&0x80; if(m==0x80)

{

}

else

{

}

SDA=1;

SDA=0;

delay(1); da=da<<1; SCL=1;

}

SCL=0; SCL=1;

}

void write\_i(unsigned char ins)

{

start(); write\_w(0x78); write\_w(0x00); write\_w(ins); stop();

}

void write\_d(unsigned char dat)

{

start(); write\_w(0x78); write\_w(0x40); write\_w(dat); stop();

}

void start()

{

SCL=1; SDA=1;

delay(1); SDA=0; SCL=0;

}

void stop()

{

SCL=0; SDA=0;

delay(1); SDA=1; SCL=1;

}

void delay(unsigned int i)

{

while(i>0)

{

i--;

}

}

void clear()

{

unsigned char x,y; unsigned int j=0; write\_i(0x00);

write\_i(0x10); /\*set higher column address\*/

for(y=0;y<16;y++)

{

write\_i(0xB0+y); /\*set page address\*/ write\_i(0x00);

write\_i(0x10); for(x=0;x<64;x++)

{

write\_d(0x00); write\_d(0x00);

}

}

}

* + 1. VCC Generated by Internal DC/DC Circuit

<Power up Sequence>

**VDD/VCC off State**

Set Display Offset 0xD3, 0x00

Set Entire Display On/Off 0xA4

Power up VDD (RES# as Low State)

Set Display Start Line 0x00

**Clear Screen**

Power Stabilized (Delay Recommended)

Set Charge Pump 0x8D, 0x72

Power up VCC & Stabilized (Delay Recommended)

Set RES# as High (3μs Delay Minimum)

Set Segment Re-Map 0Xa0

Set Display On 0xAF

Initialized State (Parameters as Default)

Set COM Output Scan Direction 0xC8

(100ms Delay Recommended)

Set Display Off 0xAE

Set COM Pins Hardware Configuration 0xDA, 0x10

**Display Data Sent**

Set VCOMH Deselect Level 0xDB, 0x30

Set Multiplex Ratio 0xA8, 0x3F

Set Pre-Charge Period 0xD9, 0x22

Set Display Clock Divide Ratio/Oscillator Frequency 0xD5, 0x80

Set Contrast Control 0x81, 0x5F

**Initial Settings Configuration**

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

**Normal Operation**

Power Stabilized

(100ms Delay Recommend

ed)

**VDD/VBAT off State**

Set Display Off 0xAE

Power down VBBAT (50ms Delay Recommended)

Power down VDD

Set Charge Pump 0x8D, 0x10

<Entering Sleep Mode>

**Normal Operation**

Set Charge Pump 0x8D, 0x10

**Sleep Mode**

Set Display Off 0xAE

Power down VBAT

<Exiting Sleep Mode>

**Sleep Mode**

Set Charge Pump 0x8D, 0x72

Power up VBAT

(100ms Delay Recommended)

**Normal Operation**

Set Display On 0xAF

Power Stabilized (100ms Delay Recommended)

Internal setting（Charge pump） void SSD1312()

{

RES=1;

delay(1000);

RES=0;

delay(1000);

RES=1;

delay(1000);

write\_i(0xAE); /\*display off\*/

write\_i(0x00); /\*set lower column address\*/ write\_i(0x10); /\*set higher column address\*/

write\_i(0xB0); /\*set page address\*/

write\_i(0x81); /\*contract control\*/ write\_i(0x5f); /\*128\*/

write\_i(0x20); /\* Set Memory addressing mode (0x20/0x21) \*/ write\_i(0x02); /\* 0x09 \*/

write\_i(0xA0); /\*set segment remap 0XA1 \*/ write\_i(0xC8); /\*Com scan direction 0Xc8 \*/ write\_i(0xA4); /\*Disable Entire Display On (0xA4/0xA5)\*/ write\_i(0xA6); /\*normal / reverse\*/

write\_i(0xA8); /\*multiplex ratio\*/ write\_i(0x3F); /\*duty = 1/64\*/

write\_i(0xD3); /\*set display offset\*/ write\_i(0x00); /\* 0x20 \*/

write\_i(0xD5); /\*set osc division\*/ write\_i(0x80);

write\_i(0xD9); /\*set pre-charge period\*/ write\_i(0x22);

write\_i(0xDA); /\* Set SEG Pins Hardware Configuration \*/ write\_i(0x10);

write\_i(0xdb); /\*set vcomh\*/ write\_i(0x30);

write\_i(0x8d); /\*set charge pump enable\*/

write\_i(0x72); /\* 0x12:7.5V; 0x52:8V; 0x72:9V; 0x92:10V \*/ clear(); /\* Clear Screen \*/

write\_i(0xAF); /\*display ON\*/

}

void write\_w(unsigned char dat)

{

unsigned char m,da; unsigned char j; da=dat; for(j=0;j<8;j++)

{

m=da; SCL=0;

m=m&0x80; if(m==0x80)

{

}

else

{

}

SDA=1;

SDA=0;

delay(1); da=da<<1; SCL=1;

}

SCL=0; SCL=1;

}

void write\_i(unsigned char ins)

{

start(); write\_w(0x78); write\_w(0x00); write\_w(ins); stop();

}

void write\_d(unsigned char dat)

{

start(); write\_w(0x78); write\_w(0x40); write\_w(dat); stop();

}

void start()

{

SCL=1; SDA=1;

delay(1); SDA=0; SCL=0;

}

void stop()

{

SCL=0; SDA=0;

delay(1); SDA=1; SCL=1;

}

void delay(unsigned int i)

{

while(i>0)

{

i--;

}

}

void clear()

{

unsigned char x,y; unsigned int j=0; write\_i(0x00);

write\_i(0x10); /\*set higher column address\*/

for(y=0;y<16;y++)

{

write\_i(0xB0+y); /\*set page address\*/ write\_i(0x00);

write\_i(0x10); for(x=0;x<64;x++)

{

write\_d(0x00); write\_d(0x00);

}

}

}

# Reliability

### Contents of Reliability Tests

|  |  |  |
| --- | --- | --- |
| **Item** | **Conditions** | **Criteria** |
| High Temperature Operation | 70C, 240 hrs |  |
|  |  |  |
| Low Temperature Operation | -40C, 240 hrs |  |
|  |  |  |
| High Temperature Storage    Low Temperature Storage | 85C, 240 hrs    -40C, 240 hrs | The operational functions work. |
|  |  |  |
| High Temperature/Humidity Operation | 60C, 90% RH, 120 hrs |  |
| Thermal Shock | -40C  85C, 24 cycles 60 mins dwell |  |

* + - The samples used for the above tests do not include polarizer.

Please note that the reliability test project requires the use of virgin samples

* + - No moisture condensation is observed during tests.

### Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 235C; 5515% RH.

# Outgoing Quality Control Specifications



### Environment Required

Customer’s test & measurement are required to be conducted under the following conditions: Temperature: 23  5C

Humidity: 55  15% RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥ 50cm Distance between the Panel & Eyes of the Inspector: ≥ 30cm Finger glove (or finger cover) must be worn by the inspector. Inspection table or jig must be anti-electrostatic.

### Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

### Criteria & Acceptable Quality Level

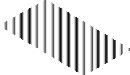
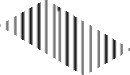
|  |  |  |
| --- | --- | --- |
| **Partition** | **AQL** | **Definition** |
| Major | 0.65 | Defects in Pattern Check (Display On) |
|  |  |  |
| Minor | 1.0 | Defects in Cosmetic Check (Display Off) |

6.3.1 Cosmetic Check (Display Off) in Non-Active Area



|  |  |  |
| --- | --- | --- |
| **Check Item** | **Classification** | **Criteria** |
| Panel General Chipping | Minor | X > 6 mm (Along with Edge)  Y > 1 mm (Perpendicular to edge)  X    Y  X  Y |

* + 1. Cosmetic Check (Display Off) in Non-Active Area (Continued)



|  |  |  |
| --- | --- | --- |
| **Check Item** | **Classification** | **Criteria** |
|  |  | Any crack is not allowable. |
|  |  |  |
| Panel Crack | Minor |  |
| Copper Exposed (Even Pin or Film) | Minor | Not Allowable by Naked Eye Inspection |
| Film or Trace Damage | Minor |  |
|  |  |  |
| Terminal Lead Prober Mark | Acceptable |  |
|  |  |  |
| Glue or Contamination on Pin (Couldn’t Be Removed by Alcohol) | Minor |  |
| Ink Marking on Back Side of panel (Exclude on Film) | Acceptable | Ignore for Any |

* + 1. Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

|  |  |  |
| --- | --- | --- |
| **Check Item** | **Classification** | **Criteria** |
| Any Dirt & Scratch on Polarizer’s Protective Film | Acceptable | Ignore for not Affect the Polarizer W ≤ 0.1 Ignore  W > 0.1  L ≤ 2 n ≤ 1  L > 2 n = 0    Φ ≤ 0.1 Ignore  0.1 < Φ ≤ 0.25 n ≤ 1  0.25 < Φ n = 0  Φ ≤ 0.5   Ignore if no Influence on Display  0.5 < Φ n = 0    Not Allowable |
| Scratches, Fiber, Line-Shape Defect (On Polarizer) | Minor |
|  |  |
| Dirt, Black Spot, Foreign Material, (On Polarizer) | Minor |
|  |  |
| Dent, Bubbles, White spot (Any Transparent Spot on Polarizer) | Minor |
| Fingerprint, Flow Mark (On Polarizer) | Minor |

\* Protective film should not be tear off when cosmetic check.

\*\* Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2

b: Minor Axis



L

W

a: Major Axis

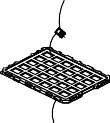
* + 1. Pattern Check (Display On) in Active Area

|  |  |  |
| --- | --- | --- |
| **Check Item** | **Classification** | **Criteria** |
| No Display  Missing Line    Pixel Short  Darker Pixel  Wrong Display  Un-uniform | Major    Major  Major  Major  Major  Major |  |

# Package Specifications

x 1 pcs (Empty)

EPE COVER FOAM 351x212x1, ANTISTATIC x 1 Pcs

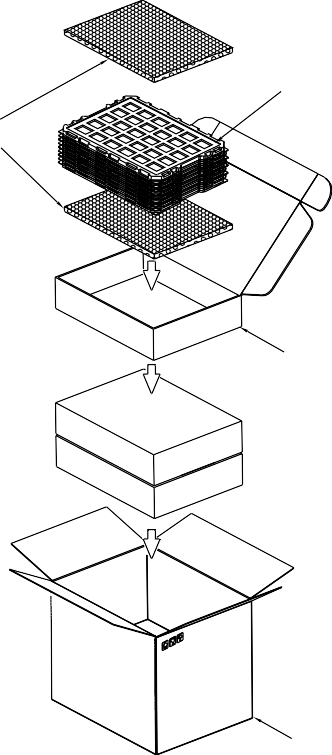


Module

Tray 420x285mm

B Pcs Tray Vacuum packing

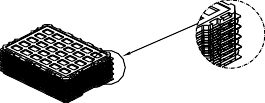
16



EPE PROTECTTIVE

15

T=0.8mm



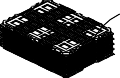
x A pcs Staggered Stacking

Primary Box C SET

Exsiccator x 2 pcs

16

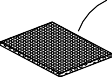
Brimary Box 4 SET



Wrapped with adhesive tape x B pcs

Vacuum packing bag

EPE PROTECTTIVE

370mm x 280mm x 20mm

CARTON BOX

Label

Univision Technology Inc. Part ID :

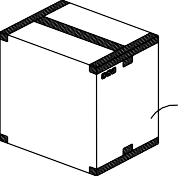
Lot ID :

Q'ty : QC :

Primary L450mm x W296 x H110, B wave x C4Pcs



Label

Carton Box L464mm x W313mm x H472mm, AB wave

(Major / Maximum)

|  |  |
| --- | --- |
| Item | Quantity |
| **Module**    **Holding Trays (A)**    **Total Trays (B)**    **Primary Box (C)** | **840 per Primary Box**     1. **per Primary Box**      1. **per Primary Box (Including 1 Empty Tray) 1~4 per Carton (4 as Major / Maximum)** |

# Precautions When Using These OEL Display Modules

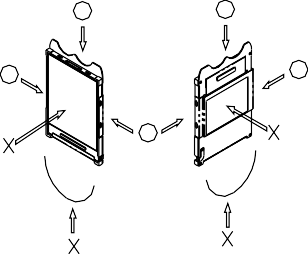
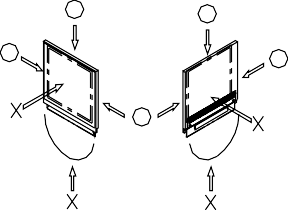
### Handling Precautions

1. Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2. If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3. If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4. The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5. When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

Also, pay attention that the following liquid and solvent may spoil the polarizer:

* + Water
  + Ketone
  + Aromatic Solvents

1. Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



1. Do not apply stress to the driver IC and the surrounding molded sections.
2. Do not disassemble nor modify the OEL display module.
3. Do not apply input signals while the logic power is off.
4. Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
   * Be sure to make human body grounding when handling OEL display modules.
   * Be sure to ground tools to use or assembly such as soldering irons.
   * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
   * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
5. Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
6. If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

### Storage Precautions

1. When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Limito technology Inc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2. If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

### Designing Precautions

1. The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2. To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3. We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4. Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5. As for EMI, take necessary measures on the equipment side basically.
6. When fastening the OEL display module, fasten the external plastic housing section.
7. If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8. The electric potential to be connected to the rear face of the IC chip should be as follows: SH1106

\* Connection (contact) to any other potential than the above may lead to rupture of the IC.

### Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

### Other Precautions

1. When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

1. To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
2. With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
3. Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may

be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

1. We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

**Warranty:**

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. Limito technology Inc. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

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