

SmartMedia™ 128MByte Product Manual



CORPORATE HEADQUARTERS

140 Caspian Court
Sunnyvale, CA 94089
408-542-0500

FAX: 408-542-0503

URL: <http://www.sandisk.com>

SanDisk® Corporation general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury. Per SanDisk Terms and Conditions of Sale, the user of SanDisk products in life support applications assumes all risk of such use and indemnifies SanDisk against all damages.

The information in this manual is subject to change without notice.

SanDisk Corporation shall not be liable for technical or editorial errors or omissions contained herein; nor for incidental or consequential damages resulting from the furnishing, performance, or use of this material.

All parts of the SanDisk documentation are protected by copyright law and all rights are reserved. This documentation may not, in whole or in part, be copied, photocopied, reproduced, translated, or reduced to any electronic medium or machine readable form without prior consent, in writing, from SanDisk Corporation.

SanDisk and the SanDisk logo are registered trademarks of SanDisk Corporation. SmartMedia is a trademark of Toshiba Corporation.

Product names mentioned herein are for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

© 2001 SanDisk Corporation. All rights reserved.

SanDisk products are covered or licensed under one or more of the following U.S. Patent Nos. 5,070,032; 5,095,344; 5,168,465; 5,172,338; 5,198,380; 5,200,959; 5,268,318; 5,268,870; 5,272,669; 5,418,752; 5,602,987. Other U.S. and foreign patents awarded and pending.

Lit. No. 80-36-00174 Rev. 1.2 8/01

Printed in U.S.A.

Revision History

- *Revision 1 – initial release.*
- *Revision 1.1 – several minor edits throughout document.*
- *Revision 1.2 – several minor edits throughout document.*

Table of Contents

1.0	Description.....	5
1.1	Features.....	5
2.0	Timing Diagrams	11
3.0	Pin Functions	26
3.1	Pin Descriptions	26
3.2	Schematic Cell Layout and Address Assignment	27
3.3	Operation Mode: Logic and Command Tables	28
4.0	Device Operation	30
4.1	Read Mode (1)	30
4.2	Read Mode (2)	31
4.3	Read Mode (3)	32
4.4	Sequential Read (1) (2) (3).....	32
4.5	Status Read	33
4.6	Auto Page Program	34
4.7	Auto Block Erase.....	35
4.8	Multi Block Program	36
4.8.1	Internal Addressing in Relation with the Districts	37
4.8.2	Address Input Restriction for the Multi Block Program Operation.....	38
4.8.3	Operating Restriction During the Multi Block Program Operation.....	38
4.9	Status Read Operation	38
4.10	Multi District Block Erase.....	39
4.10.1	Internal Addressing in Relation with the Districts.....	39
4.10.2	Address Input Restriction for the Multi District Block Erase Operation	40
4.11	Reset.....	40
4.12	ID Read.....	42
5.0	Application Notes and Comments	43
5.1	Prohibition of Unspecified Commands	43
5.2	Restriction of Commands While in Busy State	43
5.3	Pointer Control for 00H, 01H and 50H	43
5.4	Acceptable Commands After Serial Input Command 80H	44
5.5	Status Read During a Read Operation.....	45
5.6	Auto-Programming Failure.....	45
5.7	Addressing for Program Operation	45
5.8	R/B : Termination for the Ready/Busy Pin (R/B).....	46
5.9	Status After Power-on.....	46
5.10	Power-on/off Sequence.....	46
5.11	Note Regarding the WP Signal	47
5.12	When Five Address Cycles are Input.....	48
5.13	Several Programming Cycles on the Same Page (Partial Page Program).....	49
5.14	Note Regarding the RE Signal.....	49
5.15	Invalid Blocks (Bad Blocks)	50
5.16	Failure Phenomena for Program and Erase Operations.....	52
5.17	Chattering of Connector	52

Table of Contents (continued)

6.0	Handling Precautions.....	53
7.0	Package Dimensions.....	54
7.1	SmartMedia Card Dimensions.....	54
	Ordering Information and Technical Support.....	55
	Ordering Information.....	57
	SmartMedia Card	57
	Technical Support Services.....	58
	Direct SanDisk Technical Support	58
	SanDisk Worldwide Web Site.....	58
	SanDisk Sales Offices.....	59
	Limited Warranty.....	63

1.0 Description

The SanDisk SmartMedia Card is a 3.3-V 1-Gbit (1,107,296,256) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) device, organized as 528 bytes X 32 pages X 8192 blocks. This device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes X 32 pages).

The SanDisk SmartMedia Card is a serial-type memory device which uses the I/O pins for both address and data input and output as well as for command inputs. The Erase and Program operations are automatically executed making the device ideal for applications such as solid-state file storage, voice recording, image storage for digital cameras and other systems which require high-density non-volatile memory data storage.

1.1 Features

- Organization
 - Memory cell array 528 × 128K × 8 × 2
 - Data Register 528 × 8
 - Page size 528 bytes
 - Block size (16K + 512) bytes
- Modes
 - Read, Reset, Auto Page Program
 - Auto Block Erase, Status Read
 - Multi Block Program, Multi Block Erase
- Mode Control
 - Serial Input/Output
 - Command control
- Complies with the SmartMedia™ Electrical Specification and Data Format Specification issued by SSFDC Forum (SmartMedia Card).
- Power Supply – V_{CC} = 2.7 V to 3.6 V
- Program/Erase Cycles – 1E5 cycles (with ECC)
- Access time
 - Cell array to register 25 μs max
 - Serial Read Cycle 50 ns min
- Operating current
 - Read (50 ns cycle) 10 mA typ.
 - Program (avg.) 10 mA typ.
 - Erase (avg.) 10 mA typ.
 - Standby 100 μA max
- Package
 - SDSM-128-101-01: SmartMedia Card (Weight: 1.8g typical)

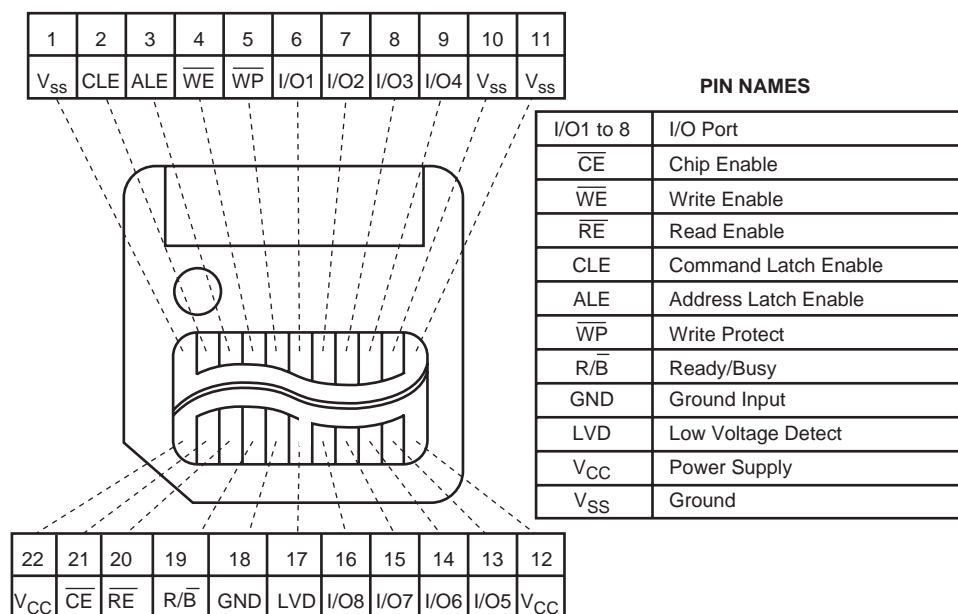


Figure 1-1 1024 Mbit SmartMedia Card Pin Assignments (Top View)

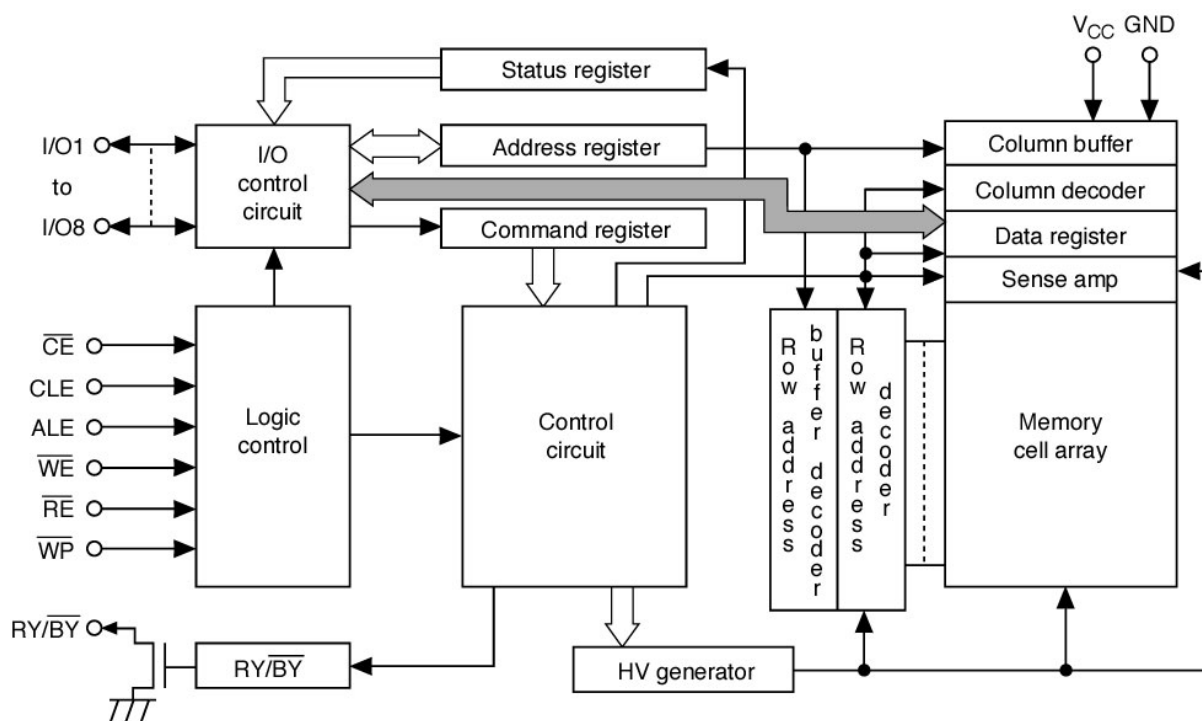


Figure 1-2 Block Diagram

Table 1-1 Absolute Maximum Ratings

Symbol	Item	Value	Unit
V _{CC}	Power Supply Voltage	-0.6 to 4.6	V
V _{IN}	Input Voltage	-0.6 to 4.6	V
V _{I/O}	Input /Output Voltage	-0.6 V to V _{CC} + 0.3 V (≤4.6 V)	V
P _D	Power Dissipation	0.3	W
T _{STG}	Storage Temperature	-20 to 65	°C
T _{OPR}	Operating Temperature	0 to 55	°C

Table 1-2 Capacitance *(Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Condition	Min.	Max.	Unit
C _{IN}	Input	V _{IN} = 0 V	—	20	pF
C _{OUT}	Output	V _{OUT} = 0 V	—	20	pF

* This parameter is periodically sampled and is not tested for every device.

Table 1-3 Valid Blocks ⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
N _{VB}	Number of Valid Blocks	8032 ⁽²⁾	-	8192	Blocks

Notes: (1) The SmartMedia Card occasionally contains unusable blocks. Refer to section 5.15 toward the end of this document.

(2) SSFDC Forum Spec. : 1002 MIN per Zone (each 16 k Bytes).

Table 1-4 Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Power Supply Voltage	2.7	3.3	3.6	V
V _{IH}	High Level Input Voltage	2.0	—	V _{CC} + 0.3	V
V _{IL}	Low Level Input Voltage	-0.3*	—	0.8	V

* -2 V (pulse width ≤ 20 ns)

Table 1-5 DC Characteristics**(Ta = 0 to 70° C, V_{CC} = 2.7 V to 3.6 V)**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{CC}	—	—	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4 V to V _{CC}	—	—	±10	μA
I _{CCO1}	Operating Current (Serial Read)	$\overline{CE} = V_{IL}$, I _{OUT} = 0 mA, t _{cycle} = 50 ns	—	10	30	mA
I _{CCO3}	Operating Current (Command Input)	t _{cycle} = 50 ns	—	10	30	mA
I _{CCO4}	Operating Current (Data Input)	t _{cycle} = 50 ns	—	10	30	mA
I _{CCO5}	Operating Current (Address Input)	t _{cycle} = 50 ns	—	10	30	mA
I _{CCO7}	Programming Current	—	—	10	30	mA
I _{CCO8}	Erasing Current	—	—	10	30	mA
I _{CCS1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	1	mA
I _{CCS2}	Standby Current	$\overline{CE} = V_{CC} - 0.2 \text{ V}$	—	—	100	μA
V _{OH}	High Level Output Voltage	I _{OH} = -400 μA	2.4	—	—	V
V _{OL}	Low Level Output Voltage	I _{OL} = 2.1 mA	—	—	0.4	V
I _{OL} (R/ \overline{B})	Output current of R/ \overline{B} pin	V _{OL} = 0.4 V	—	8	—	mA

Table 1-6 AC Characteristics and Recommended Operating Conditions**(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)**

Symbol	Parameter	Min.	Max.	Unit	Notes
t _{CLS}	CLE Setup Time	0	—	ns	
t _{CLH}	CLE Hold Time	10	—	ns	
t _{CS}	$\overline{\text{CE}}$ Setup Time	0	—	ns	
t _{CH}	$\overline{\text{CE}}$ Hold Time	10	—	ns	
t _{WP}	Write Pulse Width	25	—	ns	
t _{ALS}	ALE Setup Time	0	—	ns	
t _{ALH}	ALE Hold Time	10	—	ns	
t _{DS}	Data Setup Time	20	—	ns	
t _{DH}	Data Hold Time	10	—	ns	
t _{WC}	Write Cycle Time	50	—	ns	
t _{WH}	$\overline{\text{WE}}$ High Hold Time	15	—	ns	
t _{WW}	$\overline{\text{WP}}$ High to $\overline{\text{WE}}$ Low	100	—	ns	
t _{RR}	Ready to $\overline{\text{RE}}$ Falling Edge	20	—	ns	
t _{RP}	Read Pulse Width	35	—	ns	
t _{RC}	Read Cycle Time	50	—	ns	
t _{REA}	$\overline{\text{RE}}$ Access Time (Serial Data Access)	—	35	ns	
t _{CEH}	$\overline{\text{CE}}$ High Time for Last Address in Serial Read Cycle	100	—	ns	(1)
t _{READID}	$\overline{\text{RE}}$ Access Time (ID Read)	—	35	ns	
t _{OH}	Data Output Hold Time	10	—	ns	
t _{RHZ}	$\overline{\text{RE}}$ High to Output High Impedance	—	30	ns	
t _{CHZ}	$\overline{\text{CE}}$ High to Output High Impedance	—	20	ns	
t _{REH}	$\overline{\text{RE}}$ High Hold Time	15	—	ns	
t _{IR}	Output High Impedance to $\overline{\text{RE}}$ Rising Edge	0	—	ns	
t _{RSTO}	$\overline{\text{RE}}$ Access Time (Status Read)	—	35	ns	
t _{CSTO}	$\overline{\text{CE}}$ Access Time (Status Read)	—	45	ns	
t _{RHW}	$\overline{\text{RE}}$ High to $\overline{\text{WE}}$ Low	0	—	ns	
t _{WHC}	$\overline{\text{WE}}$ High to $\overline{\text{CE}}$ Low	30	—	ns	
t _{WHR}	$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	30	—	ns	
t _{AR1}	ALE Low to $\overline{\text{RE}}$ Low (ID Read)	100	—	ns	
t _{CR}	$\overline{\text{CE}}$ Low to $\overline{\text{RE}}$ Low (ID Read)	100	—	ns	
t _R	Memory Cell Array to Starting Address	—	25	μs	
t _{WB}	$\overline{\text{WE}}$ High to Busy	—	200	ns	
t _{AR2}	ALE Low to $\overline{\text{RE}}$ Low (Read Cycle)	50	—	ns	
t _{RB}	$\overline{\text{RE}}$ Last Clock Rising Edge to Busy (in Sequential Read)	—	200	ns	
t _{CRY}	$\overline{\text{CE}}$ High to Ready (When interrupted by $\overline{\text{CE}}$ in Read Mode)	—	$1 + t_r(\text{R}/\overline{\text{B}})$	μs	(2)
t _{RST}	Device Reset Time (Read/Program/Erase)	—	6/10/500	μs	

Note: (1) Sequential Read is terminated when t_{CEH} is greater than or equal to 100 ns. If the $\overline{\text{RE}}$ to $\overline{\text{CE}}$ delay is less than 30ns, R/ $\overline{\text{B}}$ signal stays Ready.

(2) $\overline{\text{CE}}$ High to Ready time depends on the pull-up resistor tied to the R/ $\overline{\text{B}}$ pin. (Refer to section 5.8.)

Table 1-7 AC Test Conditions

Parameter	Conditions
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C _L (100 pF) + 1 TTL

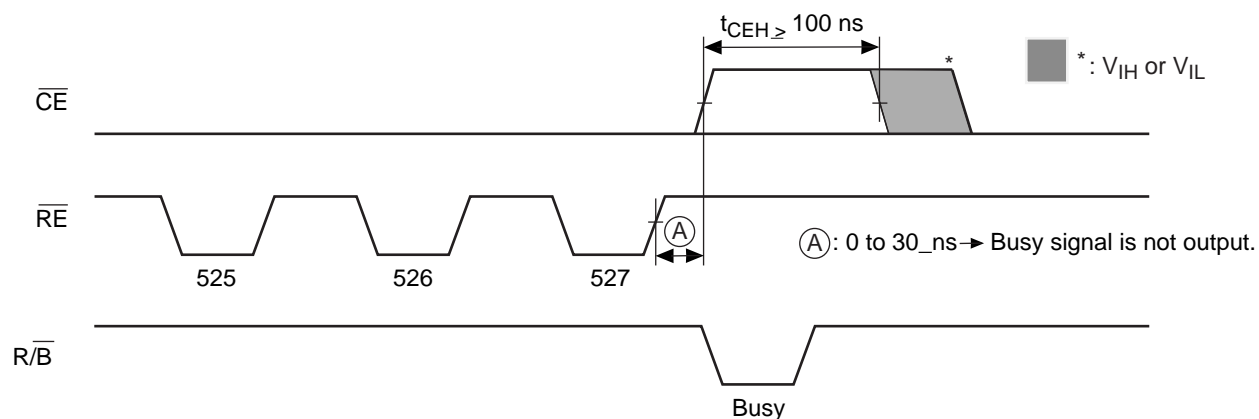


Figure 1-3

Table 1-8 Programming and Erasing Characteristics

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t _{PROG}	Average Programming Time	—	200	1000	μs	
t _{DBSY}	Dummy Busy Time for Multi Block Programming	—	2	10	μs	
t _{MBPSY}	Multi Block Program Busy Time	—	200	1000	μs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t _{BERASE}	Block Erasing Time	—	2	10	ms	

Notes: (1) Refer to section 5.13.

2.0 Timing Diagrams

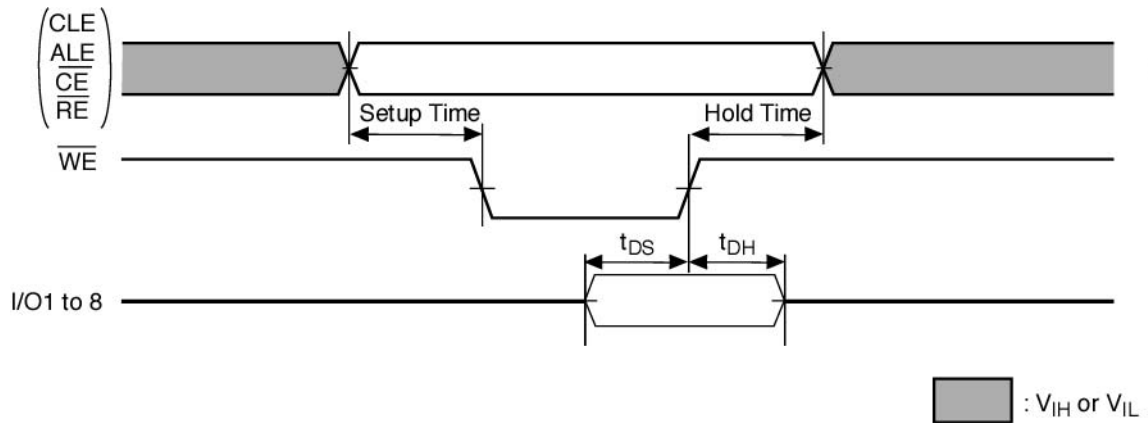


Figure 2-1 Latch Timing Diagram for Command/Address/Data

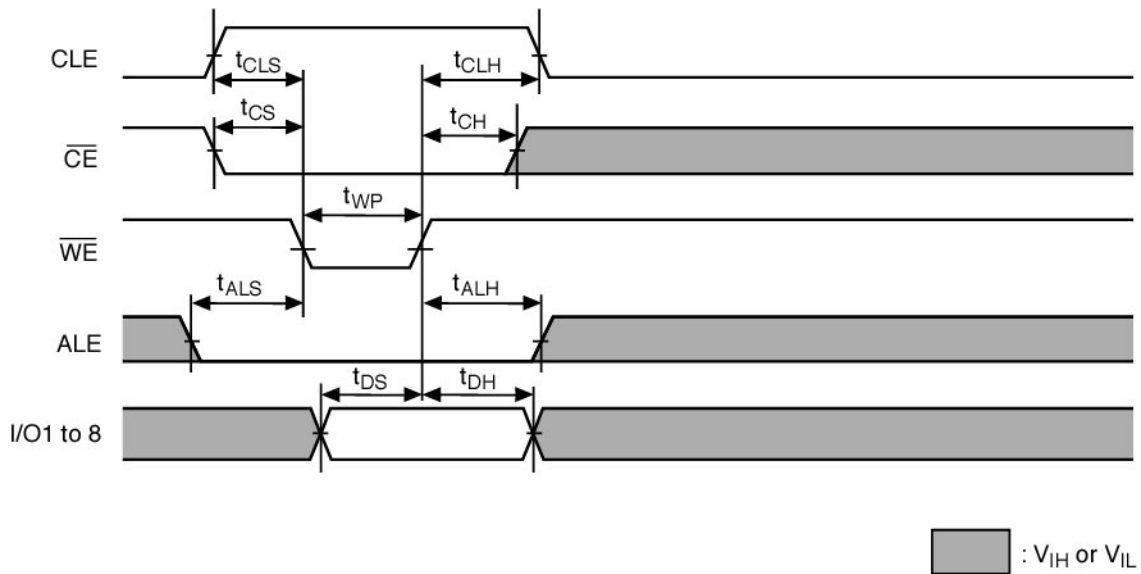


Figure 2-2 Command Input Cycle Timing Diagram

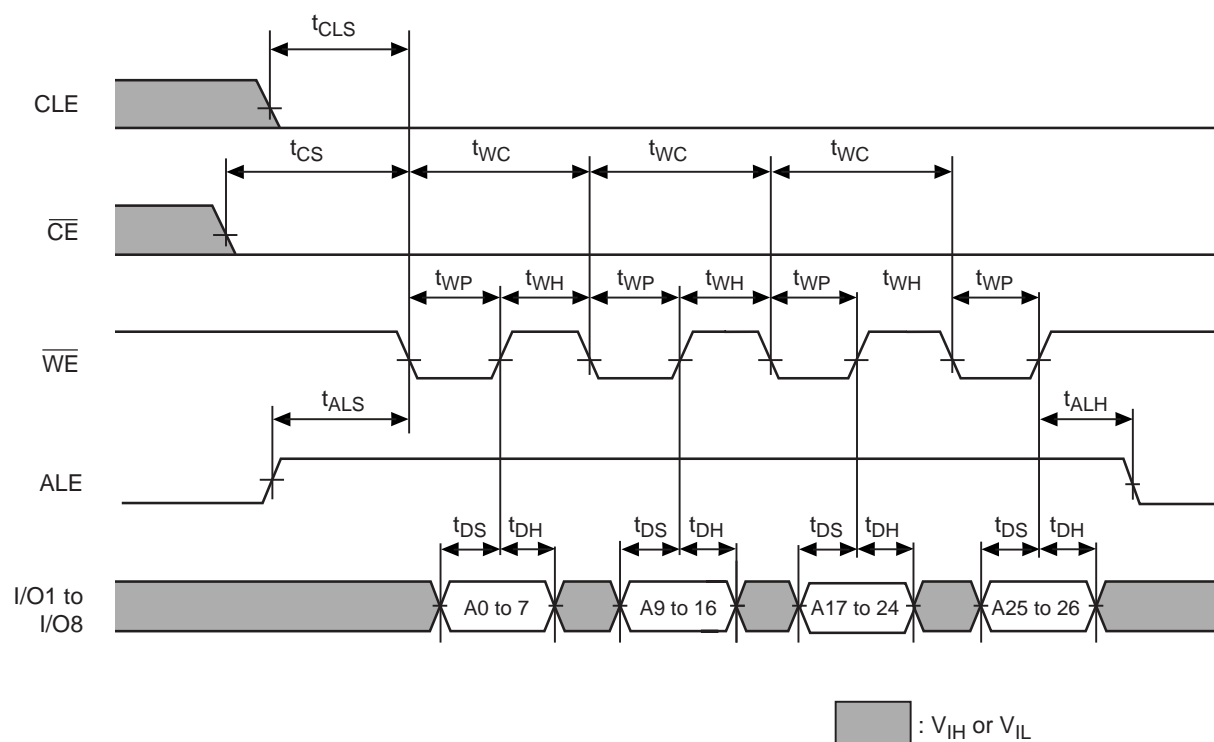


Figure 2-3 Address Input Cycle Timing Diagram

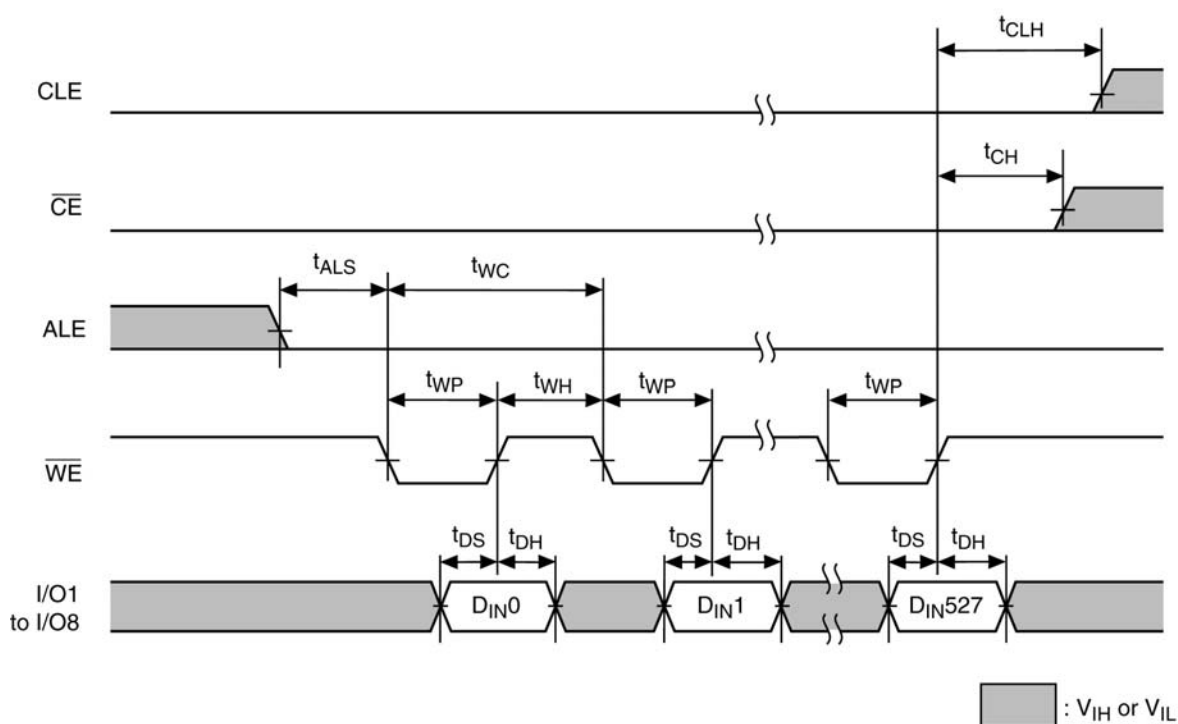


Figure 2-4 Data Input Cycle Timing Diagram

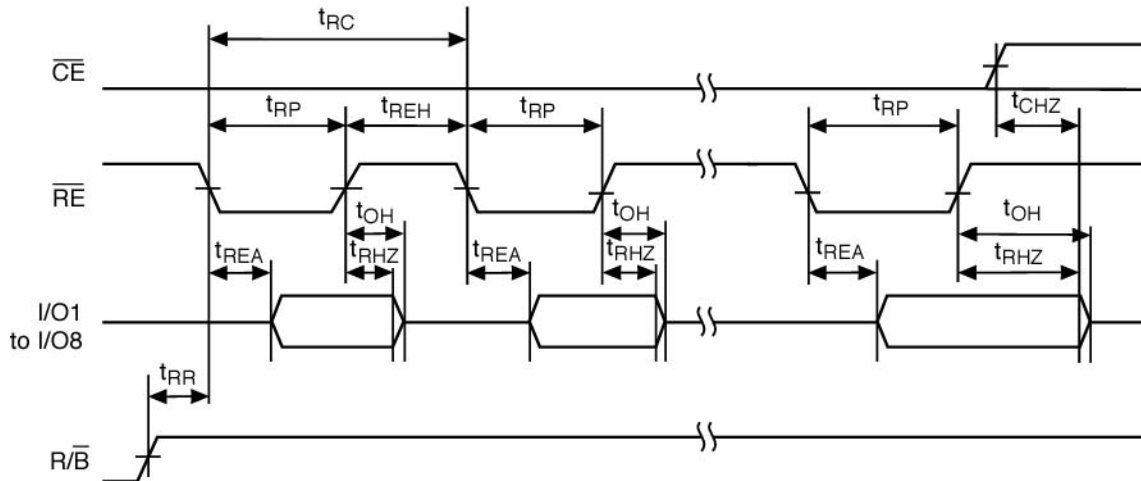


Figure 2-5 Serial Read Cycle Timing Diagram

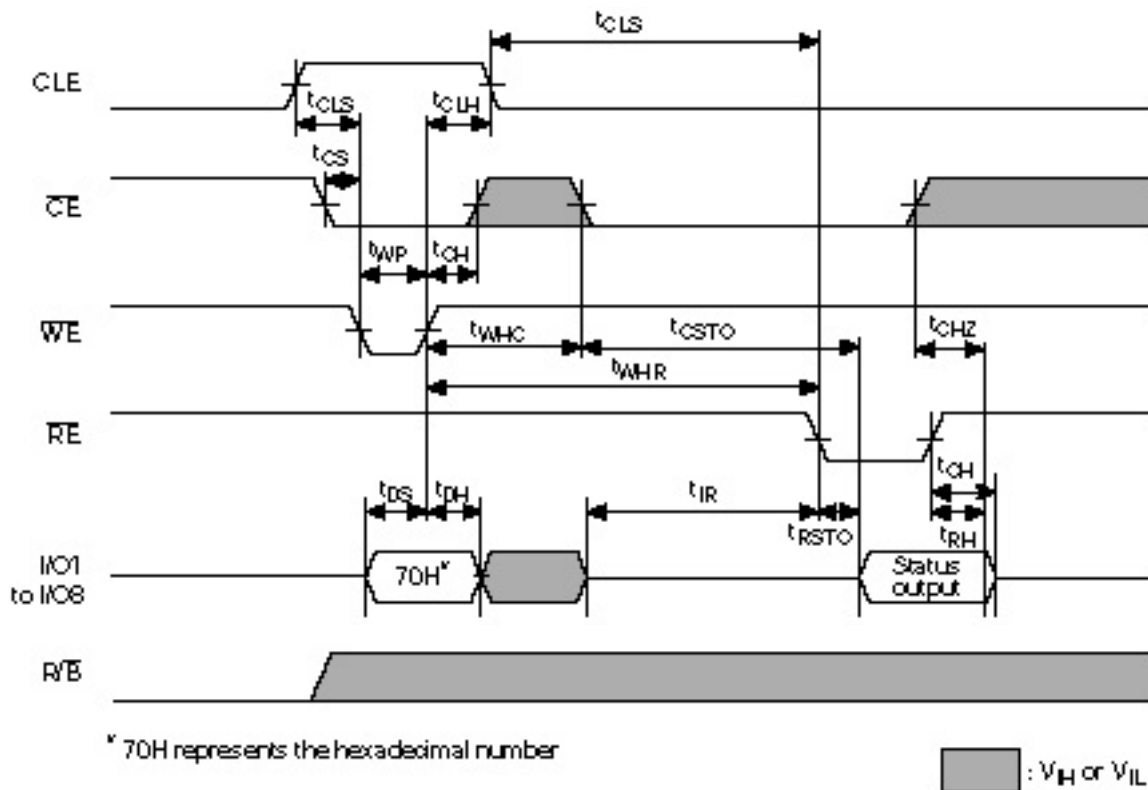


Figure 2-6 Status Read Cycle Timing Diagram

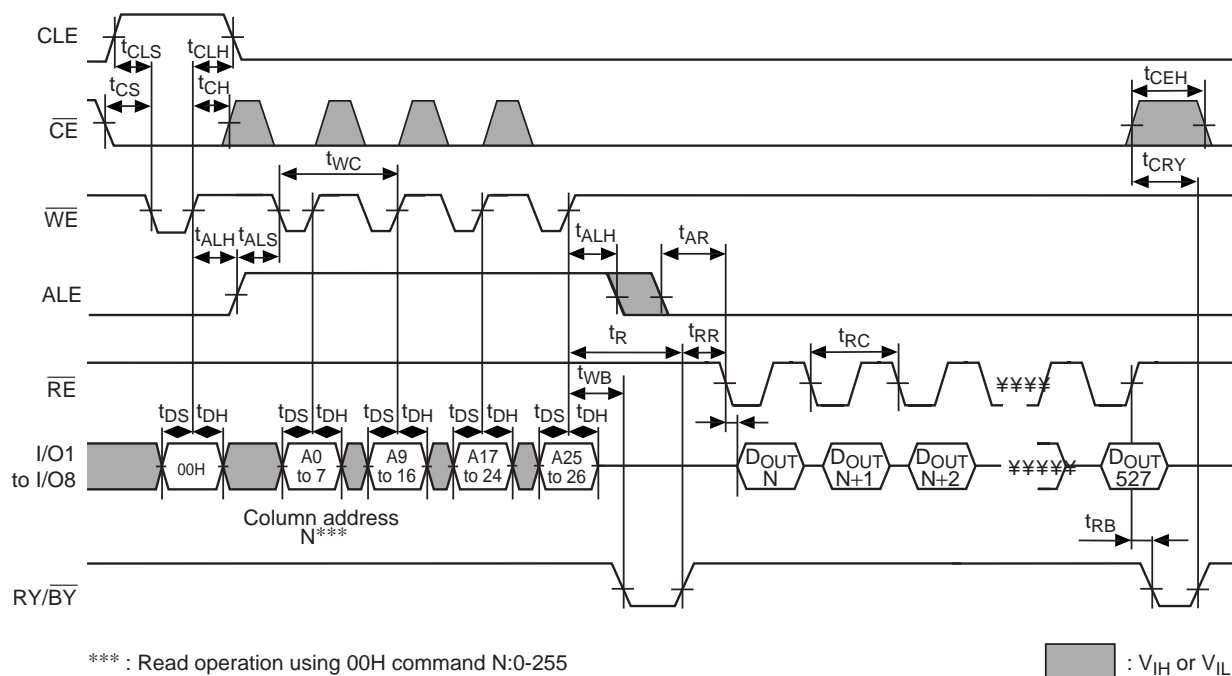
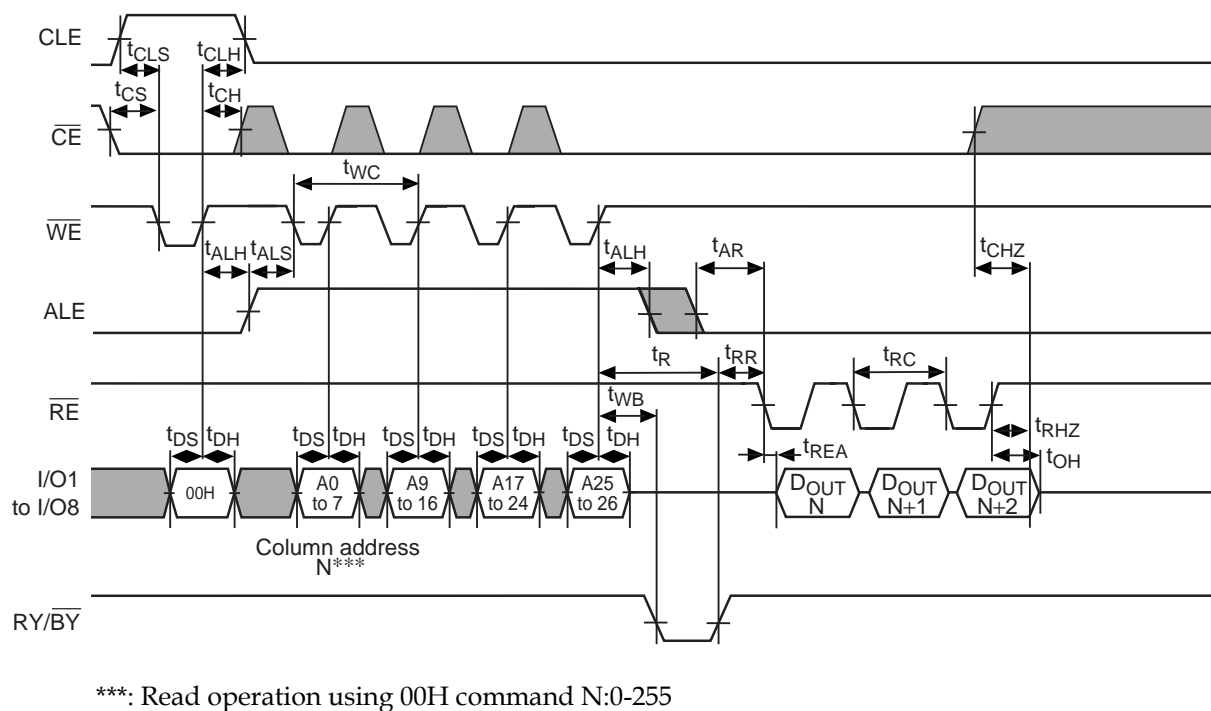


Figure 2-7 Read Cycle (1) Timing Diagram

Figure 2-8 Read Cycle (1) Timing Diagram: When Interrupted by \overline{CE}

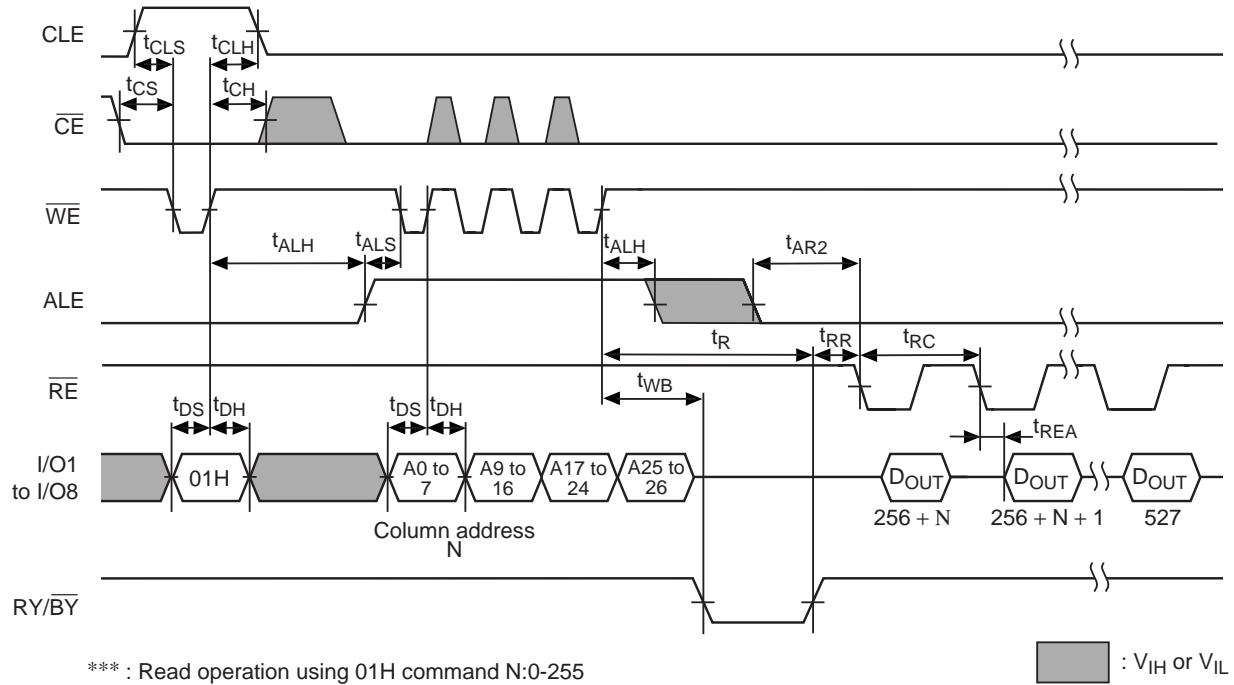


Figure 2-9 Read Cycle (2) Timing Diagram

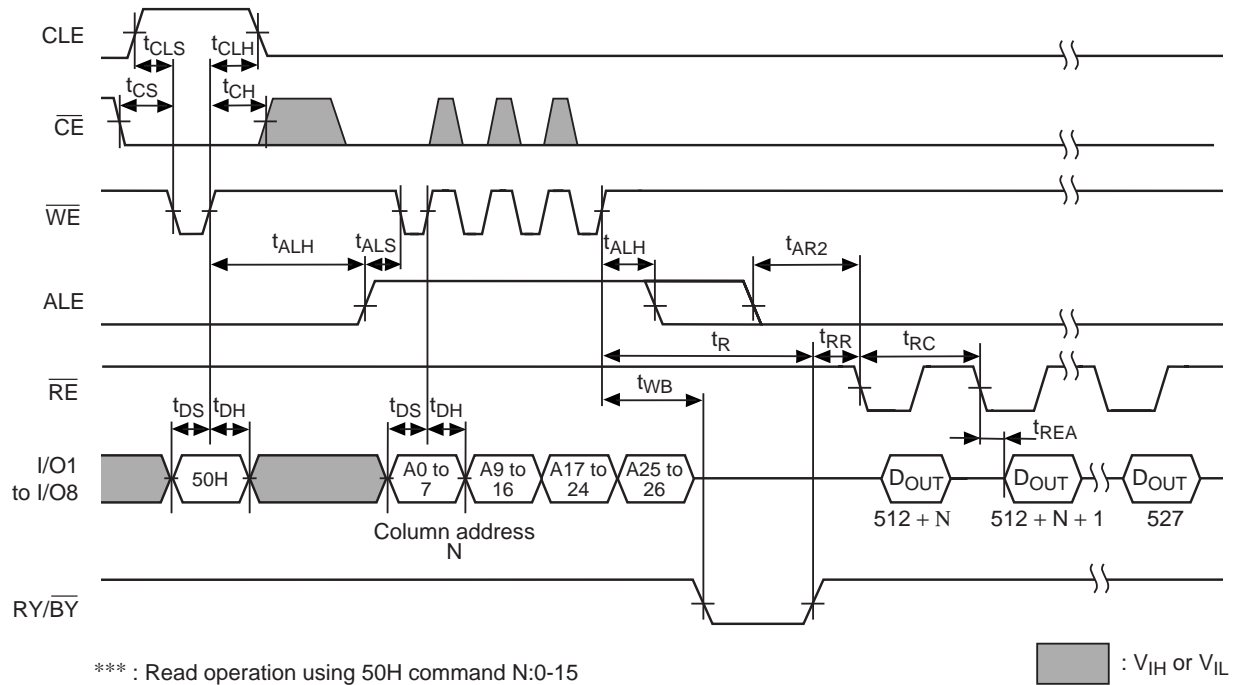


Figure 2-10 Read Cycle (3) Timing Diagram

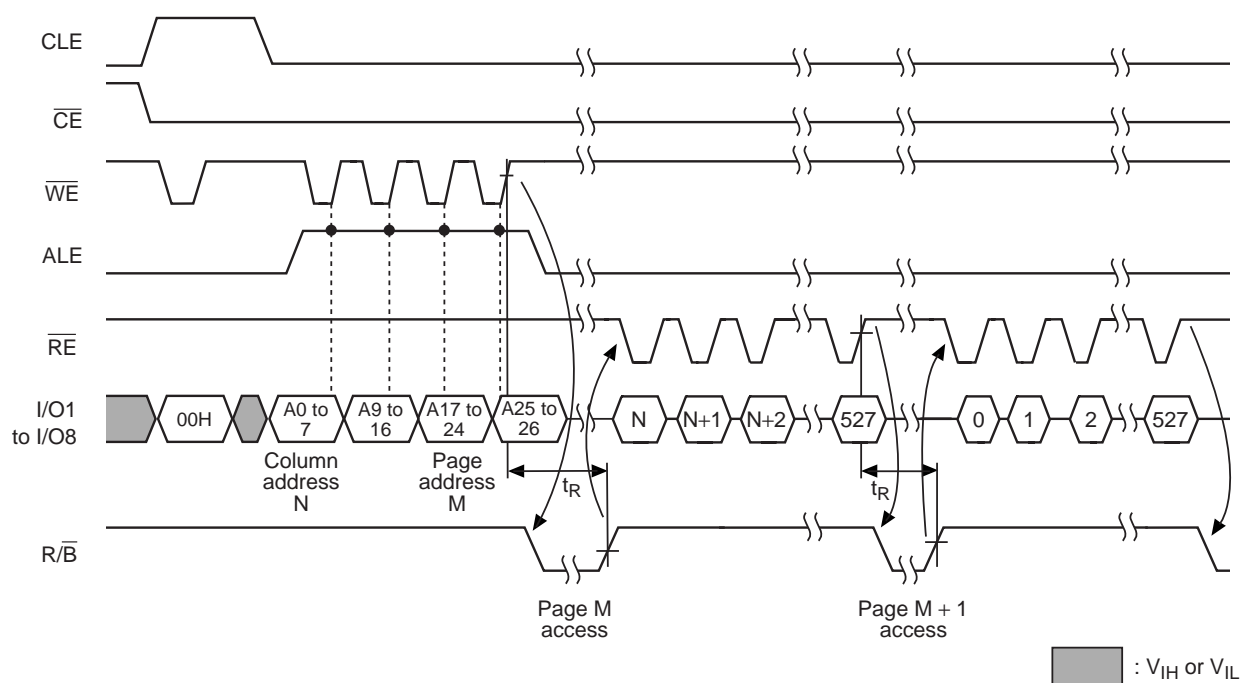


Figure 2-11 Sequential Read (1) Timing Diagram

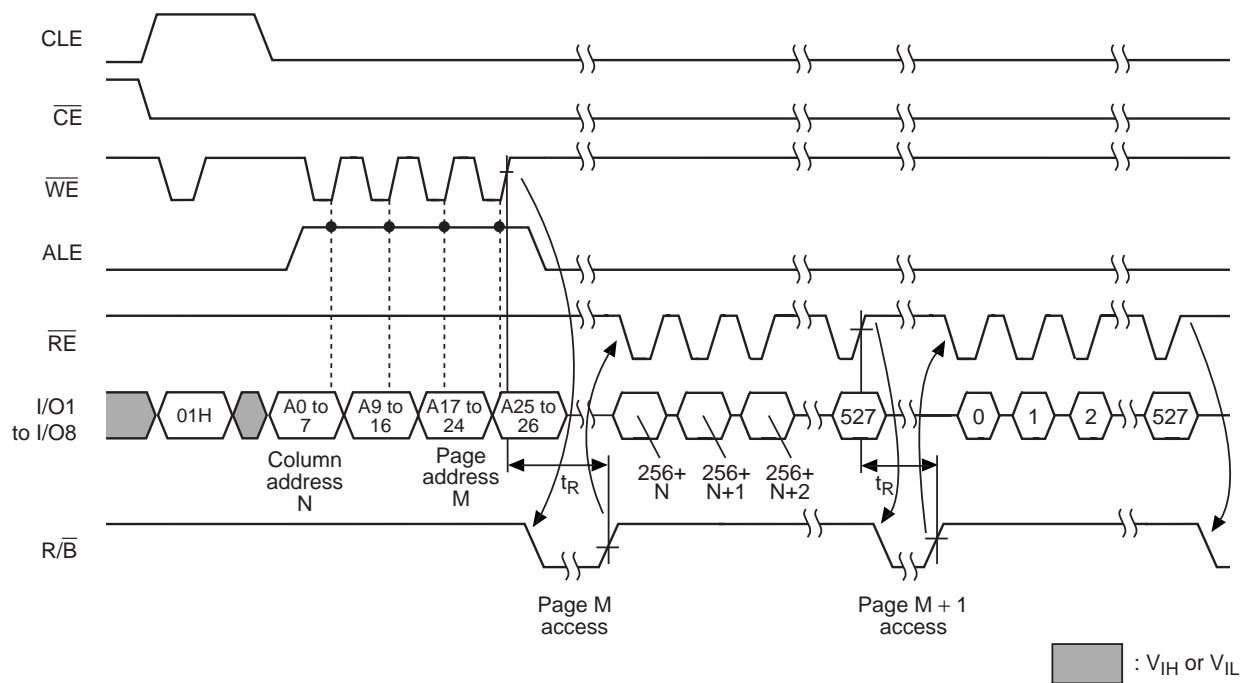


Figure 2-12 Sequential Read (2) Timing Diagram

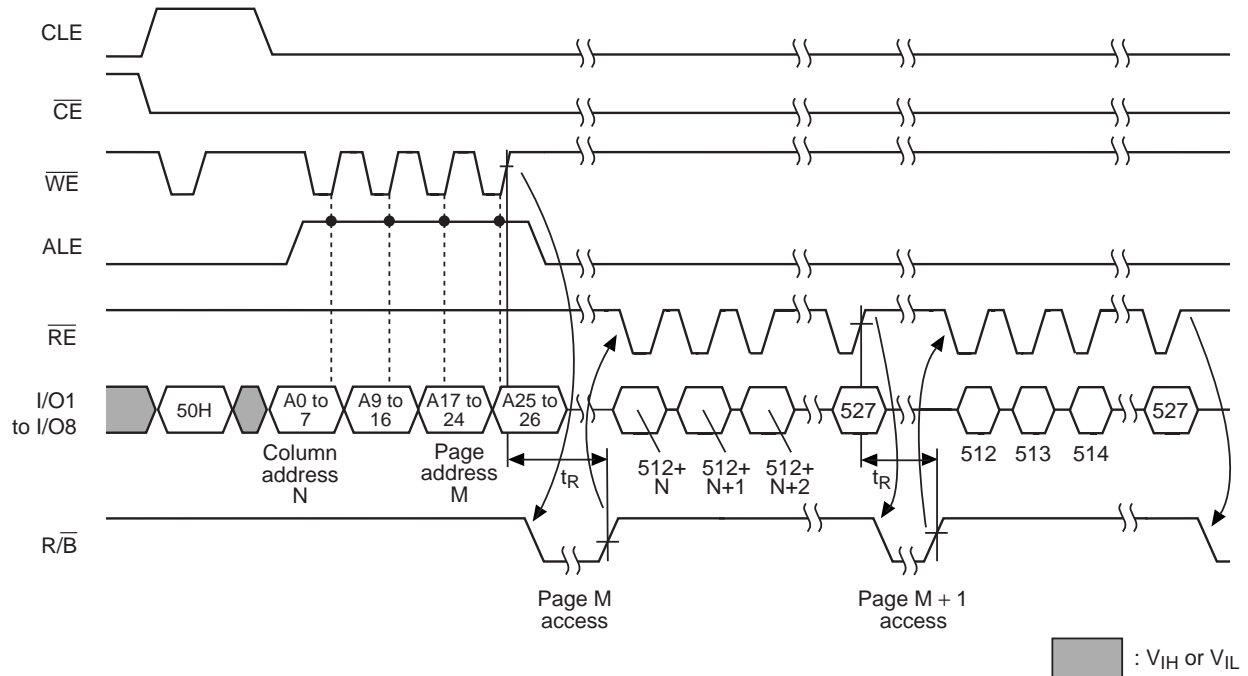


Figure 2-13 Sequential Read (3) Timing Diagram

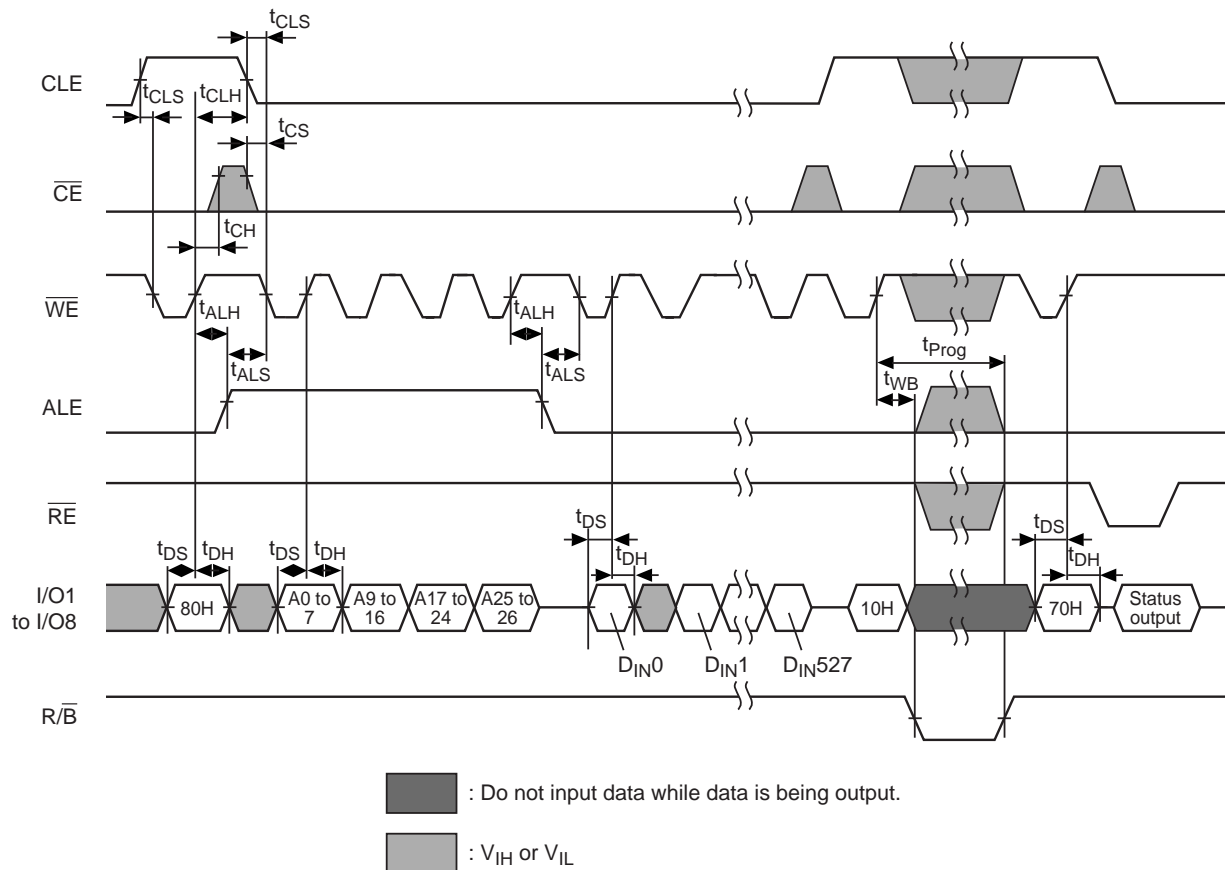


Figure 2-14 Auto-Program Operation Timing Diagram

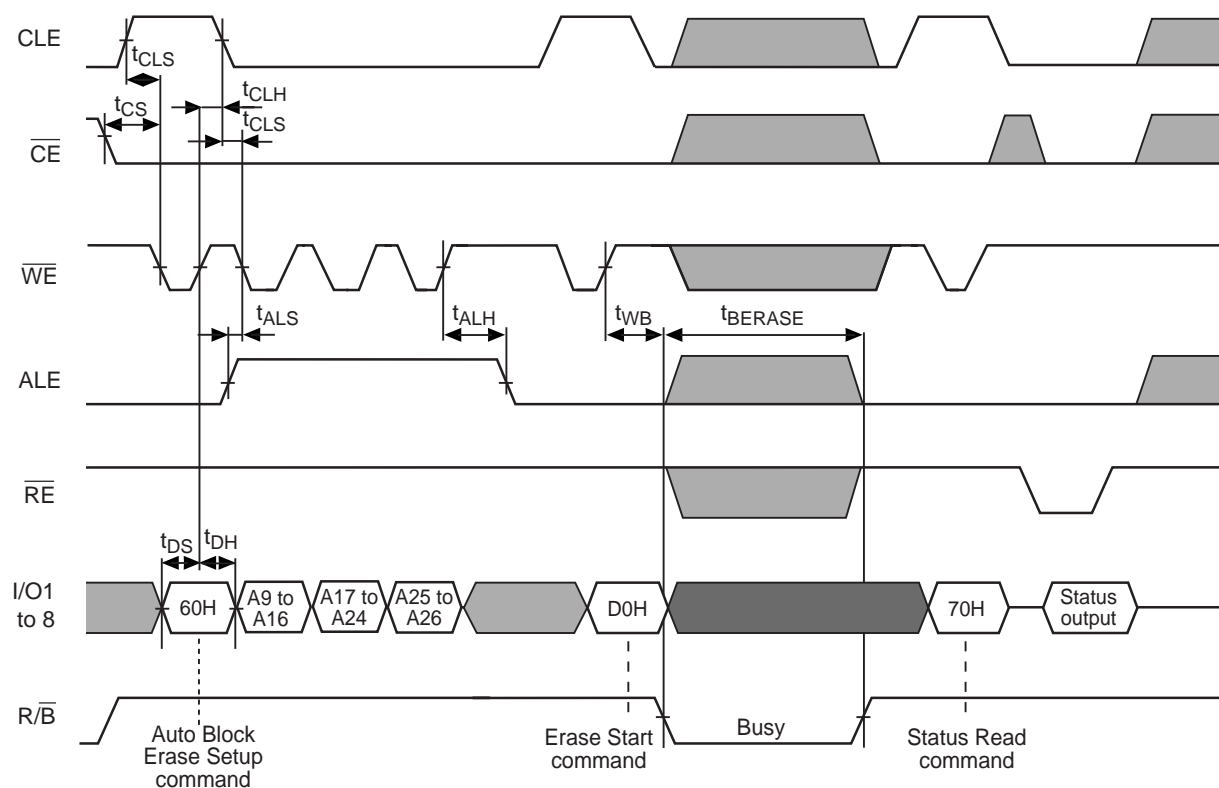


Figure 2-15 Auto Block Erase Timing Diagram

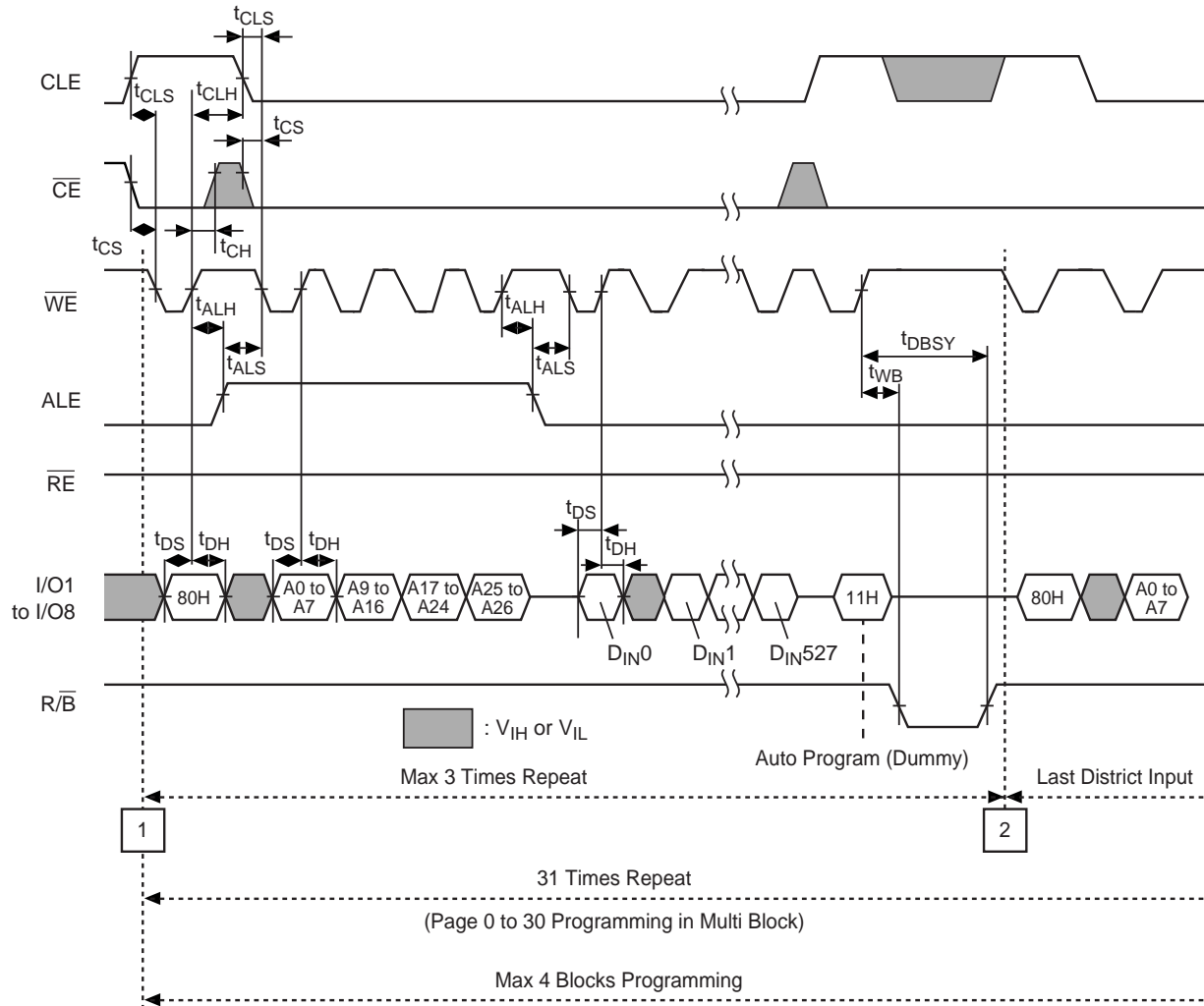


Figure 2-16 Multi Block Programming Timing

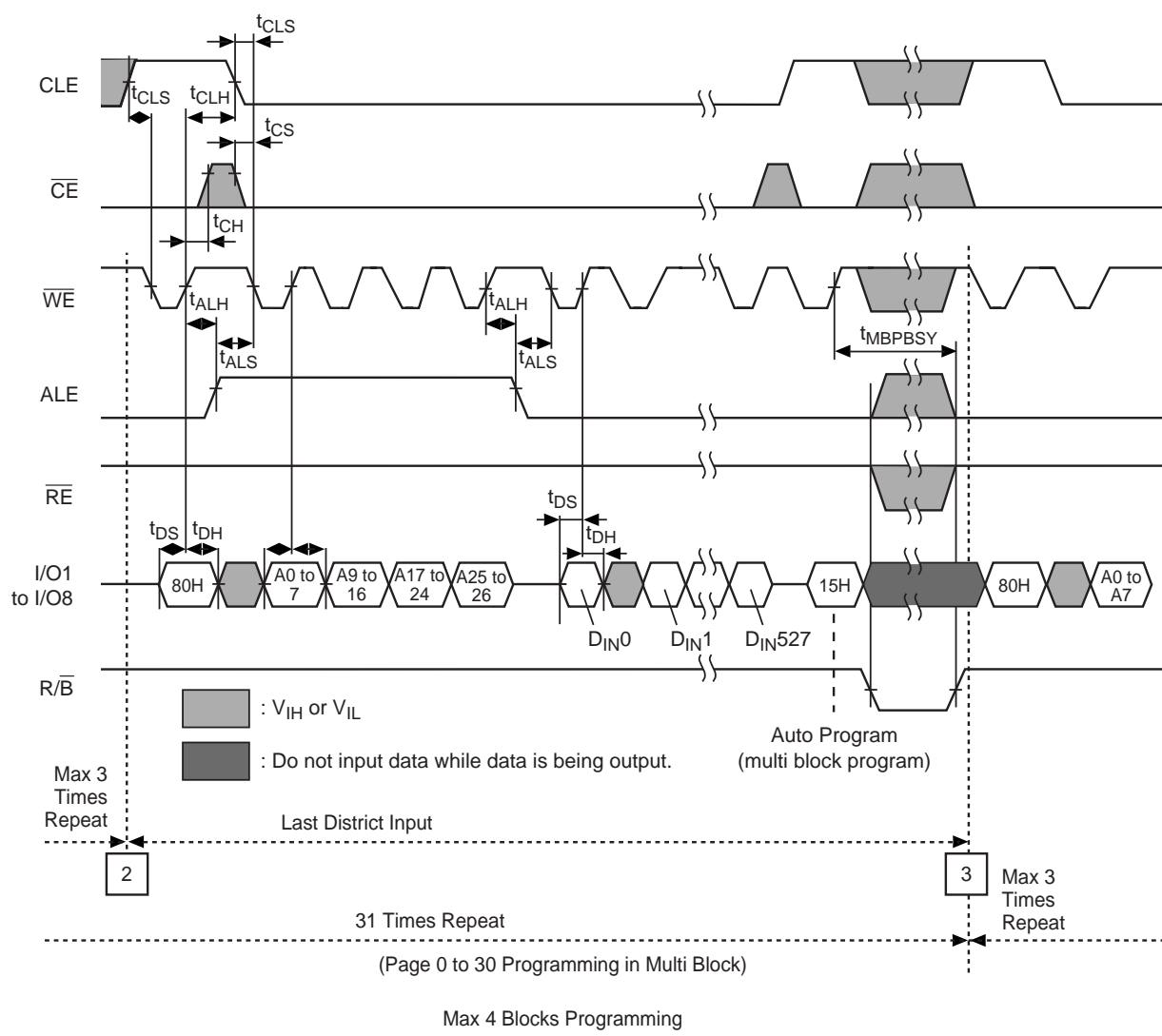


Figure 2-16 Multi Block Programming Timing (continued)

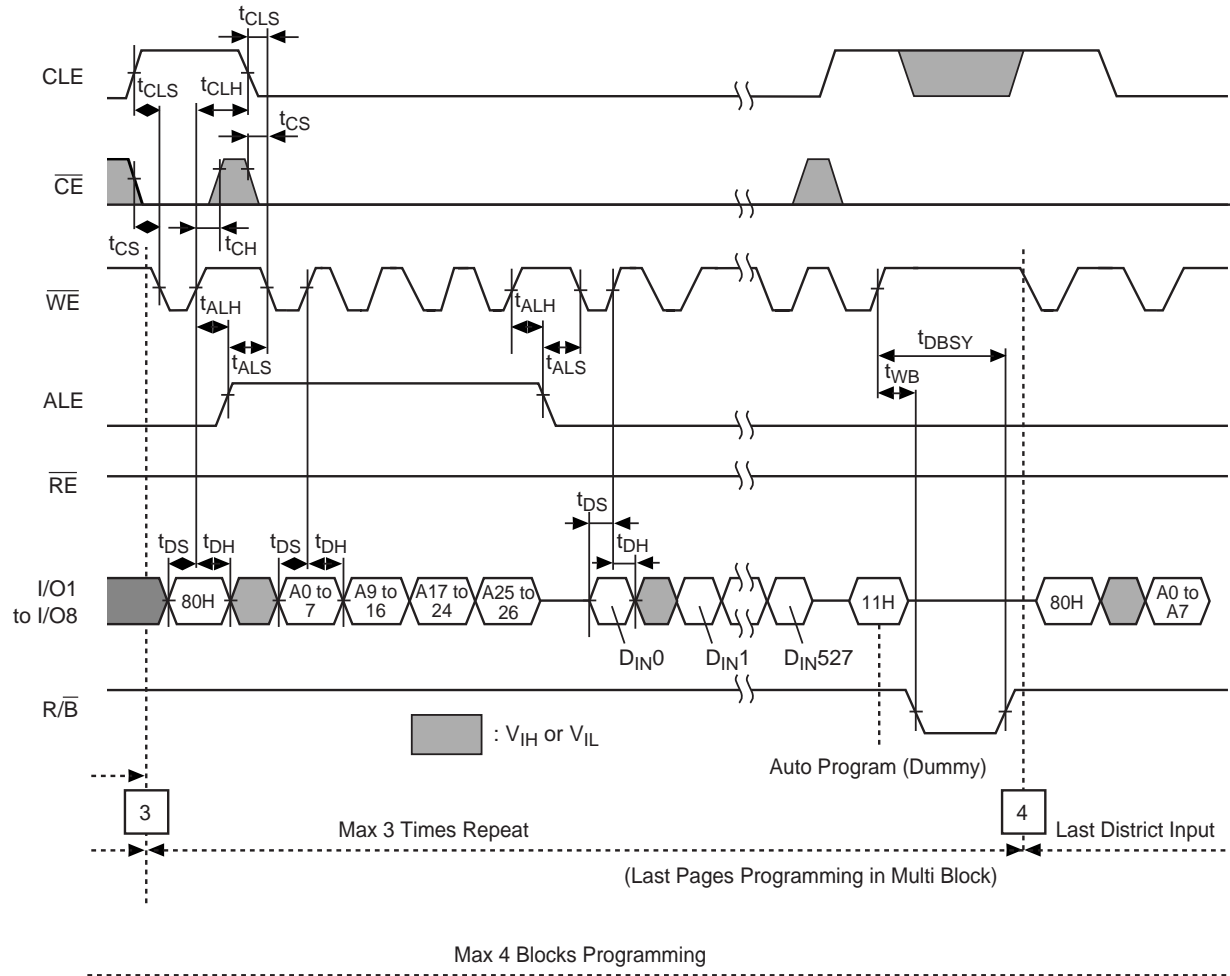


Figure 2-16 Multi Block Programming Timing (continued)

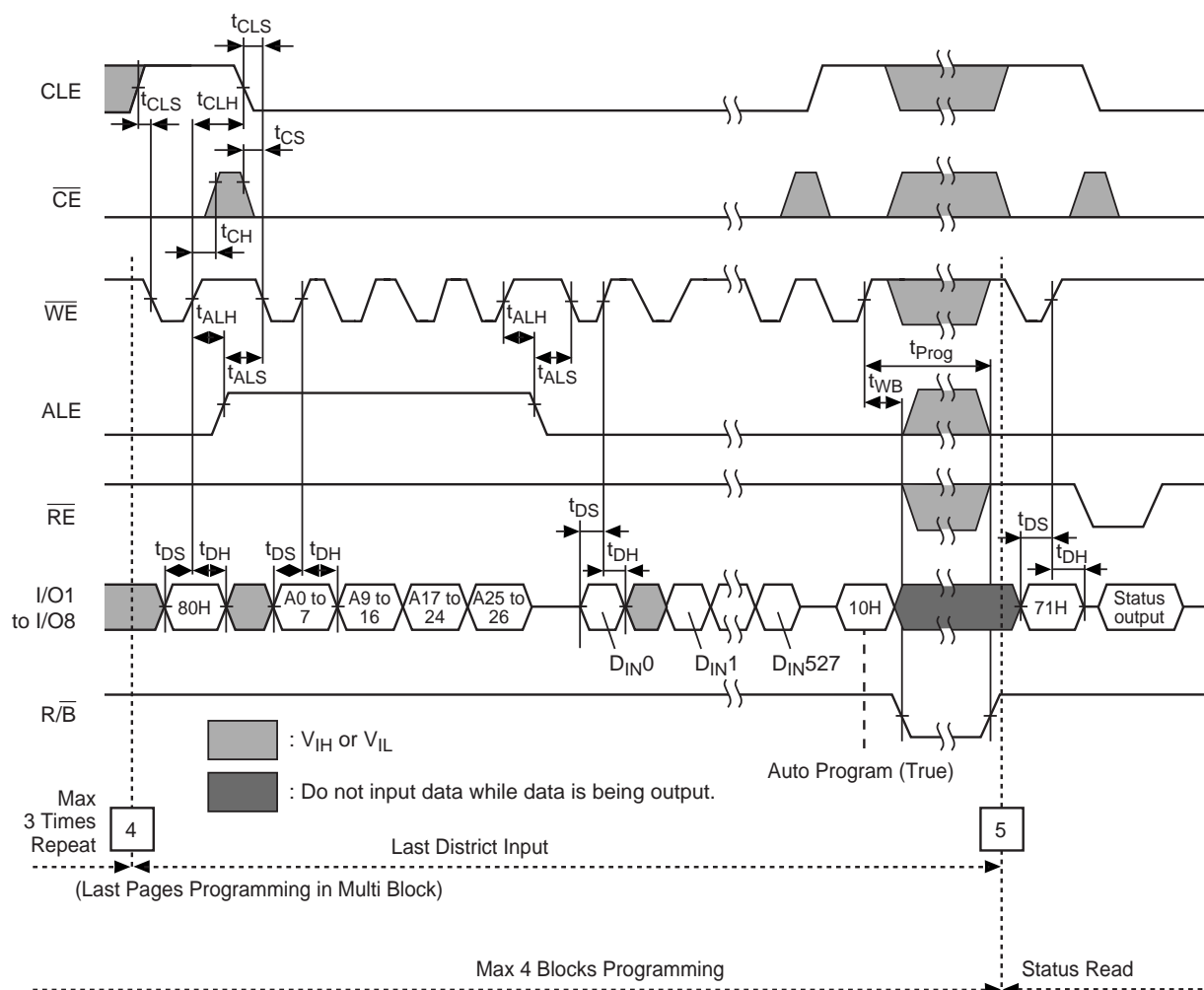


Figure 2-16 Multi Block Programming Timing (continued)

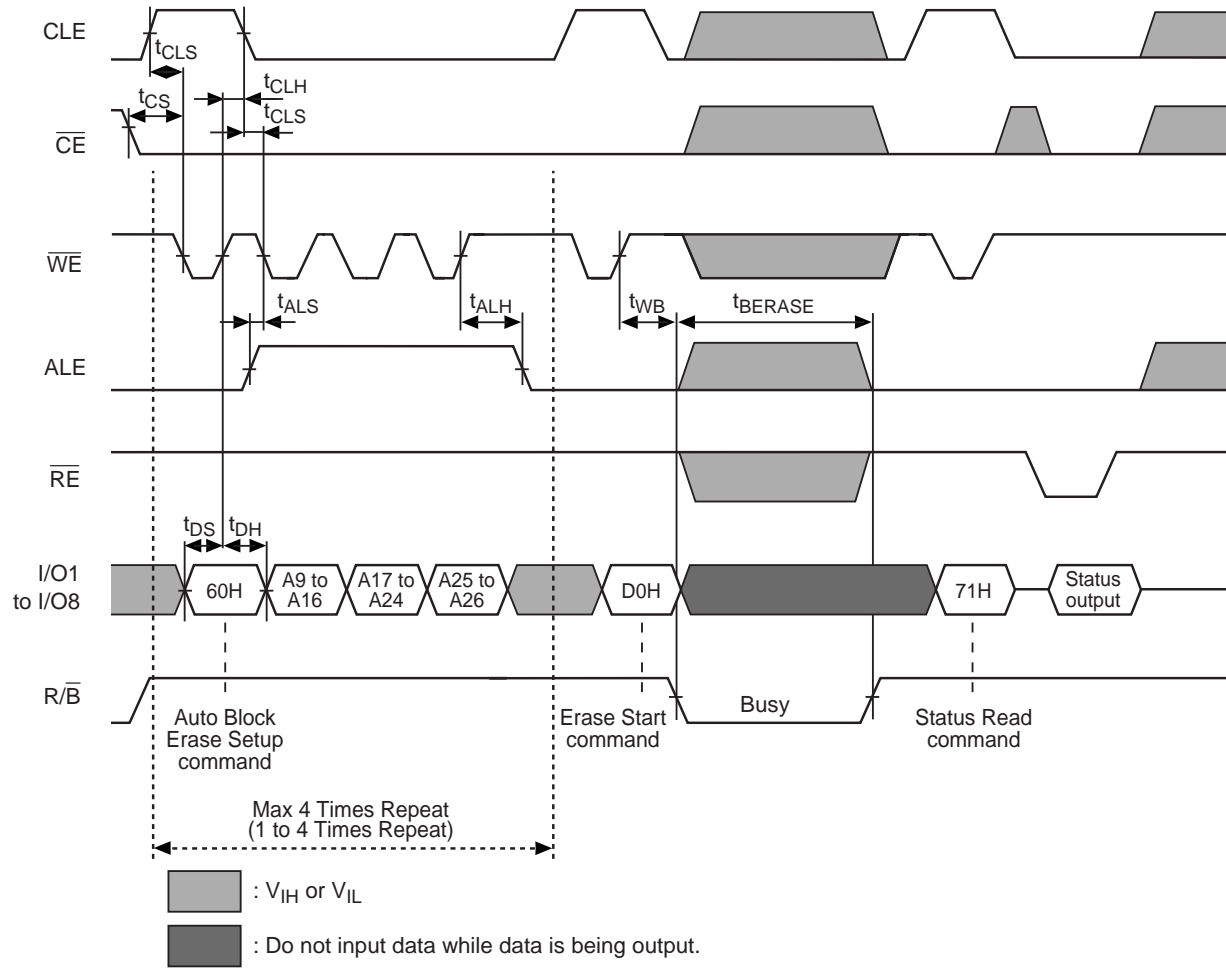


Figure 2-17 Multi Block Erase Timing Diagram

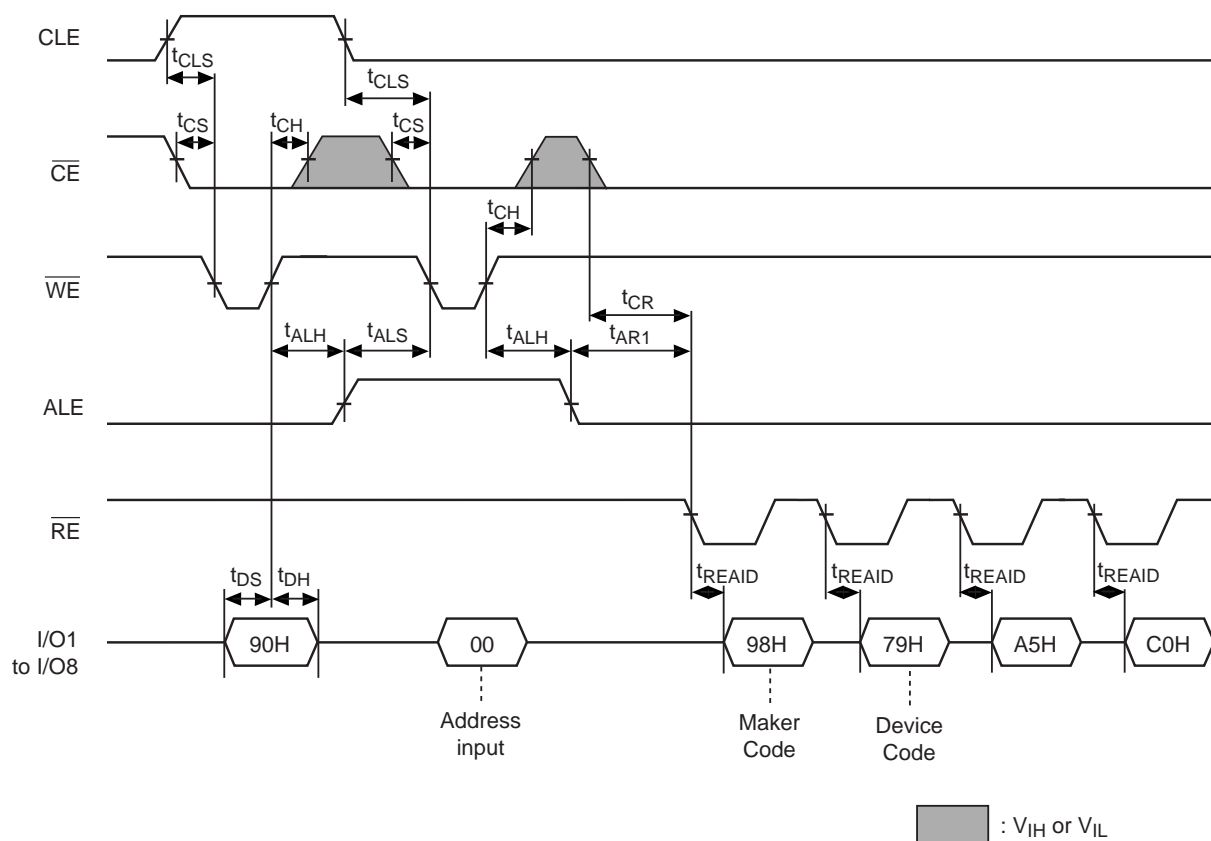


Figure 2-18 ID Read (1) Operation Timing Diagram

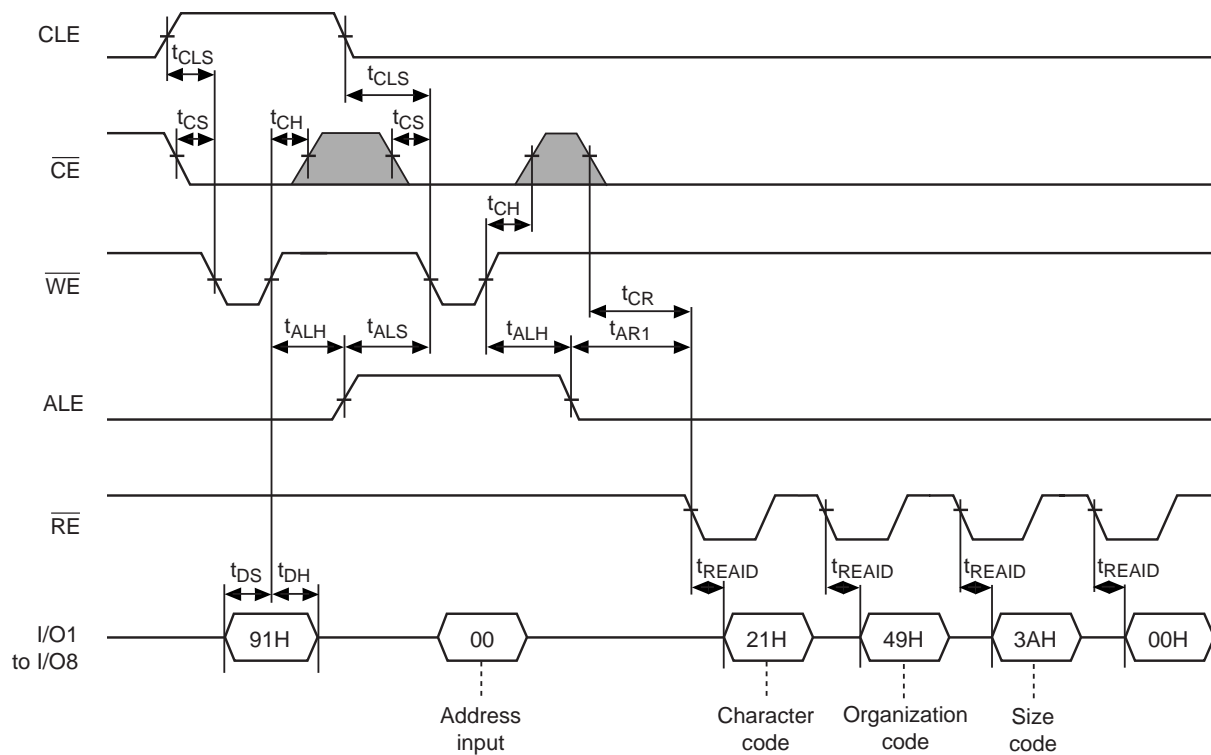


Figure 2-19 ID Read (2) Operation Timing Diagram

Table 2-1 Extended ID Information**Device Characteristics Code**

(automatically changed)

Organization Code**Size Code**

	IO1	IO0		IO3	IO2	IO1	IO0		IO7	IO6	IO5
Single chip use	0	0	64 MB	0	1	1	0	16KB	0	0	1
2-chip module	0	1	128 MB	0	1	1	1	32KB	0	1	0
4-chip module	1	0	256 MB	1	0	0	0	64KB	0	1	1
8-chip module	1	1	512 MB	1	0	0	1	128KB	1	0	0
			1 GB	1	0	1	0				

IO3,2 = 00 in 2LC mode

= 01 in 4LC mode

The number of bits per cell and the number of chips in the multi-chip module automatically change the organization code.

IO2,1,0 = 010
(meaning 512B-page size)

IO6,5,4 = 010

This device includes x4 multi-block mode.

IO4,5 = 00

IO3,4 = 11
(meaning extended page size = 16B)

IO7 = 0

This device doesn't have secondary data cache.

IO7,6 = 01 (meaning x8-data-bus width)

3.0 Pin Functions

The SmartMedia Card is a serial access memory device which uses time-sharing input of address information. The device pinouts are configured as shown in Figure 3-1.

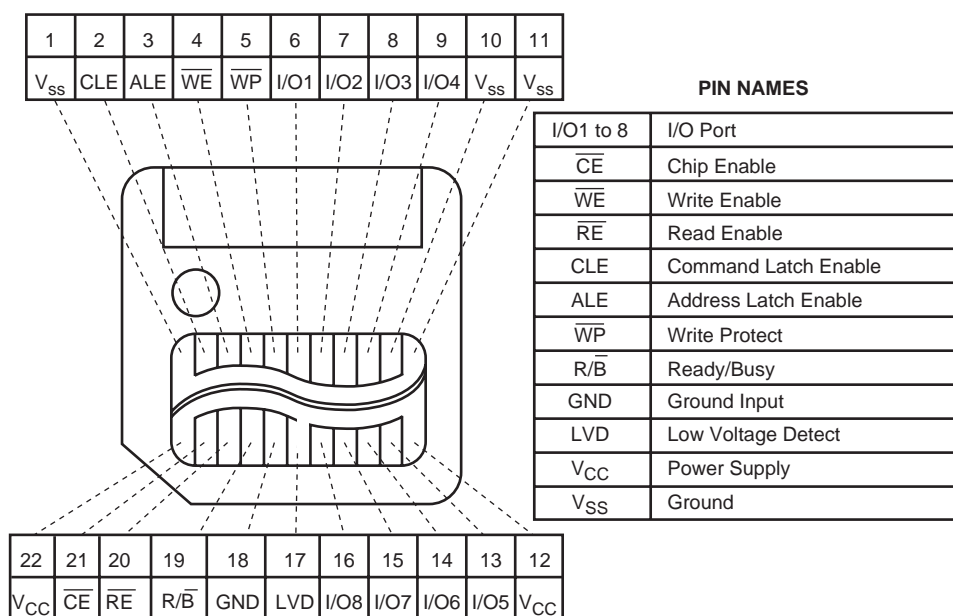


Figure 3-1 SmartMedia Card Pinout

3.1 Pin Descriptions

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of WE if ALE is High. If ALE is Low, input data is latched.

Chip Enable: $\overline{\text{CE}}$

The device goes into a low-power Standby Mode when $\overline{\text{CE}}$ goes High during a Read operation. The $\overline{\text{CE}}$ signal is ignored when the device is in the Busy state (R/B = L), such as during a Program or Erase operation, and will not enter Standby Mode even if the CE input goes High. The CE signal must stay Low during the Read Mode Busy state to ensure that memory array data is correctly transferred to the data register.





Write Enable: $\overline{\text{WE}}$

The WE signal is used to control the acquisition of data from the I/O port.

3.3 Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the different command operations shown in Table 3-4. Address input, command input and data input/output are controlled by the CLE, ALE, CE, WE, RE and WP signals, as shown in Table 3-3.

Table 3-2 Logic Table

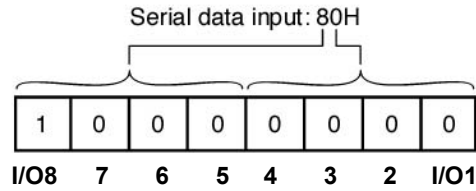
	CLE	ALE	CE	WE	RE	WP
Command Input	H	L	L		H	*
Data Input	L	L	L		H	*
Address input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

Table 3-3 Command Table (HEX)

	First Cycle	Second Cycle	Acceptable While Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	√
Auto Program (True)	10	—	
Auto Program (Dummy)	11	—	
Auto Program (Cache)	15	—	
Auto Block Erase	60	D0	
Status Read (1)	70	—	√
Status Read (2)	71	—	√
ID Read (1)	90	—	
ID Read (2)	91	—	

HEX data bit assignment
(Example)



Once the device has been set to Read mode by an 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations. The following table shows the operation states for Read mode.

Table 3-4 Read Mode Operation States

	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	I/O1 to I/O8	Power
Output Select	L	L	L	H	L	Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active
Standby	L	L	H	H	*	High Impedance	Standby

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

4.0 Device Operation

4.1 Read Mode (1)

Read mode (1) is set when an 00H command is issued to the Command register. Refer to Figure 4-1 below for timing details and the block diagram.

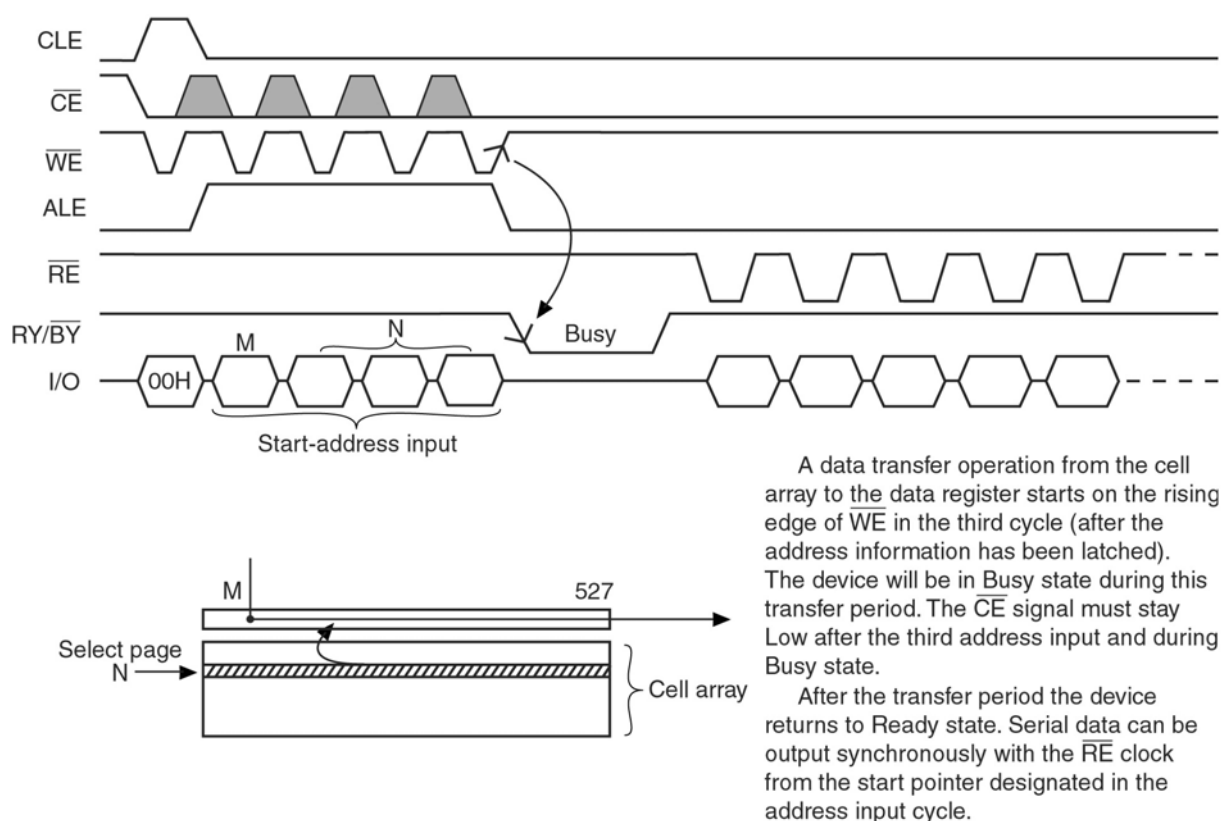


Figure 4-1 Read Mode (1) Operation

4.2 Read Mode (2)

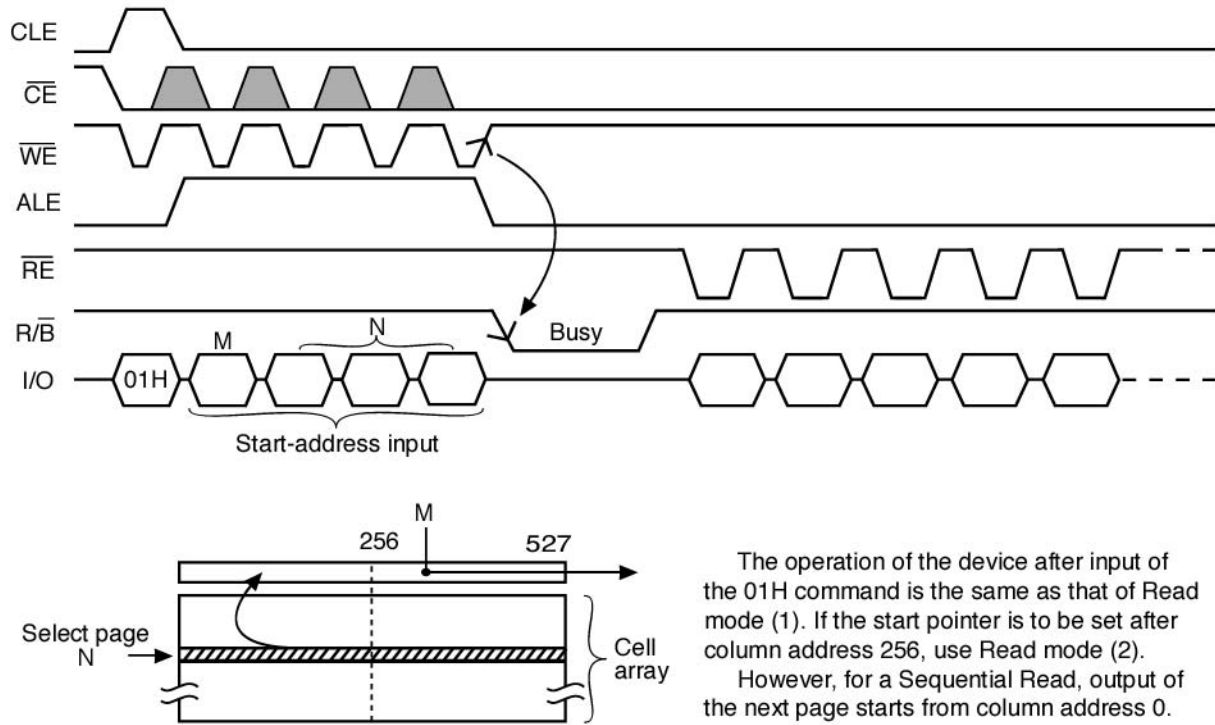


Figure 4-2 Read Mode (2) Operation

4.3 Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

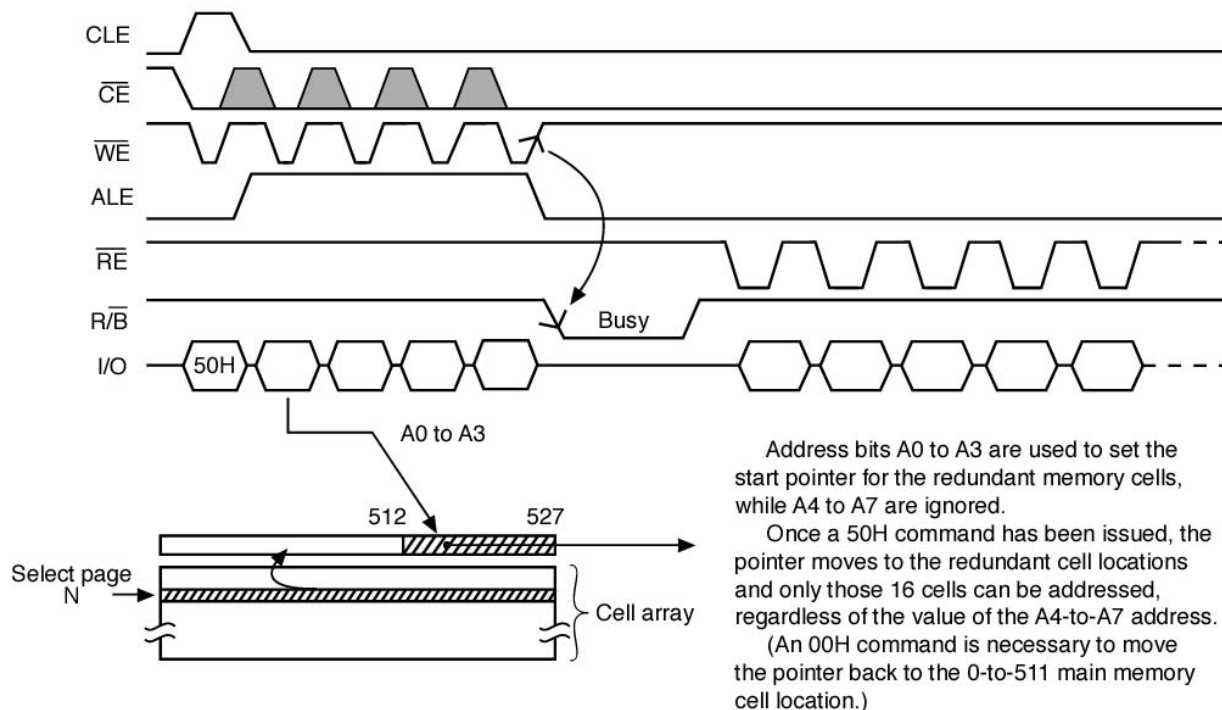


Figure 4-3 Read Mode (3) Operation

4.4 Sequential Read (1) (2) (3)

This mode allows the sequential reading of pages without additional address input.

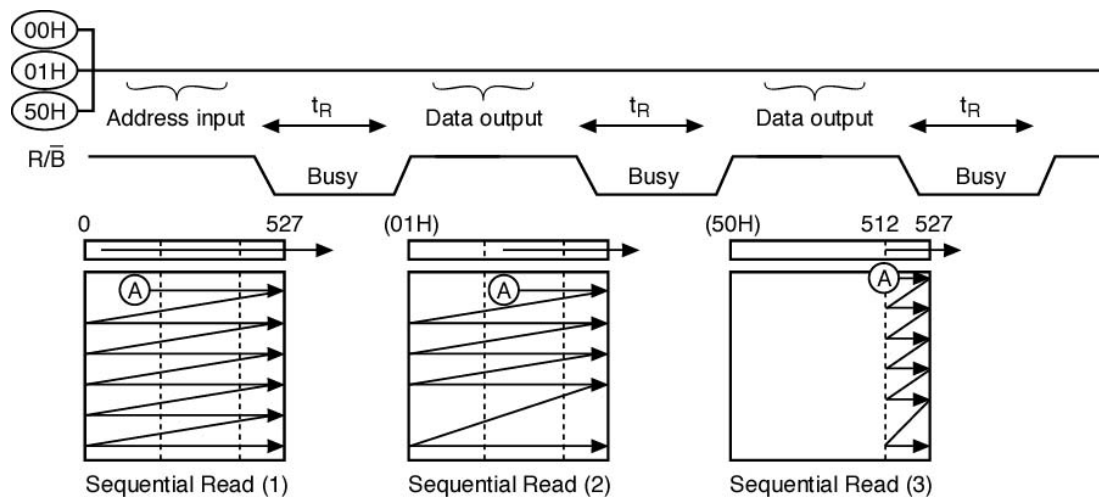


Figure 4-4 Sequential Read (1) (2) (3) Operation

Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the page address reaches the next block address, read command (00H/01H/50H) and address input are needed.

4.5 Status Read

The SmartMedia Card has two Status Read commands. One is Status Read (1) command 70H and the other is Status Read (2) command 71H.

This device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass / fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the \overline{RE} clock after a 70H or 71H command input.

The resulting information of the Status Read (1) command 70H is outlined in the table below and the resulting information of Status Read (2) command 71H is outlined in the explanation for Multi Block Program and Multi Block Erase toward the end of this document.

Table 4-1 Status Output Table for Status Read (1) Command 70H

	Status	Output
I/O1	Pass/Fail	Pass: 0 Fail: 1
I/O2	Not Used	0
I/O3	Not Used	0
I/O4	Not Used	0
I/O5	Not Used	0
I/O6	Not Used	0
I/O7	Ready/Busy	Ready: 1 Busy: 0
I/O8	Write Protect	Protect: 0 Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

Note: In the case of Multi Block Write/Erase, I/O1 to I/O5 have an additional definition.

An application example with multiple devices is shown in Figure 4-5.

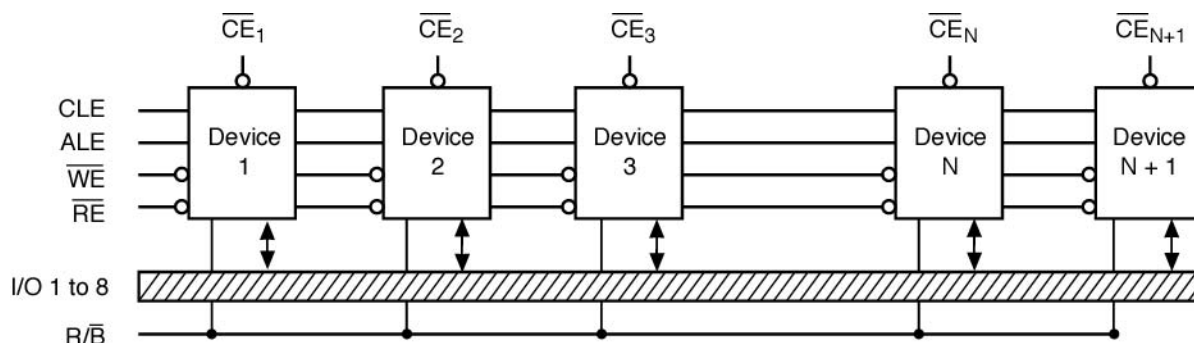


Figure 4-5 Application Example with Multiple Devices

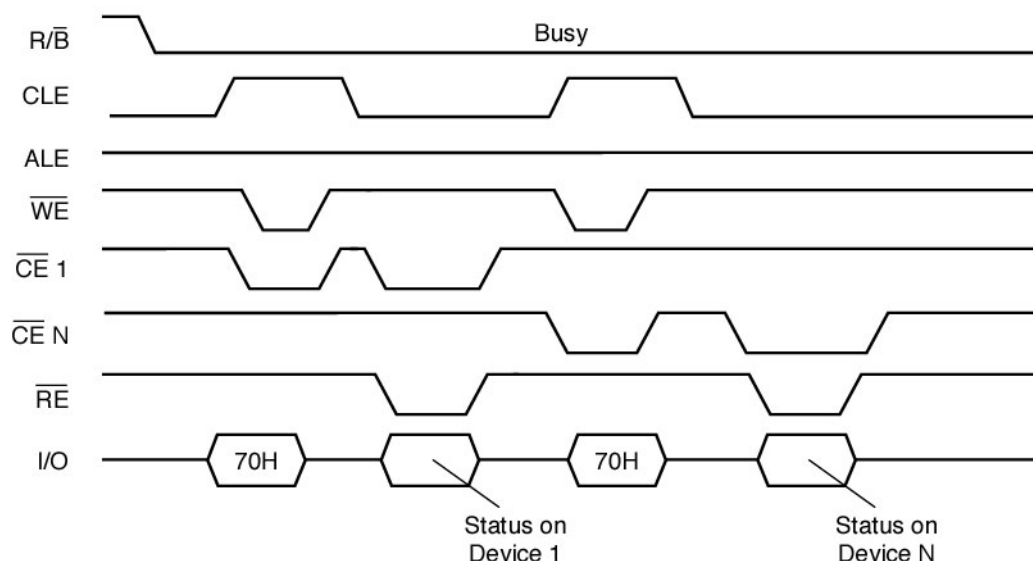


Figure 4-6 Status Read Timing Application Example

System Design Note: If the $\overline{R/B}$ pin signals from multiple devices are wired together as shown in Figure 4-5, the Status Read function can be used to determine the status of each individual device.

4.6 Auto Page Program

The device carries out an Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below.

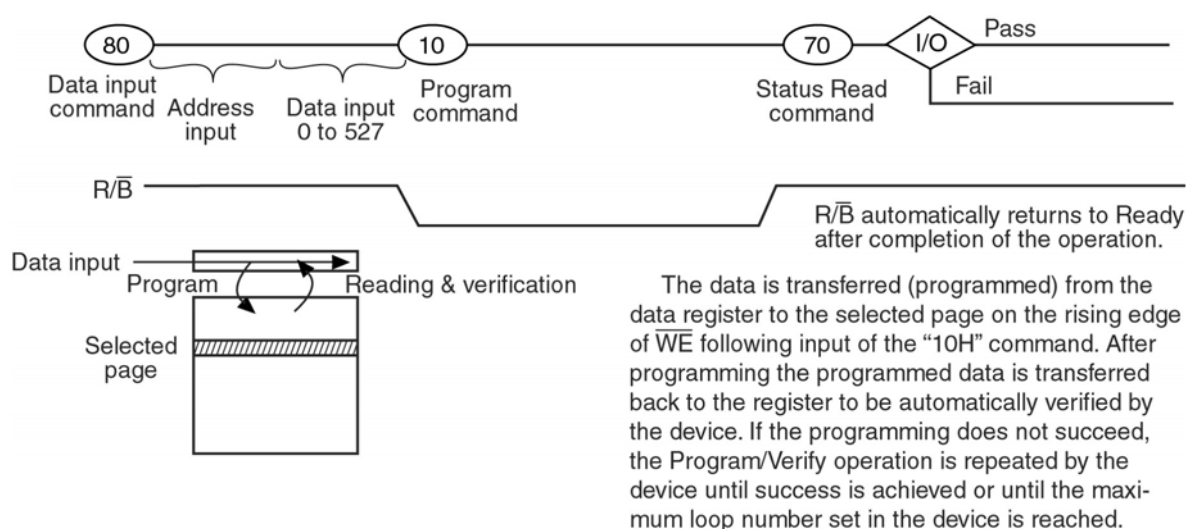


Figure 4-7 Auto Page Program Operation

4.7 Auto Block Erase

The Auto Block Erase operation starts on the rising edge of \overline{WE} after the Erase Start command DOH which follows the Erase Setup command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.

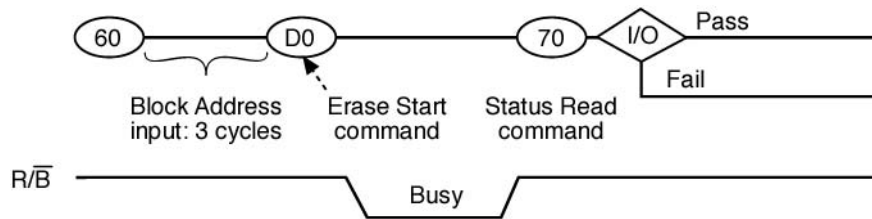
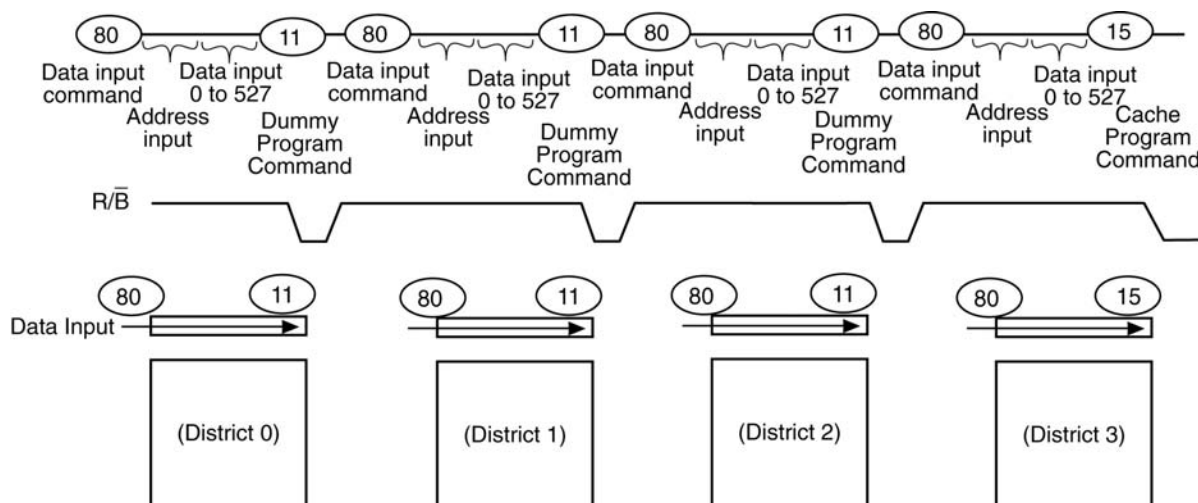


Figure 4-8 Auto Block Erase Operation

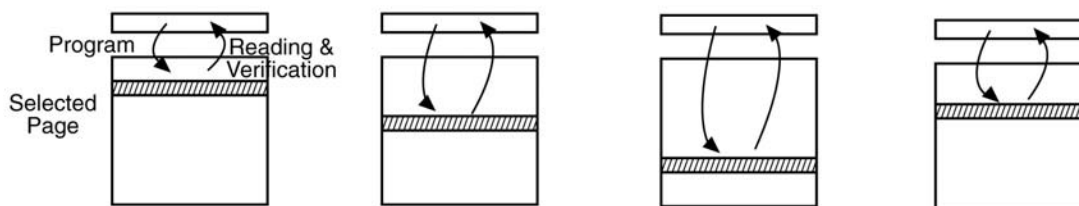
4.8 Multi Block Program

The device carries out a Multi Block Program operation when it receives a 15H or 10H Program command after some sets of the address and data have been input.

In the interval of the Multi District address and the data input (512+16Byte), 11H Dummy Program command is used when it still continues the data input into another District. The sequence of command, address and data input is shown below.



After the 15H Cache Program command, physical programming starts as follows:



The data is transferred (programmed) from the register to the selected page on the rising edge of \overline{WE} following input of the 15H command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Figure 4-9 Multi Block Program Operation

After 15H Cache Program command, physical programming starts as follows.

Starting the upper operation from the first page of the selected erase blocks, and then repeating the operation for a total of 31 times while incrementing the page address in the blocks, and then inputting the last page data of the blocks, the 10H command executes final programming.

In this full sequence, the command sequence is below.

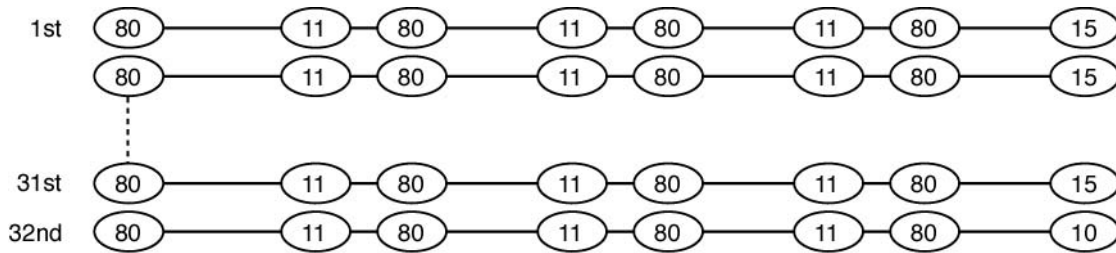


Figure 4-10 Command Sequence

After the 10H command, the total results of the upper operation is shown through the Status Read command.

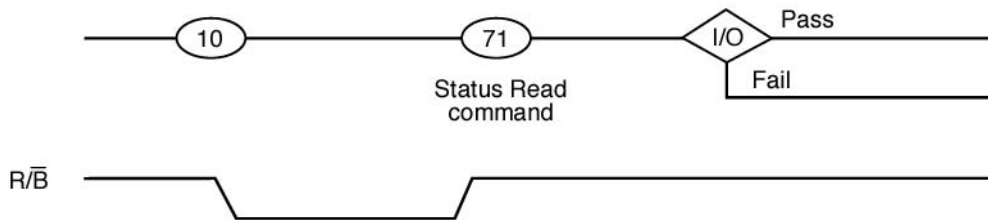


Figure 4-11 Status Read (2) Command

The Status description is below.

Table 4-2 Status Description Table

	Status	Output	<p>I/O1 describes total Pass/ Fail condition. If at least one fail occurred in 32 times X 4 (512+16Byte) page write operation, it shows "Fail" condition,</p> <p>I/O2 describes total Pass/ Fail condition. If at least one fail occurred in 32 times X 1 (512+16Byte) page write operation in District 0 area, it shows "Fail" condition,</p> <p>I/O3, I/O4 and I/O5 are as same manner as I/O2.</p>
I/O1	Total Pass/Fail	Pass: 0 Fail: 1	
I/O2	District 0 Pass/Fail	Pass: 0 Fail: 1	
I/O3	District 1 Pass/Fail	Pass: 0 Fail: 1	
I/O4	District 2 Pass/Fail	Pass: 0 Fail: 1	
I/O5	District 3 Pass/Fail	Pass: 0 Fail: 1	
I/O6	Not Used	do not care	
I/O7	Ready/Busy	Ready: 1 Busy: 0	
I/O8	Write Protect	Protect: 0 Not Protect: 1	

4.8.1 Internal Addressing in Relation with the Districts

To use the Multi Block Program operation, the internal addressing should be such that at most one block is selected within each district.

The device consists of two chips, each of which has four Districts. Each District consists from 1024 erase blocks. The allocation rule is follows.

Chip0, District0 : Block0, Block4, Block8, Block12,,Block4092

Chip0, District1 : Block1, Block5, Block9, Block13,,Block4093

Chip0, District2 : Block2, Block6, Block10, Block14,,Block4094

Chip0, District3 : Block3, Block7, Block11, Block15,,Block4095

Chip1, District0 : Block4096, Block4100, Block4104, Block4108,,Block8188

Chip1, District1 : Block4097, Block4101, Block4105, Block4109,,Block8189

Chip1, District2 : Block4098, Block4102, Block4106, Block4110,,Block8190

Chip1, District3 : Block4099, Block4103, Block4107, Block4111,,Block8191

4.8.2 Address Input Restriction for the Multi Block Program Operation

In selecting the blocks for the Multi Block Program operation, the conditions below apply.

- Restriction
 - Maximum one block should be selected from each District.
 - The data input operation should be started from the same number page of the selected block and the page number in the blocks should be the same number at programming time.
- Acceptance
 - There is no order limitation of the District for address input.
 - Any number of the District can be select for programming.
 - For example, the following operation is acceptable.
 - (80) [District2] (11) (80) [District0] (11) (80) [District1] (15)

No mutual address relation between the selected blocks from each District is required.

4.8.3 Operating Restriction During the Multi Block Program Operation

- Restriction—Starting from the first page of data input, until the device issues a 10H command, any other command out of defined sequence can not be issued except Status Read and Reset commands.
- Acceptance—The data input operation can be terminated with the 10H command instead of 15H command in the middle of the page number in the block. In this case the Status represents the reflected value accumulated from first page programming of this sequence and up to the last page programming terminated by 10H command.

4.9 Status Read Operation

Until the Ready condition after the programming is terminated by a 10H command, the effective bit in the Status data is limited to the Ready/Busy bit. In other words, Pass/Fail condition can be checked only in the Ready condition after a 10H command.

4.10 Multi District Block Erase

The device carries out a Multi District Block Erase operation when it receives a D0H command after some sets of the address have been input. After the D0H command, the total results of the Erase operation are shown through the Status Read (2) command 71H.

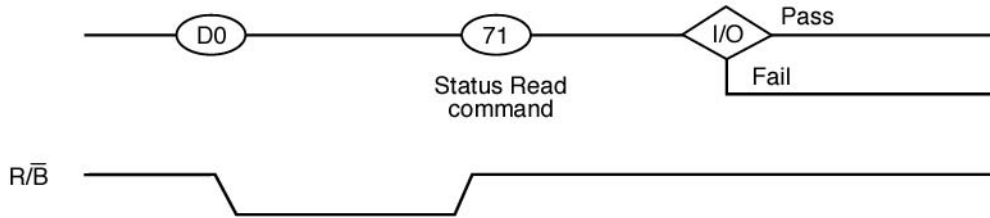


Figure 4-12 Status Read (2) Command

The Status description is below.

Table 4-3 Multi District Block Erase Status Description

	Status	Output	
I/O1	Total Pass/Fail	Pass: 0 Fail: 1	I/O1 describes total Pass/ Fail condition. If at least one fail occurred in Max4 Blocks erase operation, it shows "Fail" condition.
I/O2	District 0 Pass/Fail	Pass: 0 Fail: 1	
I/O3	District 1 Pass/Fail	Pass: 0 Fail: 1	
I/O4	District 2 Pass/Fail	Pass: 0 Fail: 1	I/O2 describes Pass/ Fail condition. If fail occurred in District 0 area, it shows "Fail" condition,
I/O5	District 3 Pass/Fail	Pass: 0 Fail: 1	
I/O6	Not Used	Do Not Care	
I/O7	Ready/Busy	Ready: 1 Busy: 0	I/O3, I/O4 and I/O5 are the same as I/O2.
I/O8	Write Protect	Protect: 0 Not Protect: 1	

4.10.1 Internal Addressing in Relation with the Districts

To use the Multi Block Erase operation, the internal addressing should be such that at most one block is selected within each district.

The device consists of two chips, each of which has four Districts.

Each District consists of 1024 erase blocks.

The allocation rule is below.

Chip0, District0 : Block0, Block4, Block8, Block12,,Block4092

Chip0, District1 : Block1, Block5, Block9, Block13,,Block4093

Chip0, District2 : Block2, Block6, Block10, Block14,,Block4094

Chip0, District3 : Block3, Block7, Block11, Block15,,Block4095

Chip1, District0 : Block4096, Block4100, Block4104, Block4108,,Block8188

Chip1, District1 : Block4097, Block4101, Block4105, Block4109,,Block8189

Chip1, District2 : Block4098, Block4102, Block4106, Block4110,,Block8190

Chip1, District3 : Block4099, Block4103, Block4107, Block4111,,Block8191

4.10.2 Address Input Restriction for the Multi District Block Erase Operation

In selecting the blocks for the Multi District Block Erase operation, the conditions below apply.

- Restriction—Maximum one block should be selected from each District.
- Acceptance—There is no order limitation of the District for the address input. Any number of the Districts can be select for the erase operation. For example, the following operation is in acceptance: (60) [District2] (60) [District0] (60) [District1] (D0).

No mutual address relation between the selected blocks from each District is required.

4.11 Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters the Wait state. The address and data registers are set as follows after a Reset:

- Address Register: All "0"
- Data Register: All "1"
- Operation Mode: Wait state

The response to an FFH Reset command input during the various device operations is as follows:

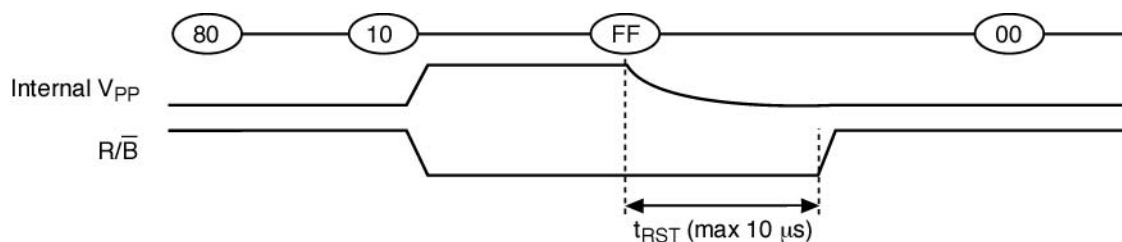


Figure 4-13 When a Reset Command (FFH) is Input During Programming

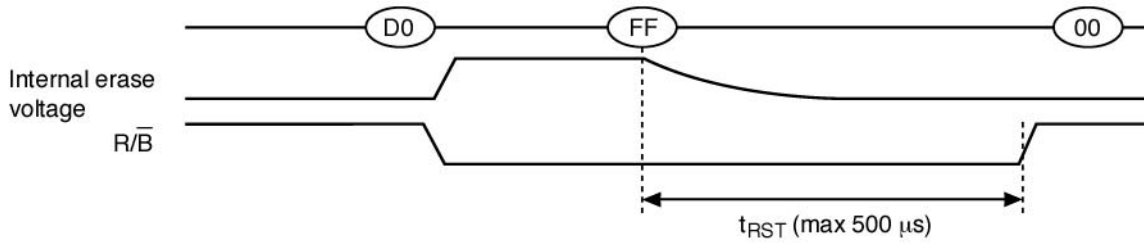


Figure 4-14 When a Reset Command (FFH) is Input During Erasing

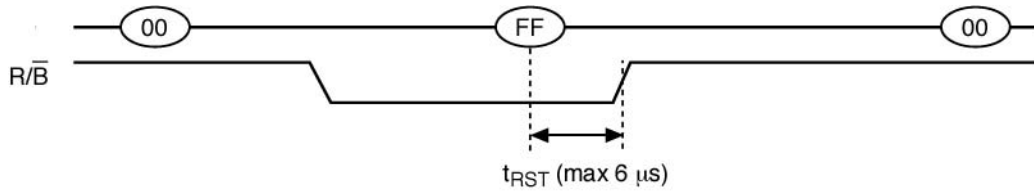


Figure 4-15 When a Reset Command (FFH) is Input During Read Operation

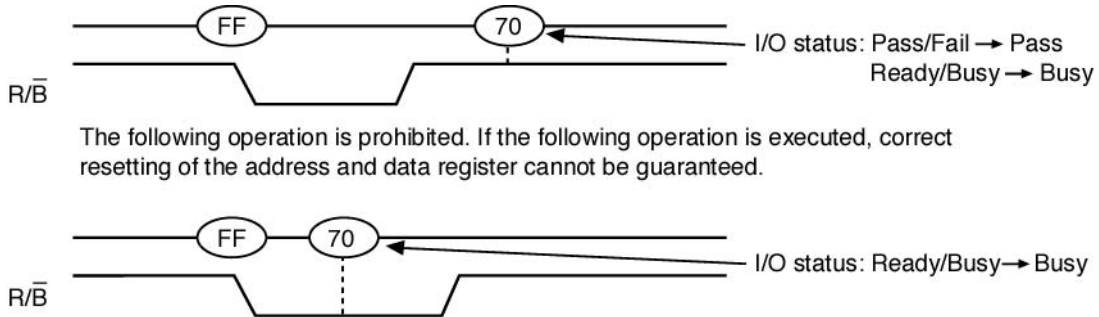


Figure 4-16 When a Status Read Command (70H) is Input After a Reset

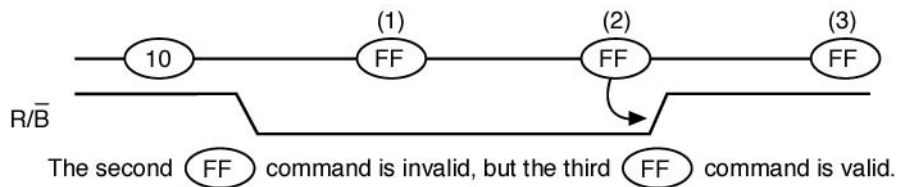
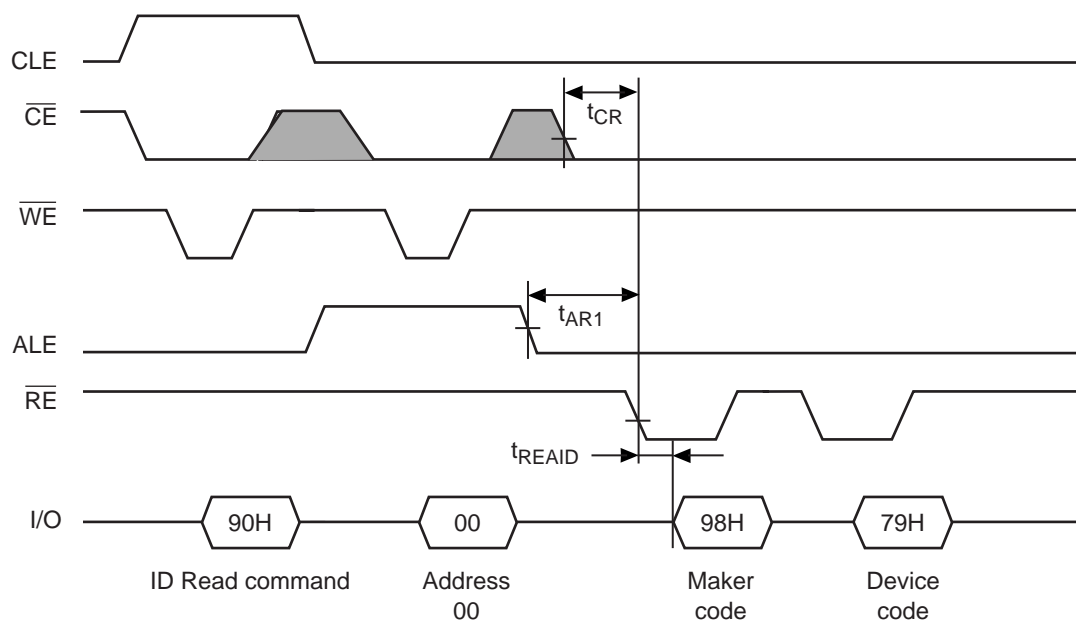


Figure 4-17 When Two or More Reset Commands are Input in Succession

4.12 ID Read

There are ID codes which identify the device type and the manufacturer. The ID codes can be read under the following timing conditions:



For the specifications of the access times t_{READ} , t_{CR} and t_{AR1} refer to the AC Characteristics.

Figure 4-18 ID Read (1) Timing

Table 4-4 Code Table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker Code	1	0	0	1	1	0	0	0	98H
Device Code	0	1	1	1	1	0	0	1	79H

5.0 Application Notes and Comments

5.1 Prohibition of Unspecified Commands

The operation commands are listed in Table 3-3. Input of a command other than those specified in Table 3-3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

5.2 Restriction of Commands While in Busy State

During the Busy state, do not input any command except 70H, 71H or FFH.

5.3 Pointer Control for 00H, 01H and 50H

The device has three Read modes which set the destination of the pointer. Table 5-1 shows the destination of the pointer, and Figure 5-1 is a block diagram of their operations.

Table 5-1 Pointer Destination

Read Mode	Command	Pointer
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527

The pointer is set to region A by the 00H command, to region B by the 01H command, and to region C by the 50H command. For example, the 00H command must be input to set the pointer back to region A when the pointer is pointing to region C. To program region C only, set the start point to region C using the 50H command.

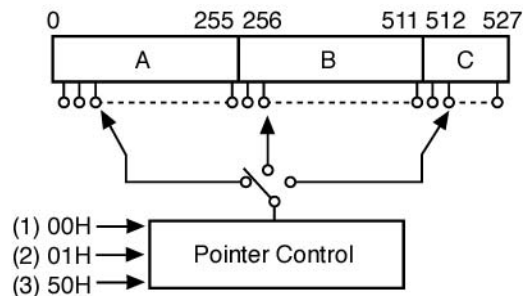


Figure 5-1 Pointer Control

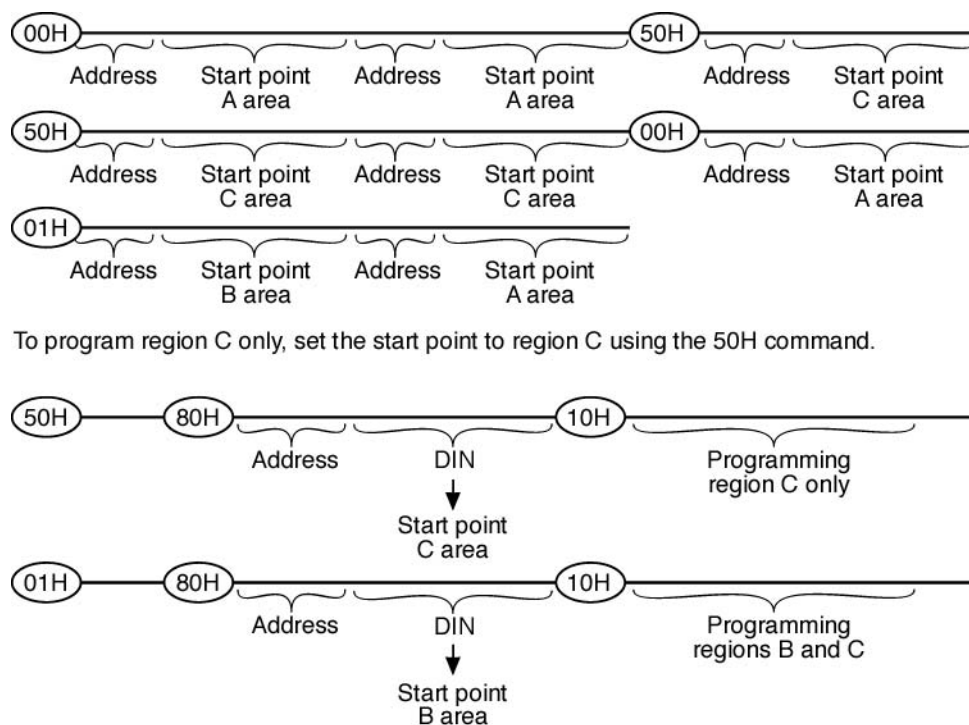
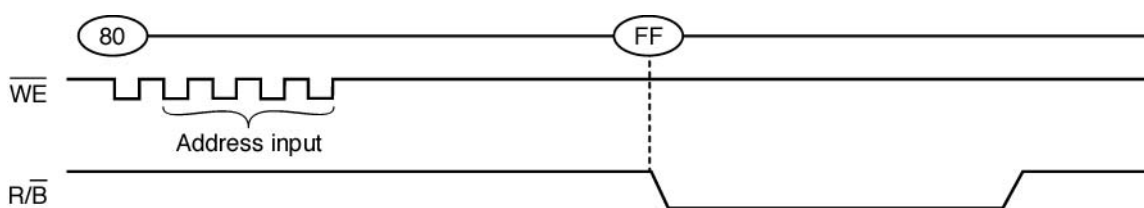


Figure 5-2 Example of How to Set the Pointer

5.4 Acceptable Commands After Serial Input Command 80H

Once the Serial Input command 80H has been input, do not input any command other than the Program Execution command 10H, 11H or 15H or the Reset command FFH.



If a command other than 10H, 11H, 15H or FFH is input, the Program operation is not performed.



Figure 5-3 Serial Input Command

5.5 Status Read During a Read Operation

The device status can be read out by inputting the Status Read command 70H in Read mode. Once the device has been set to Status Read mode by a 70H command, the device will not return to Read mode. Therefore, a Status Read during a Read operation is prohibited. However, when the Read command 00H is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

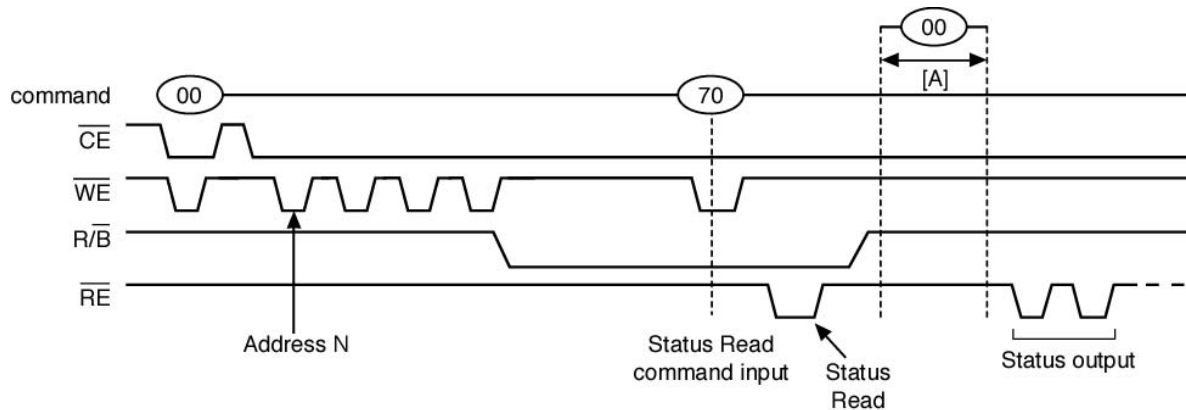


Figure 5-4 Status Read During a Read Operation

5.6 Auto-Programming Failure

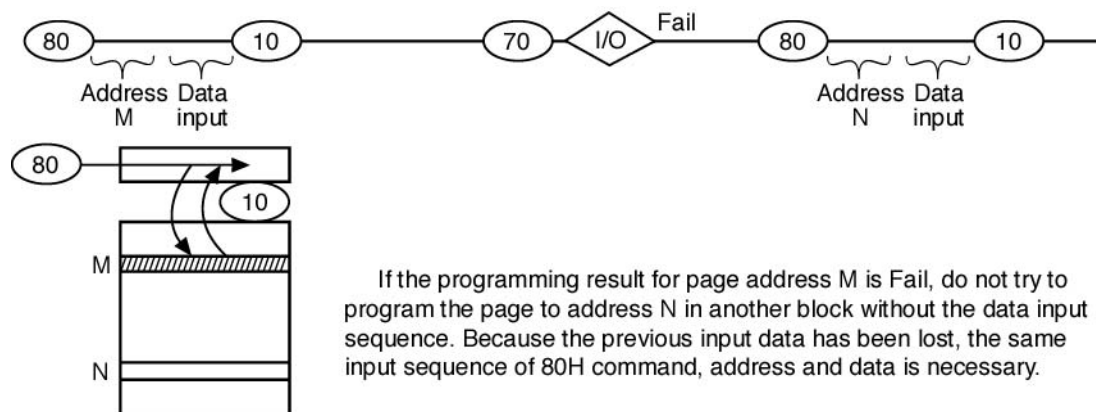


Figure 5-5 Auto-programming Failure

5.7 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block. Random page address input is prohibited.

5.8 R/\bar{B} : Termination for the Ready/Busy Pin (R/\bar{B})

A pull-up resistor needs to be used for termination because the R/\bar{B} buffer consists of an open drain circuit.

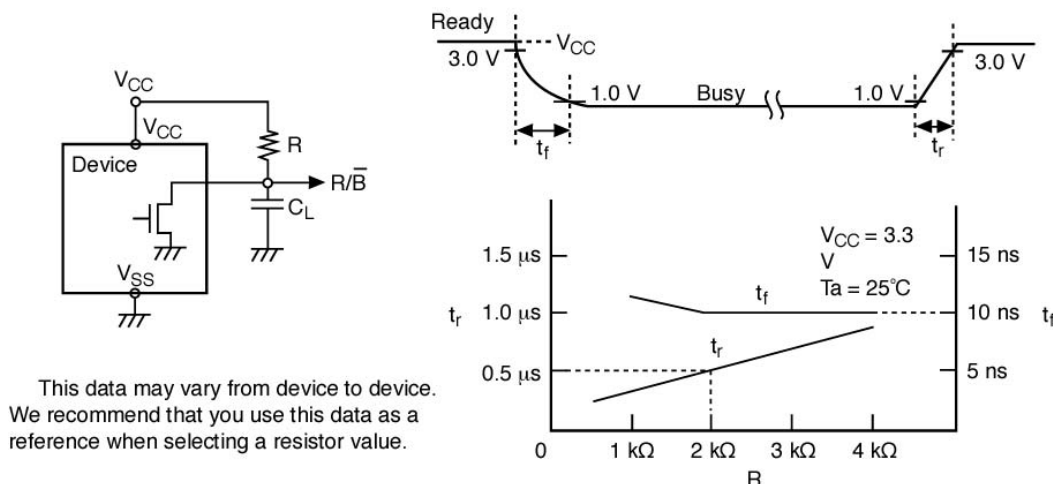


Figure 5-6 Termination of the Ready/Busy Pin

5.9 Status After Power-on

The following sequence is necessary because some input signals may not be stable at power-on.

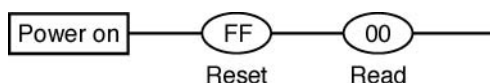


Figure 5-7 Status After Power-on

5.10 Power-on/off Sequence

The \overline{WP} signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary:

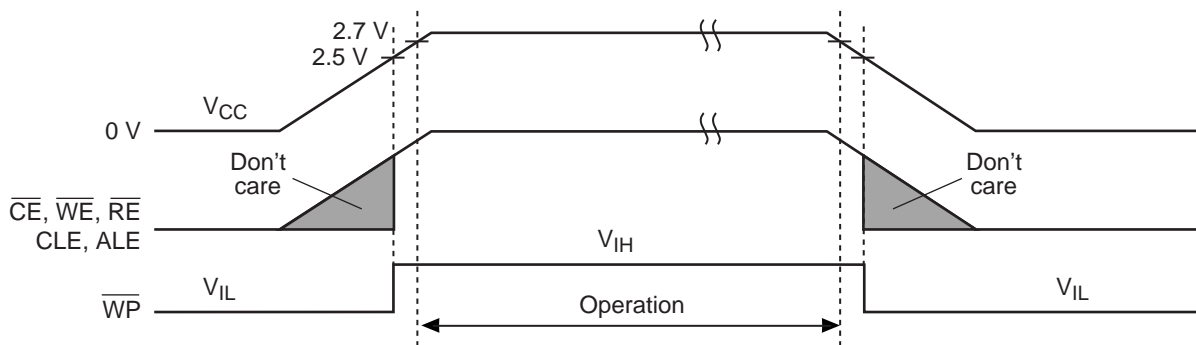


Figure 5-8 Power-on/off Sequence

5.11 Note Regarding the \overline{WP} Signal

The Erase and Program operations are automatically reset when \overline{WP} goes Low. The operations are enabled and disabled as follows:

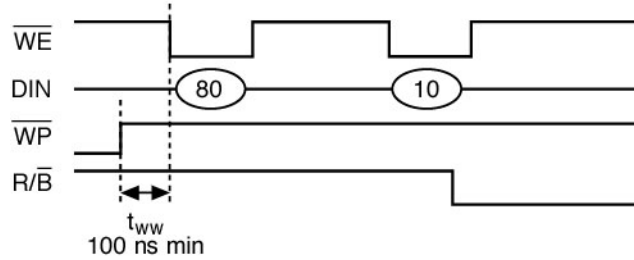


Figure 5-9 Enable Programming

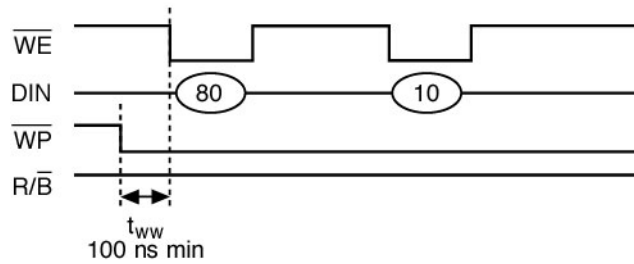


Figure 5-10 Disable Programming

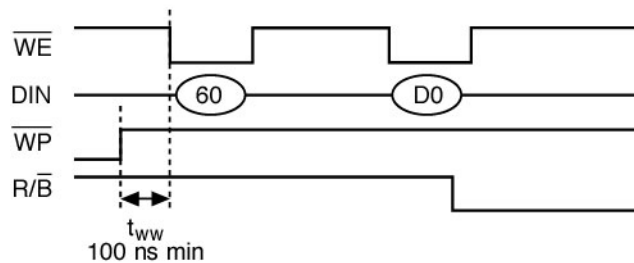


Figure 5-11 Enable Erasing

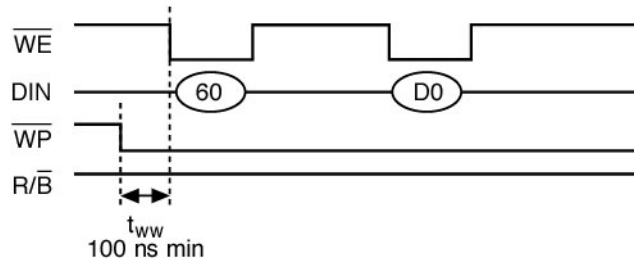


Figure 5-12 Disable Erasing

5.12 When Five Address Cycles are Input

Although the device may read in a fifth address, it is ignored inside the chip.

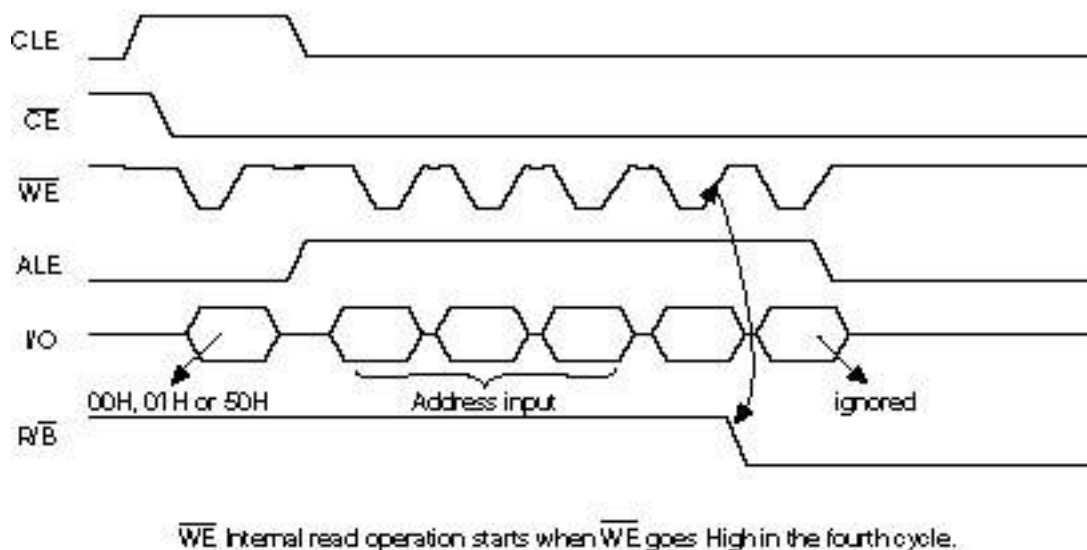


Figure 5-13 Read Operation

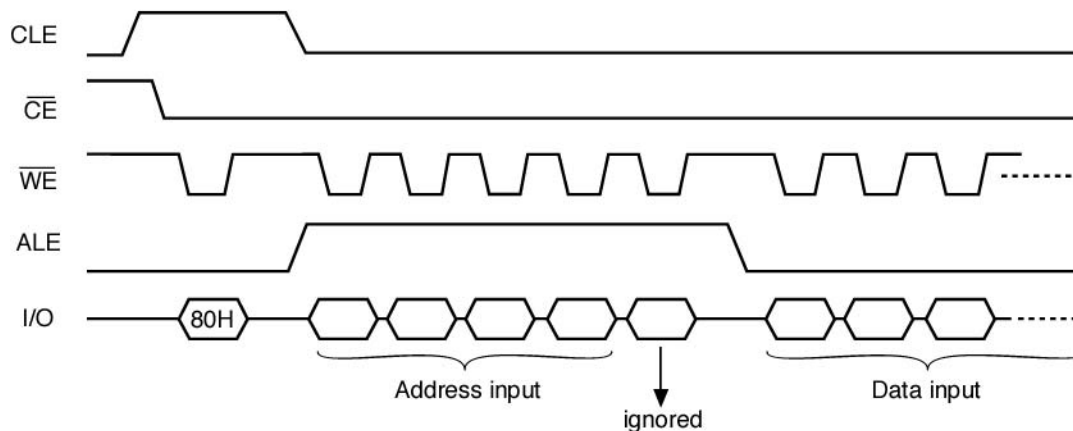


Figure 5-14 Program Operation

5.13 Several Programming Cycles on the Same Page (Partial Page Program)

A page can be divided into a maximum of three segments. Each segment can be programmed individually as follows:

(SSFDC Forum specification permits up to MAX 2 times: The second write should be in 16Byte area of 512+16Byte.)

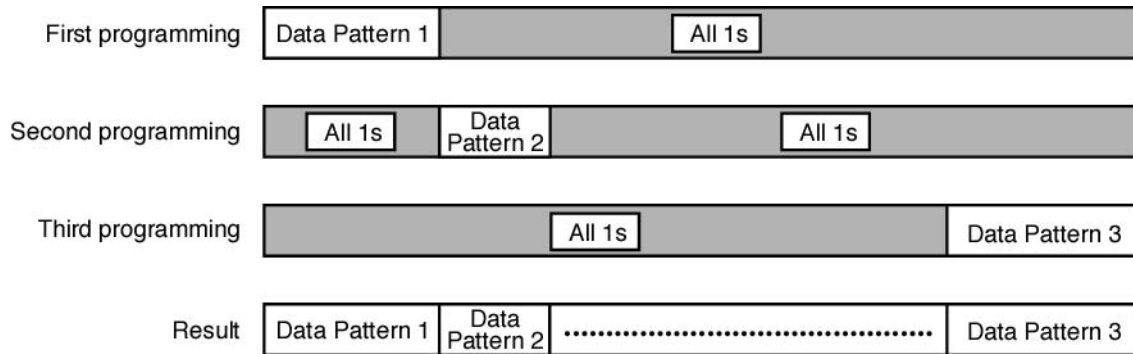


Figure 5-15 Partial Page Program

5.14 Note Regarding the \overline{RE} Signal

The internal column address counter is incremented synchronously with the \overline{RE} clock in Read mode. Therefore, once the device has been set to Read mode by an 00H, 01H or 50H command, the internal column address counter is incremented by the \overline{RE} clock independently of the address input timing. If the \overline{RE} clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to the following figure.) Hence the \overline{RE} clock input must start after the address input.

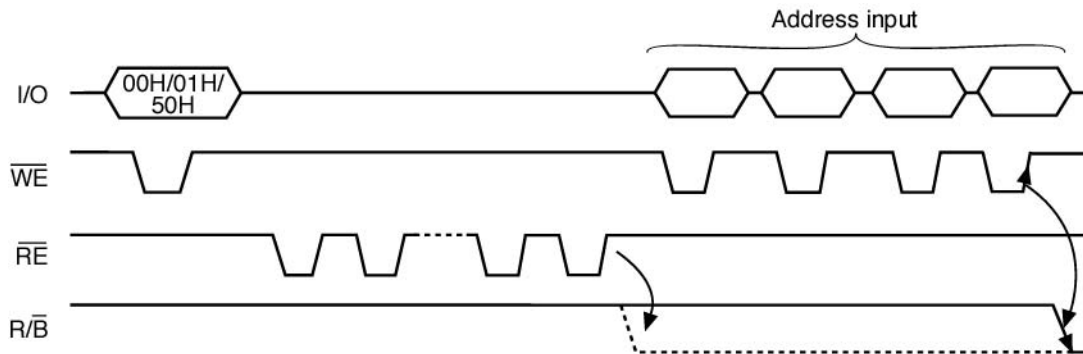


Figure 5-16 Internal Read Operation (Array to Register)

5.15 Invalid Blocks (Bad Blocks)

This product occasionally contains unusable blocks. Therefore, the following issues must be recognized:

- Referring to the Block status area in the redundant area allows the system to detect bad blocks in accordance with the physical data format issued by the SSFDC Forum. Detect the bad blocks by checking the Block Status Area at the system power-on, and do not access the bad blocks in the following routine. The number of valid blocks at the time of shipment is shown in the following table.

Table 5-2 Number of Valid Blocks

	Min.	Max.	Unit
Valid (Good) Block Number	8032	8192	Block

*: SSFDC Forum Spec. : 1002 MIN per Zone (each 16 k Bytes)

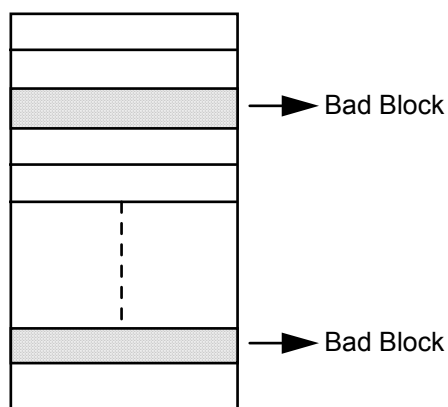
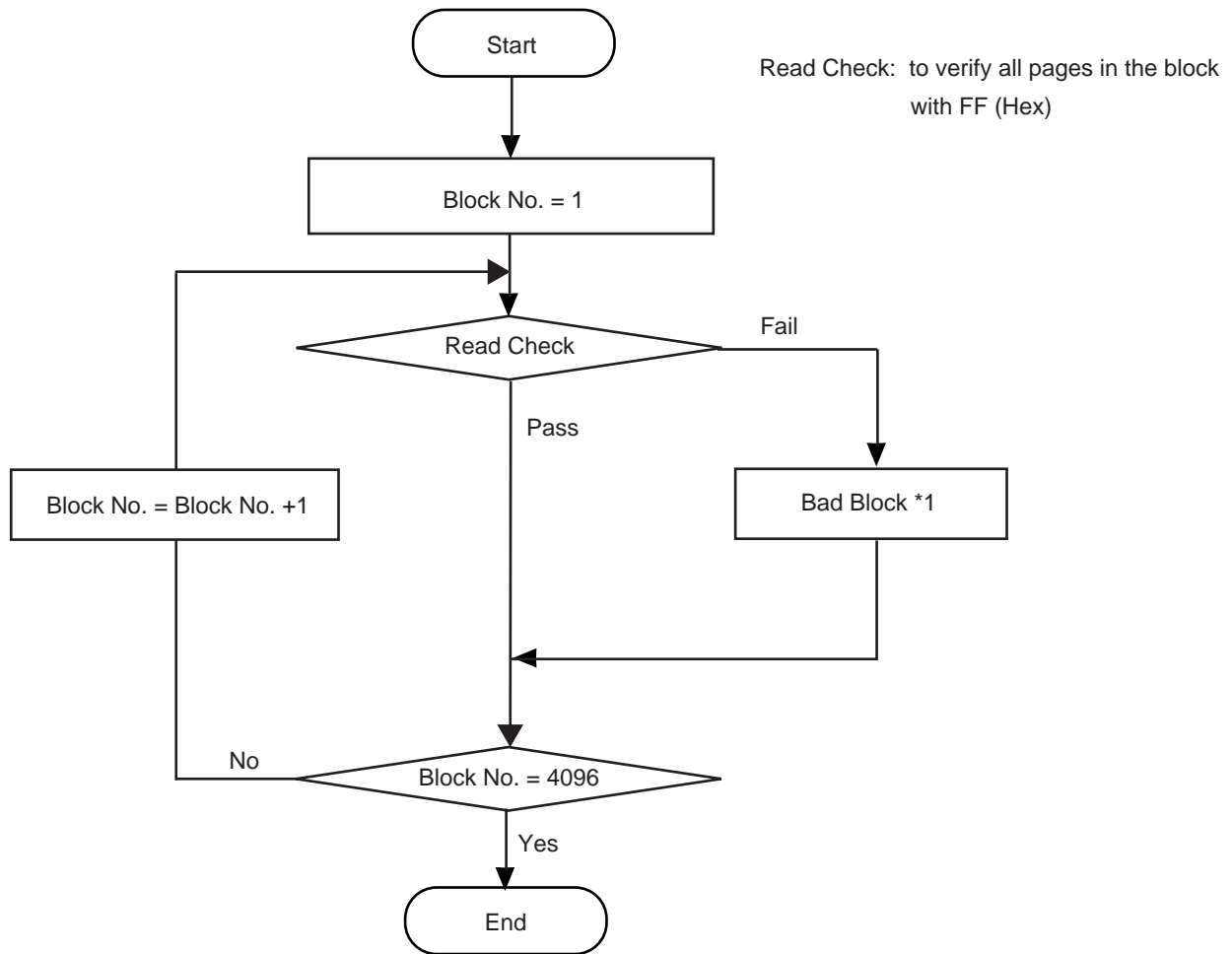


Figure 5-17 Bad Blocks in Array



*1: No erase operation is allowed to detected bad blocks.

Figure 5-18 Bad Block Test Flow

5.16 Failure Phenomena for Program and Erase Operations

The device may fail during a Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.

Table 5-3 Failure Modes

Failure Mode		Detection and Counter Measure Sequence
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure	(1) Block Verify after Program → Retry
	"1 to 0"	(2) ECC

- ECC: Error Correction Code
- Block Replacement

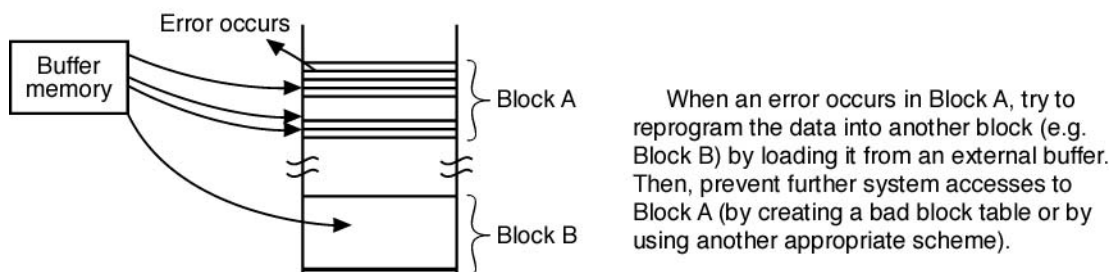


Figure 5-19 Program Fail Block Replacement

5.17 Chattering of Connector

There may be contact chattering when the SmartMedia Card is inserted or removed from a connector. This chattering may cause damage to the data in the SmartMedia Card. Therefore, sufficient time must be allowed for contact bouncing to subside when a system is designed with SmartMedia™.

- The SmartMedia Card is formatted to comply with the Physical and Logical Data Format of the SSFDC Forum at the time of shipping.

6.0 Handling Precautions

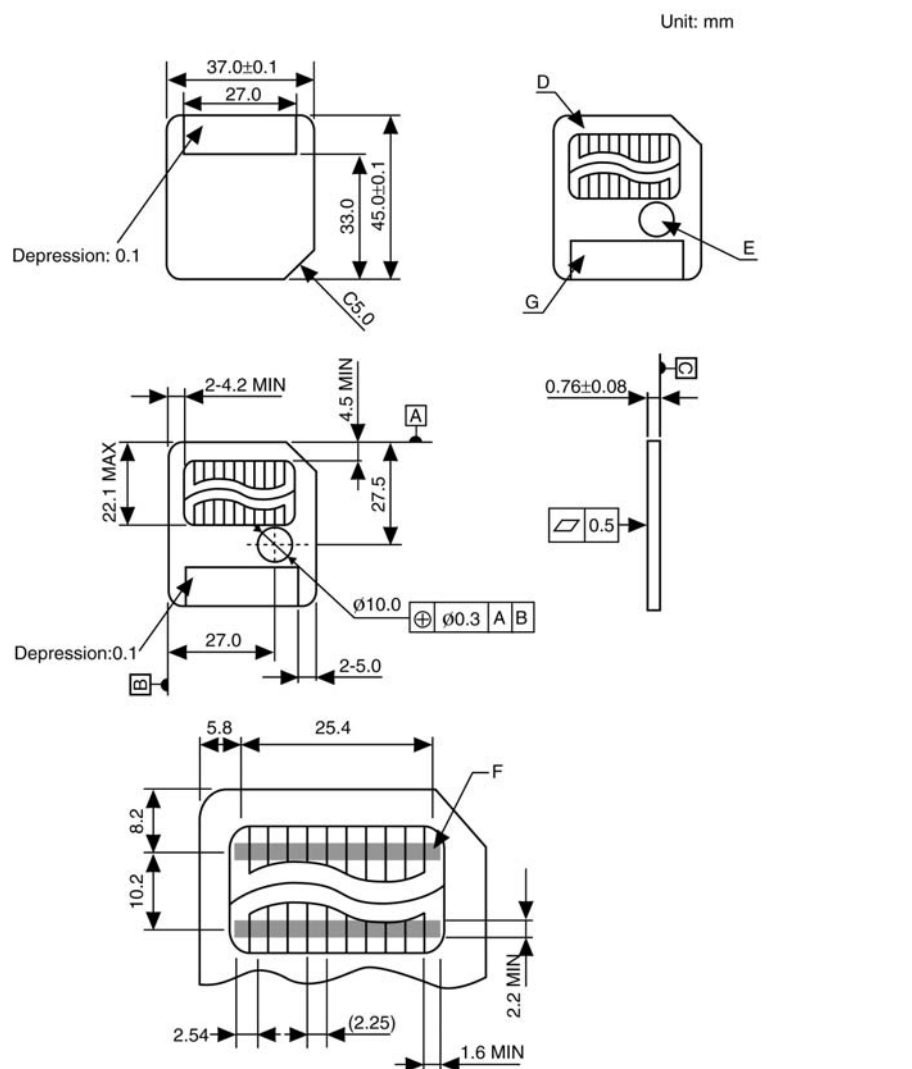
The following precautions should be observed when handling the SanDisk SmartMedia Card:

- (1) Avoid using the SmartMedia Card when the battery is low.
- (2) When writing to the card, wait for the operation to complete before removing the card.
- (3) The card is designed to fit easily into the system one way only. Do not force it into the slot.
- (4) Do not bend the card.
- (5) Do not subject the card to sudden impact.
- (6) Avoid touching the connectors so as to avoid damage from static electricity. This card should be kept in the antistatic film case when not in use.

7.0 Package Dimensions

7.1 SmartMedia Card Dimensions

The SanDisk SmartMedia Card dimensions are shown below in Figure 7-1.



E: Write-protect Area

The area has a diameter of 10.0 mm and it is indicated with a mark or depression 0.1 mm deep.

F: Contact Area

Located over the electrode block (the contact board), the gray section is the area directly in contact with the connector. Contact with the connector is ensured for this area. The variations in distance between the contact area and the card surface at Part D do not exceed 0.1 mm (*).

G: Index area

If not otherwise specified, the dimensional error is ± 0.2 mm.

(*) = Reference value

Figure 7-1 SmartMedia Card Dimensions

Ordering Information and Technical Support

This page has been left blank intentionally.

Ordering Information

To order SanDisk products directly from SanDisk, call 408-542-0595.

SmartMedia Card

Model SDSM-128-101-01 128.0 MB

Technical Support Services

Direct SanDisk Technical Support

Call SanDisk Applications Engineering at 408-542-0405 for technical support.

SanDisk Worldwide Web Site

Internet users can obtain technical support and product information along with SanDisk news and much more from the SanDisk Worldwide Web Site, 24 hours a day, seven days a week. The SanDisk Worldwide Web Site is frequently updated. Visit this site often to obtain the most up-to-date information on SanDisk products and applications. The SanDisk Web Site URL is <http://www.sandisk.com>.

SanDisk Sales Offices

This page has been left blank intentionally.

SanDisk Worldwide Sales Offices

Americas

SanDisk Corporate Headquarters

140 Caspian Court
Sunnyvale, CA 94089-9820
408-542-0500
FAX 408-542-0503
<http://www.sandisk.com>

Sales Offices

Western Region USA

408-542-0730
FAX 408-542-0403

Eastern Region USA & Canada

603-882-0888
FAX 603-882-2201

Central & Southern Region USA

614-760-3700
FAX 614-760-3701

Latin & South America

407-667-4880
FAX 407-667-4834

Europe

SanDisk GmbH

Karlsruher Str. 2C
D-30519 Hannover, Germany
49-511-8759185
FAX 49-511-8759187

SanDisk Northern Europe

Videroegaten 3 B
S-16440 Kista
Sweden
46-(0)8-75084-63
FAX 46-(0)8-75084-26

SanDisk Central Europe

Rudolf-Diesel-Str. 3
40822 Mettmann
Germany
49-(0)2104-953433
FAX 49-(0)2104-953434

Japan

SanDisk K.K.

8F Nisso Bldg. 15
2-17-19 Shin-Yokohama, Kohoku-ku
Yokohama 222-0033, Japan
81-45-474-0181
FAX 81-45-474-0371

Asia/Pacific Rim

89 Queensway, Lippo Center
Tower II, Suite 4104
Admiralty, Hong Kong
852-2712-0501
FAX 852-2712-9385

To order SanDisk products directly from SanDisk,
call 408-542-0595.

This page has been left blank intentionally.

Limited Warranty

I. WARRANTY STATEMENT

SanDisk warrants its products to be free of any defects in materials or workmanship that would prevent them from functioning properly for one year from the date of purchase. This express warranty is extended by SanDisk Corporation.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of SanDisk's responsibilities regarding the SanDisk SmartMedia Card. In satisfaction of its obligations hereunder, SanDisk, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

SanDisk's products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within one year of purchase, SanDisk will have the option of repairing or replacing the defective product, if the following conditions are met:

- A. The defective product is returned to SanDisk for failure analysis as soon as possible after the failure occurs.
- B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.
- C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to SanDisk under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

SanDisk reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

SanDisk may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, SanDisk also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

Limited Warranty

IV. RECEIVING WARRANTY SERVICE

According to SanDisk's warranty procedure, defective product should be returned only with prior authorization from SanDisk Corporation. Please contact SanDisk's Customer Service department at 408-542-0595 with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, SanDisk will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

SanDisk Corporation
Attn: RMA Returns
(Reference RMA or PRA #)
140 Caspian Court
Sunnyvale, CA 94089

V. STATE LAW RIGHTS

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES, OR LIMITATION ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU. This warranty gives you specific rights and you may also have other rights that vary from state to state.