```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 14.12.2022 11:22:20
-- Design Name:
-- Module Name: Dvas - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Dvas is
--  Port ( );
Port ( D : in STD_LOGIC;
       CLK : in STD_LOGIC;
       Q : out STD_LOGIC;
       Qn : out STD_LOGIC);
end Dvas;

architecture Behavioral of Dvas is

begin
   process (Clk)
      begin
         if Clk'event and Clk = '1' then
            Q<=D;
            Qn<=not D;
```

```
        end if;
   end process;

end Behavioral;
```