```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 14.12.2022 11:33:06
-- Design Name:
-- Module Name: muxvas - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity muxvas is
--  Port ( );
Port ( I : in STD_LOGIC_VECTOR (7 downto 0);
       S : in STD_LOGIC_VECTOR (2 downto 0);
       Y : out STD_LOGIC);
end muxvas;

architecture Behavioral of muxvas is

begin

   process (I, S)
      begin
         case S is
            when "000" => Y <= I(0);
            when "001" => Y <= I(1);
```

```
            when "010" => Y <= I(2);
            when "011" => Y <= I(3);
            when "100" => Y <= I(4);
            when "101" => Y <= I(5);
            when "110" => Y <= I(6);
            when "111" => Y <= I(7);
            when others => Y <= 'X';
        end case;
   end process;

end Behavioral;
```