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-- Company:
-- Engineer:
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-- Create Date: 14.12.2022 13:35:34
-- Design Name:
-- Module Name: shift6vas - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
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-- Dependencies:
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-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;


entity shift6vas is
    Port ( I : in STD_LOGIC_VECTOR (5 downto 0);
           SEL : in STD_LOGIC_VECTOR (2 downto 0);
           RESET : in STD_LOGIC;
           CLK : in STD_LOGIC;
           O : out STD_LOGIC_VECTOR (5 downto 0));
end shift6vas;

architecture Behavioral of shift6vas is

COMPONENT muxvas
 PORT(
      I : IN std_logic_vector(7 downto 0);
      S : IN std_logic_vector(2 downto 0);
      Y : OUT std_logic
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     );
END COMPONENT;

COMPONENT Dvas
PORT(
     D : IN std_logic;
     CLK : IN std_logic;
     Q : OUT std_logic;
     Qn : OUT std_logic
    );
END COMPONENT;

COMPONENT faddervas
Port ( X : in STD_LOGIC;
       F : in STD_LOGIC;
       Cin : in STD_LOGIC;
       S : out STD_LOGIC;
       Co : out STD_LOGIC);
END COMPONENT;

signal D5, D4, D3, D2, D1, D0, Dn5, Dn4, Dn3, Dn2, Dn1, Dn0, M5, M4, M3, M2, M1,
M0, Q5, Q4, Q3, Q2, Q1, Q0, a, b, c, d, e, Cout  : std_logic
;

begin
muxvas_0: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => RESET,
       I(2) => D5,
       I(3) => D1,
       I(4) => D1,
       I(5) => Dn0,
       I(6) => Q0,
       I(7) => I(0),
       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M0
     );

muxvas_1: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => D0,
       I(2) => D0,
       I(3) => D2,
       I(4) => D2,
       I(5) => Dn1,
       I(6) => Q1,
       I(7) => I(1),
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       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M1
     );

muxvas_2: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => D1,
       I(2) => D1,
       I(3) => D3,
       I(4) => D3,
       I(5) => Dn2,
       I(6) => Q2,
       I(7) => I(2),
       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M2
     );

muxvas_3: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => D2,
       I(2) => D2,
       I(3) => D4,
       I(4) => D4,
       I(5) => Dn3,
       I(6) => Q3 ,
       I(7) => I(3),
       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M3
     );

muxvas_4: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => D3,
       I(2) => D3,
       I(3) => D5,
       I(4) => D5,
       I(5) => Dn4,
       I(6) => Q4,
       I(7) => I(4) ,
       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M4
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    );

muxvas_5: muxvas PORT MAP (
       I(0) => RESET,
       I(1) => D4,
       I(2) => D4,
       I(3) => D0,
       I(4) => D5,
       I(5) => Dn5,
       I(6) => Q5,
       I(7) => I(5) ,
       S(0) => SEL(0),
       S(1) => SEL(1),
       S(2) => SEL(2),
       Y => M5
    );

Dvas_0: Dvas PORT MAP (
D => M0,
CLK => CLK,
Q => D0,
Qn => Dn0
);

Dvas_1: Dvas PORT MAP (
D => M1,
CLK => CLK,
Q => D1,
Qn => Dn1
);

Dvas_2: Dvas PORT MAP (
D => M2,
CLK => CLK,
Q => D2,
Qn => Dn2
);

Dvas_3: Dvas PORT MAP (
D => M3,
CLK => CLK,
Q => D3,
Qn => Dn3
);

Dvas_4: Dvas PORT MAP (
D => M4,
CLK => CLK,
Q => D4,
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Qn => Dn4
);

Dvas_5: Dvas PORT MAP (
D => M5,
CLK => CLK,
Q => D5,
Qn => Dn5
);


faddervas0: faddervas PORT MAP (
X => Dn0,
F => '1',
Cin => '0',
S => Q0,
Co => a
);
faddervas1: faddervas PORT MAP (
X => Dn1,
F => '0',
Cin => a,
S => Q1,
Co => b
);
faddervas2: faddervas PORT MAP (
X => Dn2,
F => '0',
Cin => b,
S => Q2,
Co => c
);
faddervas3: faddervas PORT MAP (
X => Dn3,
F => '0',
Cin => c,
S => Q3,
Co => d
);
faddervas4: faddervas PORT MAP (
X => Dn4,
F => '0',
Cin => d,
S => Q4,
Co => e
);
faddervas5: faddervas PORT MAP (
X => Dn5,
F => '0',
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Cin => e,
S => Q5,
Co => Cout
);

O(5) <= D5;
O(4) <= D4;
O(3) <= D3;
O(2) <= D2;
O(1) <= D1;
O(0) <= D0;

end Behavioral;
```