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-- Company:
-- Engineer:
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-- Create Date: 14.12.2022 23:07:01
-- Design Name:
-- Module Name: shift6vas_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity shift6vas_tb is
--  Port ( );
end shift6vas_tb;

architecture Behavioral of shift6vas_tb is

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT shift6vas
Port ( I : in STD_LOGIC_VECTOR (5 downto 0);
       SEL : in STD_LOGIC_VECTOR (2 downto 0);
       RESET : in STD_LOGIC;
       CLK : in STD_LOGIC;
       O : out STD_LOGIC_VECTOR (5 downto 0));
END COMPONENT;
```

```
--Inputs
signal I : std_logic_vector(5 downto 0) := (others => '0');
signal SEL : std_logic_vector(2 downto 0) := (others => '0');
signal RESET : std_logic := '0';
signal CLK : std_logic := '0';

--Outputs
signal O : std_logic_vector(5 downto 0);

-- Clock period definitions
constant CLK_period : time := 15 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
uut: shift6vas PORT MAP (
       I => I,
       SEL => SEL,
       RESET => RESET,
       CLK => CLK,
       O => O
     );

-- Clock process definitions
CLK_process :process
begin
   CLK <= '0';
   wait for CLK_period/2;
   CLK <= '1';
   wait for CLK_period/2;
end process;

-- Stimulus process
stim_proc: process
begin
   -- hold reset state for 100 ns.
   wait for 50 ns;

   --wait for CLK_period*10;

   -- insert stimulus here
   SEL <= "000";-- synchronous reset
   I <= "101101"; -- number 45d/2d to be loaded
   SEL <= "111"; -- load number 45d
   wait for CLK_period;
   SEL <= "001"; -- shift left zero padding. Q=011010/1a
   wait for CLK_period;
   SEL <= "010"; -- rotate shift left. Q=34
   wait for CLK_period;
```

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   SEL <= "011"; -- rotate shift right. Result should be 1a
   wait for CLK_period;
   SEL <="100"; -- sign shift right.Q=d
   wait for CLK_period;
   SEL <= "101"; -- 1's complement. Q=32
   wait for CLK_period;
   SEL <= "110"; -- 2'S complement. Q=e
   wait for CLK_period;


   wait;
end process;
end Behavioral;
```