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----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 14.12.2022 11:26:08
-- Design Name:
-- Module Name: Dvas_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Dvas_tb is
--  Port ( );
end Dvas_tb;

architecture Behavioral of Dvas_tb is
COMPONENT Dvas
PORT(
     D : IN std_logic;
     CLK : IN std_logic;
     Q : OUT std_logic;
     Qn : OUT std_logic
     );
END COMPONENT;


--Inputs
```

```
signal D : std_logic := '0';
signal CLK : std_logic := '0';

--Outputs
signal Q : std_logic;
signal Qn : std_logic;

-- Clock period definitions
constant CLK_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
uut: Dvas PORT MAP (
       D => D,
       CLK => CLK,
       Q => Q,
       Qn => Qn
      );

-- Clock process definitions
CLK_process :process
begin
CLK <= '0';
wait for CLK_period/2;
CLK <= '1';
wait for CLK_period/2;
end process;


-- Stimulus process
stim_proc: process
begin
-- hold reset state for 100 ns.
wait for 12.5 ns;

--wait for CLK_period*10;

-- insert stimulus here
D<='0';
wait for CLK_period*1.5;
D<='1';
wait for CLK_period*2.5;
D<='0';


wait;
end process;
```

```
end Behavioral;
```