CS & IT ENGINEERING

Computer Organization & Architecture

Cache Memory

DDP

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01 Question

02 Discussion

Q.1

Consider a processor that can support a maximum memory of 8GB, where the memory is word-addressable (a word consists of 2 bytes). Then the size of the address bus of the processor is at least _____ bits. [MCQ]

A. 31

B. 32

C. 33

D. 34

Ans (B)

Memory Size = 8GByte

1Word Size = 2 Byte

Memory is Word Addressable

Memory = 8GB

$\frac{8GB}{2Byte}$ Words

4G Words

$2^2 \cdot 2^{30}$ Words $\Rightarrow$ 2^{32} Word

or

8GB

4G × 2B

4G Words

Address = 32 bit

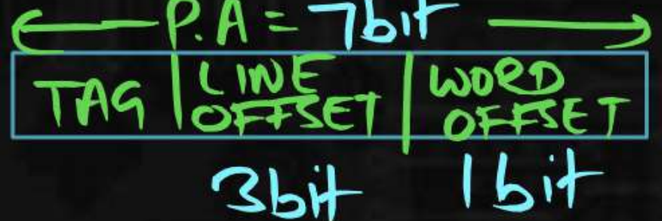
Ans

Q.2

Assume a direct mapped cache having 8 cache lines, each cache line consists of 2 words and each word is of one byte. The address bus consists of 7 bits, then the tag field of the cache consists of __3__ bits. [NAT]

Soln

Ans(3)



Line(Block) Size = 2words

1Word Size = 1Byte

Block Size = 2Byte

Word offset (W.O) = 1 bit

#LINES = 8

L.O = 3bit $\log_2 8$ or $2^n = 8$

P.A = 7bit

TAG = 7 − (3+1)

= 7 − 4

TAG = 3bit Ans

Q.3

Assume a 32-bit addressable physical memory and 2 MB cache block of size 8 kB each, then how many bits are required in the tag field of the cache address if the cache is 4-way set associative

[NAT]

13 Ans

Ans (13)

P.A = 32 bit

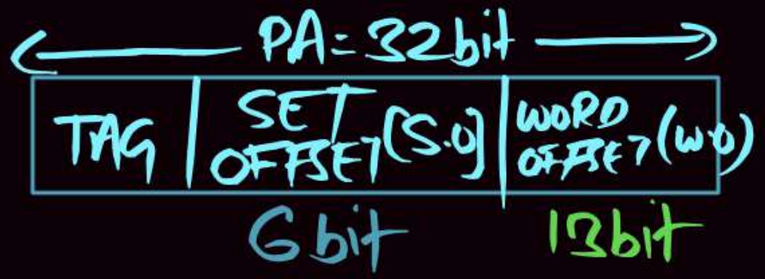
Cache Size = 2mB

Block size = 8kB

4 Way Set Associative Cache

TAG bits ?

Soln



$TAG = 32 - (6 + 13)$

TAG = 13 bit Ans

Block size = 8kByte = 2^{13} B

word offset = $\log_2$(8kB)

W.O = 13 bit

$\#LINES = \frac{Cache\ size}{Block\ size} \Rightarrow \frac{2mB}{8kB} \Rightarrow \frac{2^{21}B}{2^{13}B} = 2^8$

$\#SET = \frac{\#LINES}{N\text{-}way} = \frac{2^8}{2^2} = 2^6$ Set

S.O = 6 bit

Q.4

Consider a 16-Kbyte cache with the following features, each block will hold 32 bytes of data (not including tag, valid, etc ...), The cache would be 2-way set associative, physical addresses are 32 bits and data is addressed to the word and words are of 32 bits long. Then how many blocks would be in this cache and how many bits of tag are stored with each block entry? [MCQ]

A. 512, 19

B. 512, 22

C. 256, 20

D. 512, 21

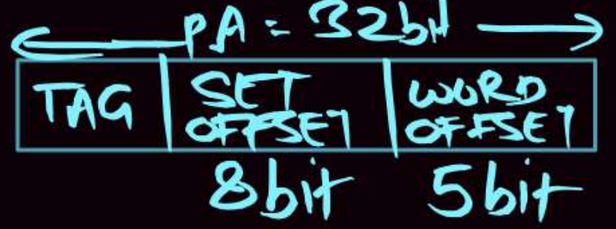
Ans (A)

Cache Size = 16kB

Block Size = 32Byte

P.A = 32 bit

2 way Set Associative



$TAG = 32 - (8+5)$

$= 32 - 13$

TAG = 19 bits Ans

Block Size = 32Byte $= 2^5$ Byte

Word offset (W.O) = 5bit

$\#LINES\ (\#CM\ Blocks) = \frac{CM\ Size}{Block\ Size} \Rightarrow \frac{16kB}{32B} \Rightarrow \frac{2^{14}B}{2^5B}$

$\#LINES\ (\#CM\ Blocks) = 2^9 = 512$ Lines Ans

2 Way set Associative

$\#SETS = \frac{\#LINES}{N\text{-}ways} = \frac{2^9}{2^1} = 2^8$ Set

set offset [5:0] = 8bit

Q.5

Consider a 16 KB, two-way associative cache with 32-Byte cache line and a 64 bit address space, there will be p bits used for index. Let suppose if that same cache were fully associative, you need q bits to be used for the index then the value for p + q = _____.

[MCQ]

A. 6

B. 7

C. 8

D. 9

Ans (c)

Cache Size = 16KB $= 2^{14}$ B

2 way Set Associative

Block Size = 32 Byte $= 2^5$ Byte

Physical address (P.A) = 64 bit

$\#LINES = \frac{\text{Cache size}}{\text{Block size}} = \frac{2^{14}}{2^5} = 2^9$ Lines

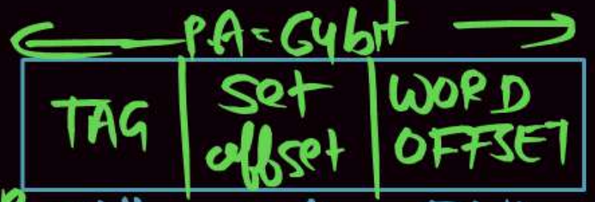
$\#SET = \frac{\#LINES}{\text{No. ways}} = \frac{2^9}{2^1} = 2^8$ Set

Set offset = 8 bit

P bit is used to Index the Cache in 2 way Set Associative (Point to Cache Set)

q bit is used to Index in fully Associative Mapping.

2 way Set Associative



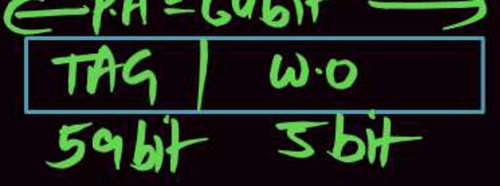
Set offset is used to Index the Cache in set Associative

$K \bmod S = i$

So P = 8 bit

$P_9 = 8 + 0 = 8$.

Fully Associative



Here No Mapping function. Mm Block Mapped to Any Cache Line (No Cache Indexing)

Each Cache Block have Comparator. q = 0

Q.6

Consider a system having 512KB, 16-way set associative L_2 cache with a 128 byte cache line size, Then how many cache lines are present? 4096

[NAT]

Ans (4096)

Cache Size = 512KB = 2^{19}B

16 Way Set Associative

CMLINE (Block) Size = 128Byte = 2^7B

$$\#LINES = \frac{CM\ Size}{Block\ Size}$$

$$\Rightarrow \frac{2^{19}B}{2^7B} = 2^{12}\ Lines = 4096$$

#LINES = 4096.

Q.7

Assume a cache with 32-bit address, 768 blocks and a block size of 128 bytes, tags are 17 bits then what is the associativity of the cache ___3___ ? Ans

[NAT]

Ans (3)

Physical address (P.A) = 32 bit

Block size = 128 Byte

Tag = 17 bit

#CM Blocks (LINES) = 768

What is the associativity ?

Block Size = 128 Byte = 2^7 Byte

Word offset = 7 bit

SET OFFSET = 32 − (17 + 7)

= 32 − 24

Set offset [S.0] = 8 bit

#SETS [Number of set] = 2^8 SET = 256 Set

$$\#SET = \frac{\#LINES\ (Blocks)}{N\text{-}way}$$

$$256 = \frac{768}{N\text{-}way}$$

$$N\text{-}way = \frac{768}{256} = 3$$ Ans

Q.8

Assume a direct mapped cache memory with 16 cache block (0 – 15) and a main memory having 256 blocks (0 to 255). Assume that, initially the cache did not have any memory block, Consider the following sequence of memory block references:

3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186 and 253, Then which memory blocks will be present in the cache after the above sequence of memory block reference?

[MCQ]

A. 2,3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186

B. 2,3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 181, 44, 186, 253

C. 2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191

Ans [C].

D. None of the above

3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186, 253.

CM LINE = 16 so K MOD N ⇒ K MOD 16

	MOD 16	LINE NO
3	% 16 =	3
180	% 16 =	4
43	% 16 =	11
2	% 16 =	2
191	% 16 =	15
881	% 16 =	1
190	% 16 =	14
14	% 16 =	14
181	% 16 =	5
44	% 16 =	12
186	% 16 =	10
253	% 16 =	13

Q.9

Assume the access patterns x, y, z, y, x where each letter corresponds to a unique ~~cache~~ MM block and also assume that there was no access to any block before this and all conflicts are random. Then what is the probability of the second access to x being a hit on a ~~direct mapped~~ Associative cache with 4 line (closet to)?

[MCQ]

K MOD 4 = i

A. 40%

B. 50%

C. 80%

D. 100%

Second Access of X is Hit

Ans (D)

X
Y
Z

Q.10 Which one is the fastest cache mapping function among the following? [MCQ]

Fastest & Expensive

A. Fully associative mapping — No Mapping function, Content Addressable.

B. Set associative mapping — K MOD S = i

C. Direct mapping → K MOD N = i → Simple But Very large No. of Conflict Miss

D. None of these

Ans (A)

Q.11

Suppose a cache has 70% hit ratio, an access time of 50 ns on a cache hit and an access time of 120 ns on a cache miss then what is the effective access time____(using hierarchical memory)

[MCQ]

A. 90 ns

B. 92 ns

C. 86 ns

D. 96 ns

EMAT

$T_{avg} = h * t_c + (1-h)(t_m + t_c)$

$\Rightarrow 0.7 \times 50 + (1-0.7)[120+50]$

$= 35 + (0.3) \times 170$

$= 35 + 51$

$= 86 \text{ nsec}$

Ans(C)

t_c: 50ns

t_m: 120ns

h: 0.7

Q.12

Suppose local hit rate for L_1 cache is 20% and the local hit rate for L_2 cache is also 30%. The hit time for the L_1 cache is 8 cycle, the hit time for L_2 cache is 20 cycles and access time for main memory is 30 cycles then what is average memory access time in cycle? (approximately)

[MCQ]

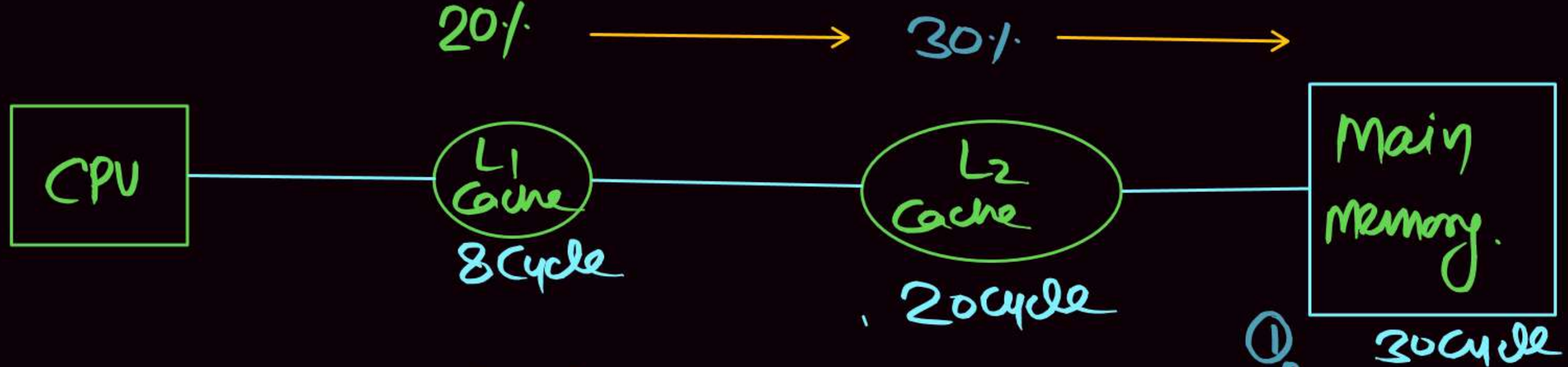
A. 41

B. 45

C. 46

D. 44

Ans (A)



$$T_{avg} = h_1 T_1 + (1-h_1) h_2 (T_2 + T_1) + (1-h_1)(1-h_2) \underset{①}{h_3} [T_m + T_2 + T_1]$$

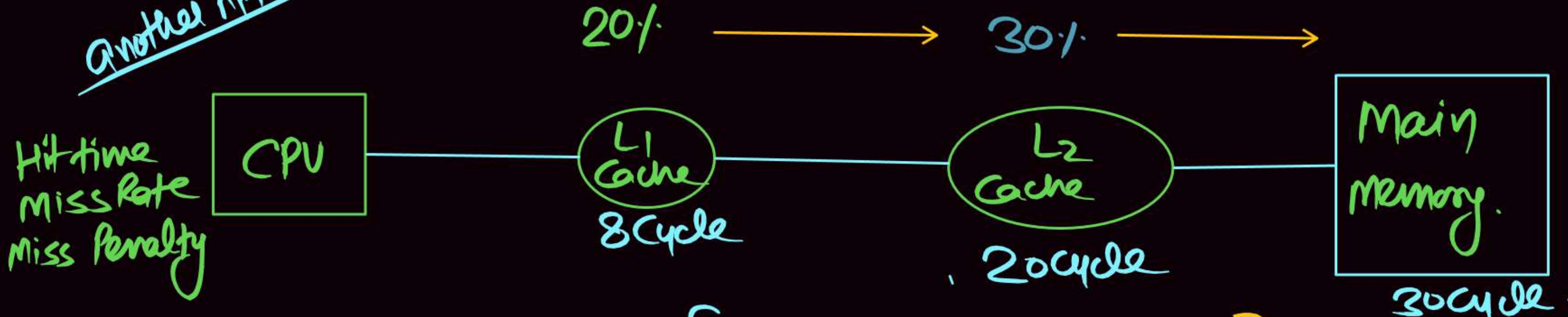
$$\Rightarrow .20 \times 8 + (1-.20) * .30 [20+8] + (1-.20)(1-.30)[30+20+8]$$

$$\Rightarrow 1.6 + (0.8) \times .30 [28] + (0.8)(0.7)(58)$$

$$1.6 + 6.72 + 32.48$$

$$40.8 = 41 \text{ Cycle}$$

Another Approach



$$T_{avg} = T_1 + [1-h_1]\left[T_2 + (1-h_2)\,T_m\right]$$

$$\Rightarrow 8 + (1-0.2)\,[20 + (1-0.3)\times 30]$$

$$\Rightarrow 8 + 0.8\,[20 + (0.7)*30) \Rightarrow 8 + 0.8\,[20+21]$$

$$= 8 + 0.8(41)$$

$$= 8 + 32.8$$

$$= 40.8 \approx 41 \text{ cycle.}$$

Q.13

Choose the correct statements from the following. [MSQ]

A. Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory.

B. Data is stored on temporary basis in cache memory.

C. Programs stored in cache takes more time to execute.

D. Cache memory has limited capacity.

Ans (B) & (D)

always → NO [if Simultaneous Access then Direct from MM
if Hierarchical Access first transfer MM to Cache then Cache to CPU.

more time → Less time.

Q.14

[MCQ]

Consider the following statements.

S_1: If size of the block is increased then compulsory misses can be reduced.

S_2 : If associativity of cache is increased then that can lead to increasing conflict misses.

A. Only S_1 is true

B. Only S_2 is true

C. Both S_1 and S_2 are true

D. Neither S_1 nor S_2 is true

Ans (A)

Compulsory Miss : Reduced by Increasing Cache Block Size

Capacity Miss : Increasing Cache Size (Capacity)

Conflict Miss : Increasing the associativity

Q.15

Consider a 128 word cache and the main memory is divided into 32 word blocks. The main memory access time is 50 μs / word and the cache access time is 20 μs/word. The hit ratio for read operation is 80% and for the write operation is 90%. Whenever a cache miss happens, associated block must be the brought from main memory to cache for both read and write operation. Let there be 40% references for write operations. If the write back updation policy is used and at any point of time 80% cache blocks are modified, then what is the T_{avg}? (upto 1 decimal in μ sec)

[NAT]

Ans (480.8)

[tc] Cache Access = 20 nsec/word ⇒ 1 Word give to CPU.

Main memory Access time = 50 nsec/word

32 Word Block.

$h_R = 80\% = 0.8$

$h_W = 90\% = 0.9$

80% Block is modified (Dirty bit set) ⇓ Write Back.

% Dirty = 0.8

Clean = 0.2

Read

$t_m = 50\ \text{nsec/word} \times 32\ \text{word}$

$t_m = 1600\ \text{nsec}$

$$T_{avg\,read} = h_R * t_c + (1-h_R)\left[\underset{\%\,Dirty}{\overset{Modified}{\overset{(Write\ Back)}{\downarrow}}}\left[t_m + t_m + t_c\right] + \underset{(1-0.80)}{\%\,Clean}\left[t_m + t_c\right]\right]$$

$$\Rightarrow 0.8 \times 20 + (1-0.8\left[0.8\left[1600+1600+20\right] + .20\left[1600+20\right]\right]$$

$$\Rightarrow 16 + 0.2\left[0.8(3220) + .20(1620)\right] \quad 2576 + 324$$

$$16 + 0.2 \times 2900$$

$$16 + 580$$

$$T_{avg\,read} = 596\ \text{nsec}$$

∴

[tc] Cache Access = 20 usec/word ⇒ 1 Word give to CPU.

Main memory Access time = 50 usec/word

32 Word Block.

$h_s = 80\% = 0.8$

$h_w = 90\% = 0.9$

80% Block is modified (Dirty bit set)

⇓

Write Back.

% Dirty = 0.8

Clean = 0.2

Write

$t_m = 50\ \text{usec/word} \times 32\ \text{word}$

$t_m = 1600\ \text{usec}$

$$T_{avg_{write}} = h_w * t_c + (1 - h_w)\left[\underset{\%\,\text{Dirty}}{\overset{\text{Modified}}{\overset{\text{Write Back}}{\downarrow}}}\left[t_m + t_m + t_c\right] + \underset{(1-0.80)}{\%\,\text{clean}}\left[t_m + t_c\right]\right]$$

Not modified

$$\Rightarrow 0.9 \times 20 + (1 - 0.9)\left[0.8\left[1600 + 1600 + 20\right] + .20\left[1600 + 20\right]\right]$$

$$\Rightarrow 18 + 0.1\left[0.8(3220) + .20(1620)\right] \quad 2576 + 324$$

$$\Rightarrow 18 + 0.1[2900]$$

$$= 18 + 290$$

$$T_{avg_{write}} = 308\ \text{usec}$$

40% Ref. Write operation

60% Reference for Read Operation

$$T_{avg_{WB}} = \%\ \text{Read operation} \times T_{avg_{read}} + \%\ \text{of write operation} \times T_{avg_{write}}$$

$$\Rightarrow .60 \times 596 + .40 \times 308$$

$$T_{avg_{WB}} = 357.6 + 123.2$$

$$T_{avg_{WB}} = 480.8\ \text{nsec}$$

$$T_{avg} = 481\ \text{nsec}.$$

Q.16 A 16-way set associative cache of size 128KB is used in a system with 32-bit address. For such cache memory, the memory size is 76 (in Kbytes) Provided block size is 4 bytes.

[NAT]

Ans(76)

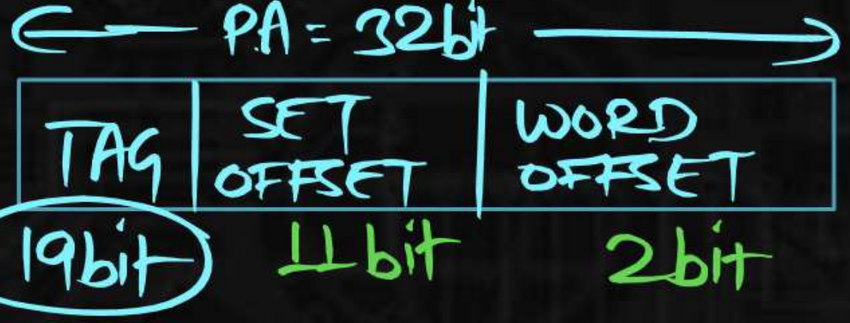
Soln

P.A = 32 bit

Cache Size = 128KB

Block Size = 4Byte = 2^2 Byte

16 Way set Associative



$$\#LINES = \frac{CM\,Size}{Block\,Size} = \frac{128KB}{4B} \Rightarrow \frac{2^{17}B}{2^2B} = 2^{15}\ Lines$$

$$\#SET = \frac{\#LINE}{N\text{-}way} = \frac{2^{15}}{2^4} = 2^{11}\ Set$$

S.O = 11bit

Tag = 32 − (11 + 2)

Tag = 19bit

#SET * $\frac{\text{Block}}{\text{Set}}$ * Tag bits

(or)

Tag Memory = #LINES * Tag bit

$\Rightarrow 2^{15} * 19$

$\Rightarrow \frac{32K \times 19 \text{ bits}}{8 \text{ bit}}$ Byte

$\Rightarrow 4K \times 19$ Byte

$\Rightarrow 76$ K Byte Ans


THANK YOU GW
SOLDIERS !