CS & IT ENGINEERING

Operating Systems

File System And Device Management

Lecture No. 1

By- Dr. Khaleel Khan Sir

- Virtual Memory Concept
- Virtual Memory Implementation

Q.

Consider the following segment table:

Segment	Base	Length
0	1219	600
1	3300	14
2	90	100
3	2327	580
4	1952	96

What are the physical addresses for the following logical addresses?

A. 0, 4302 : TRAP

B. 1, 15 : TRAP

C. 2, 50 : (90+50)

D. 3, 400 : (2327+400)

E. 4, 112 : TRAP

VIRTUAL MEMORY (VM)

: VM gives an illusion to the Programmer/user, that a huge/large amount of Memory is available for executing Programs that are greater than the Size of Available/given Physical Memory

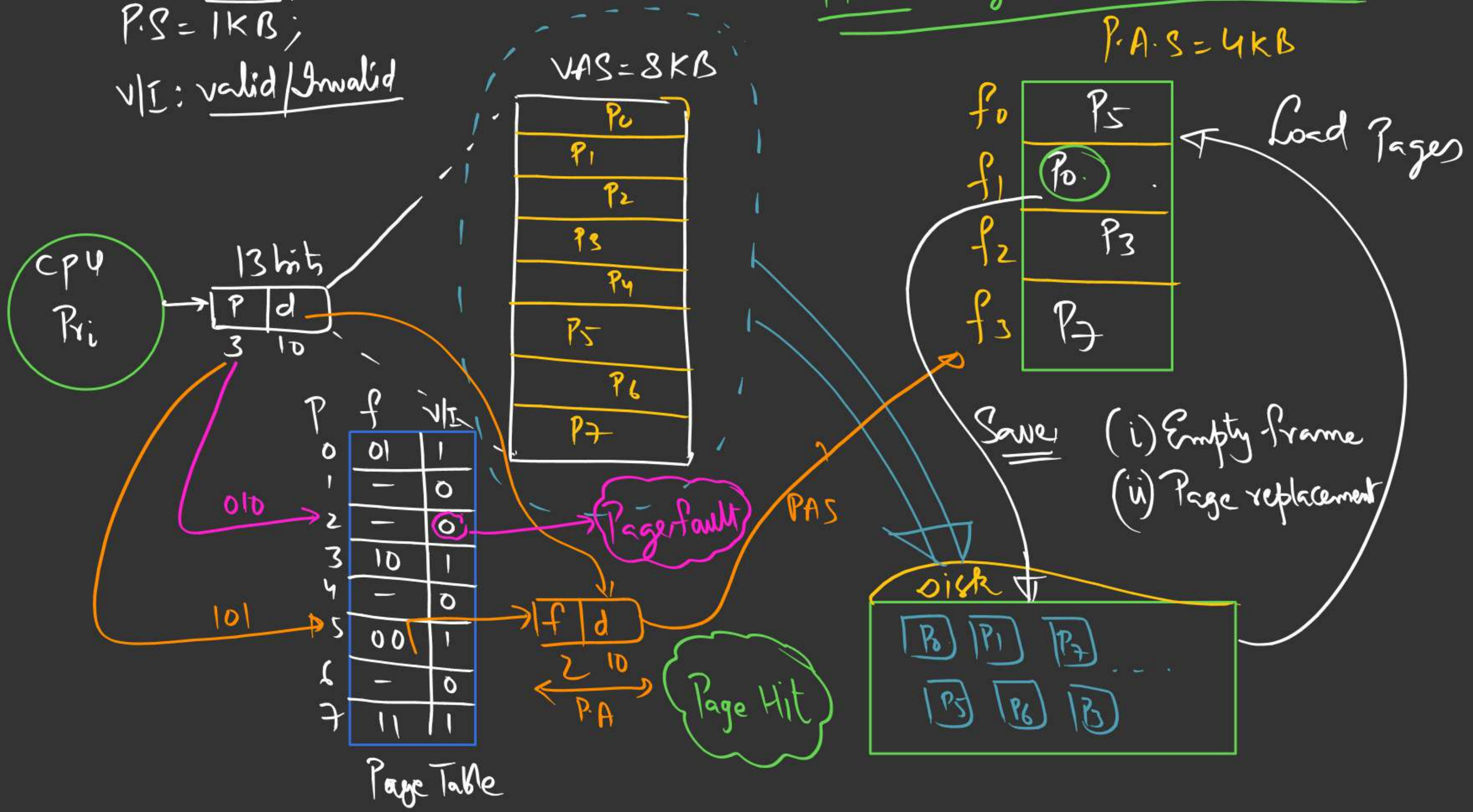
Imp($\Longrightarrow$ It is Implemented thru Demand Paging (D.P)

Demand Paging (DP): Loading the Pages on Demand @ Run Time from Disk (Sec Storage) into Memory;

V·A·S = 8KB; PAS = 4KB;
P·S = 1KB;
V/I : valid / Invalid

PFST : Page-fault Service Time : ms

P·A·S = 4KB



V.M ⟶ Demand Paging (D.P)

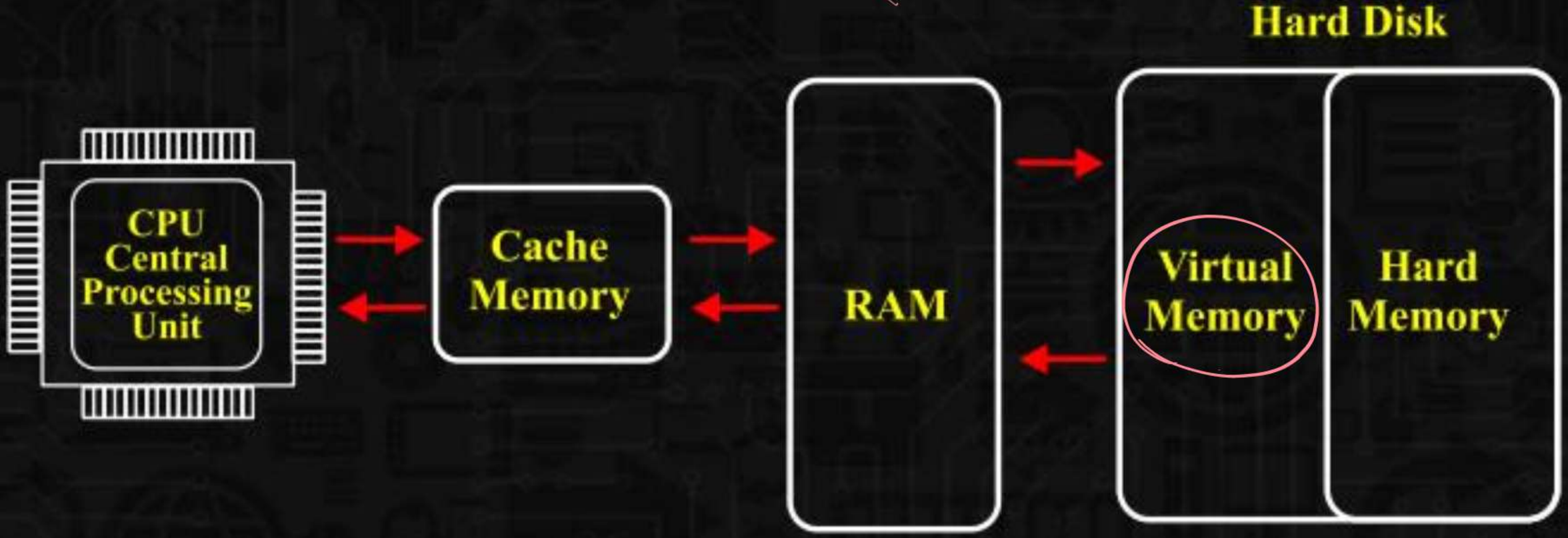
Pure D.P

(Execution of the Program (Process) Starts with all Empty frames)

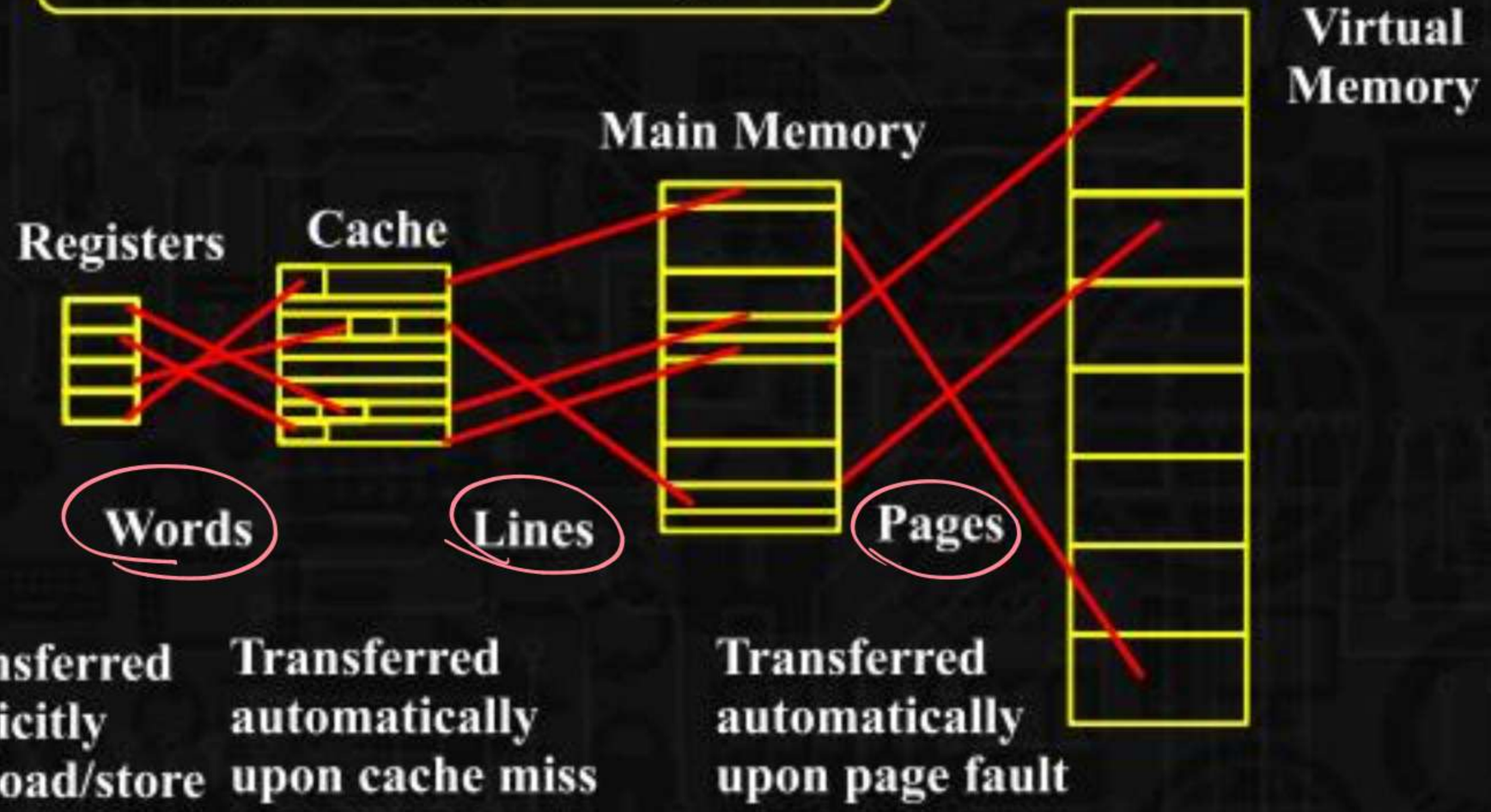
Prefetched D.P

→ (Program execution Starts with all loaded Pages in frames;)

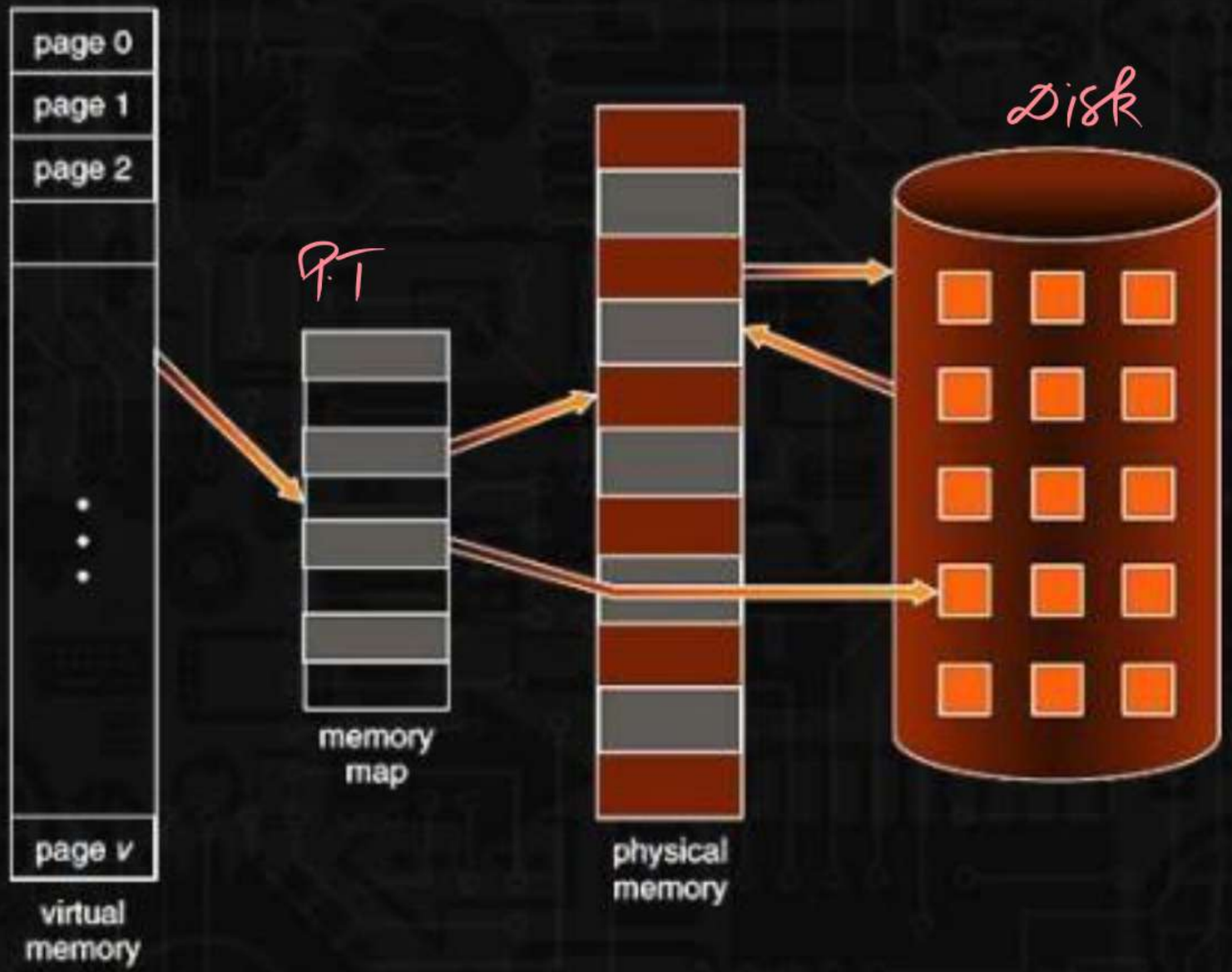
(Total Memory Hierarchy)



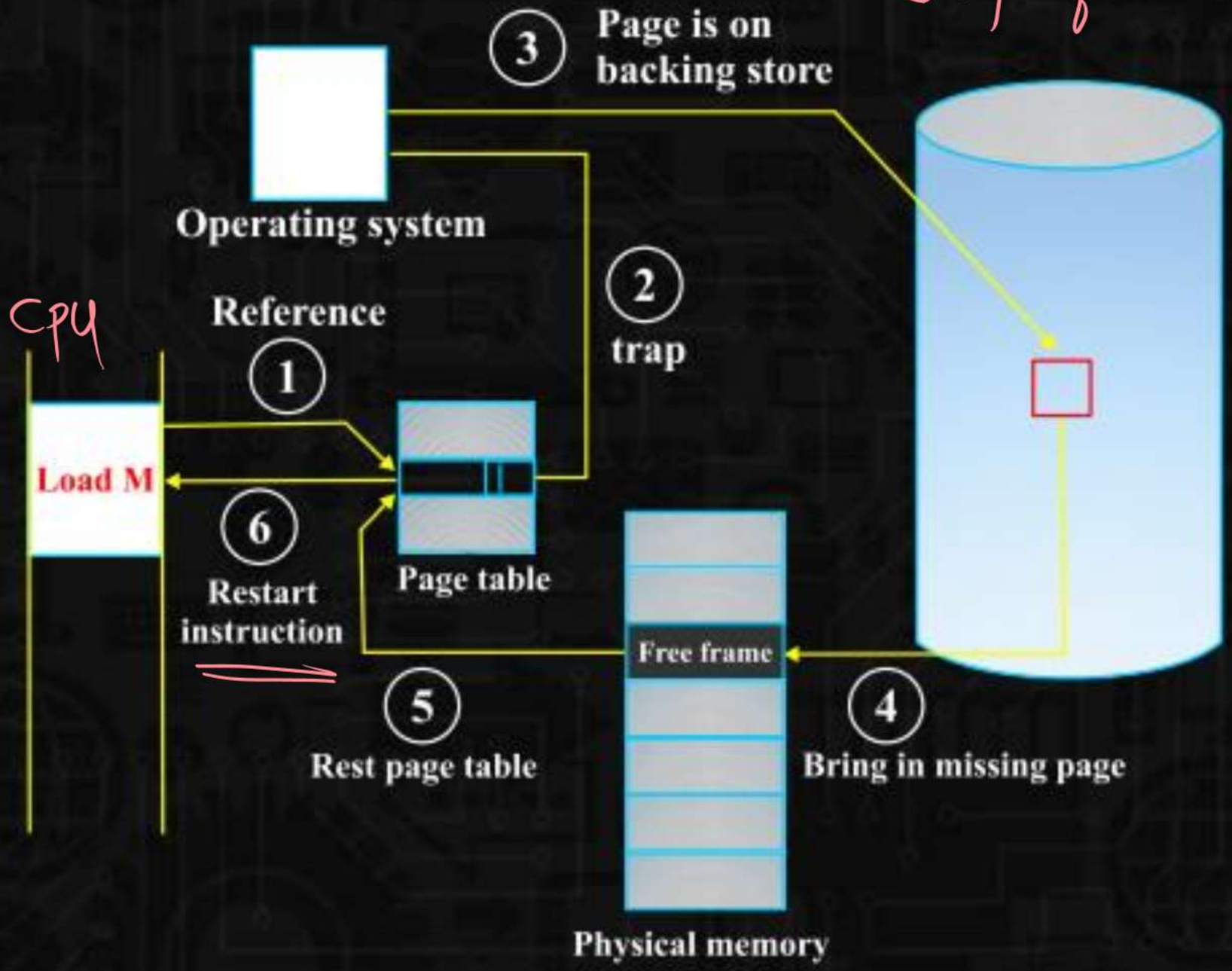
Memory Hierarchy: The Big Picture



Data movement in a memory hierarchy


page 0
page 1
page 2
page v
virtual memory
PT
memory map
physical memory
Disk

Impl. of V.M thru D.P



(1) The Size of V.M is limited by the Size of Secondary Storage

In practice

(2) $P.A.S \leq V.A.S \leq Disk.A.S$

In Theory, any relation

Performance of V.M

1) Temporal Issue :

→ M.M.A.T = 'm'

→ P.F.S.T = 'S' [S >> m]

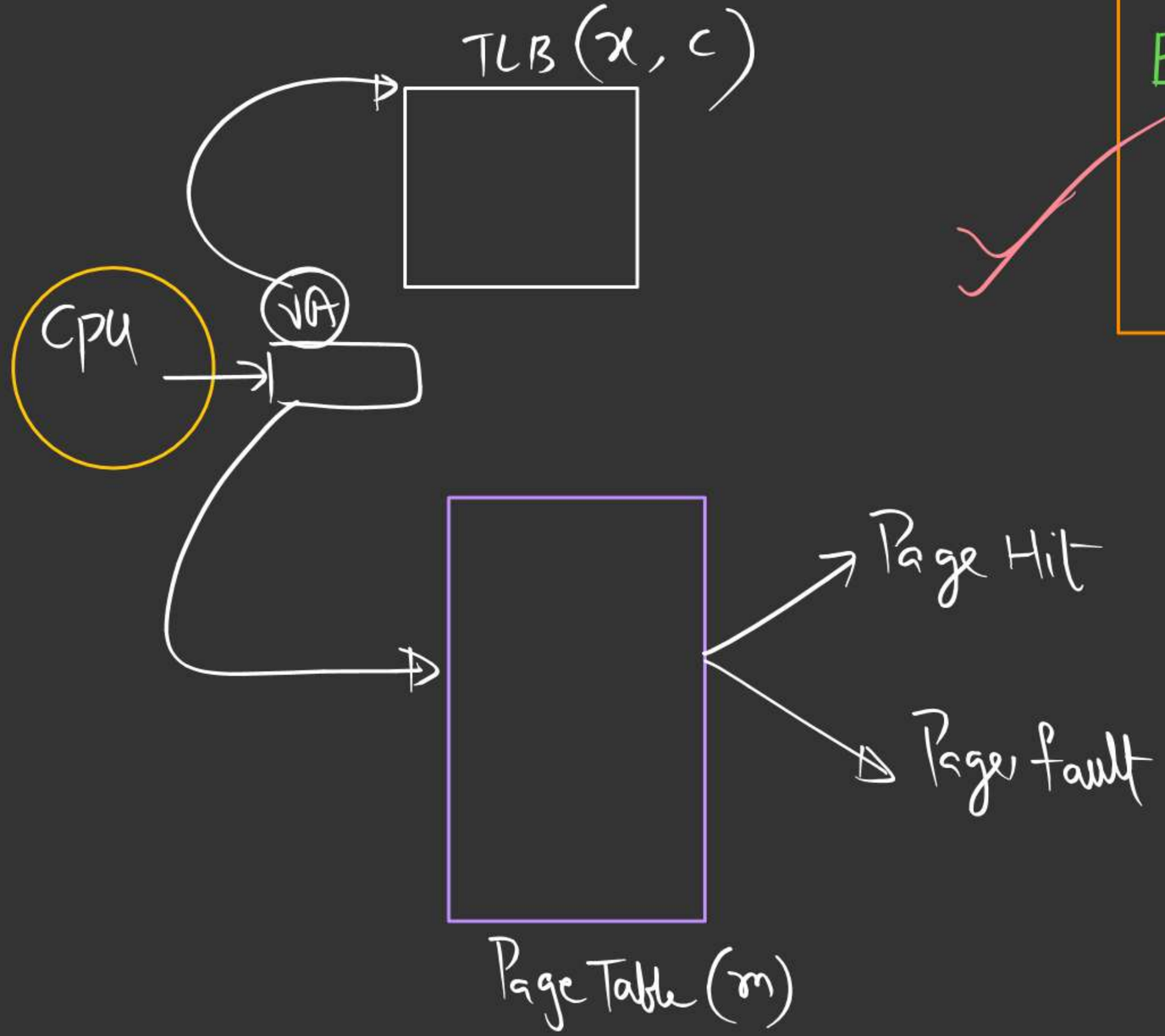
→ Page fault rate = 'P' [0 < P < 1]

→ Page hit rate = '1-P'

$$EMAT = (1-P)m + P*S$$

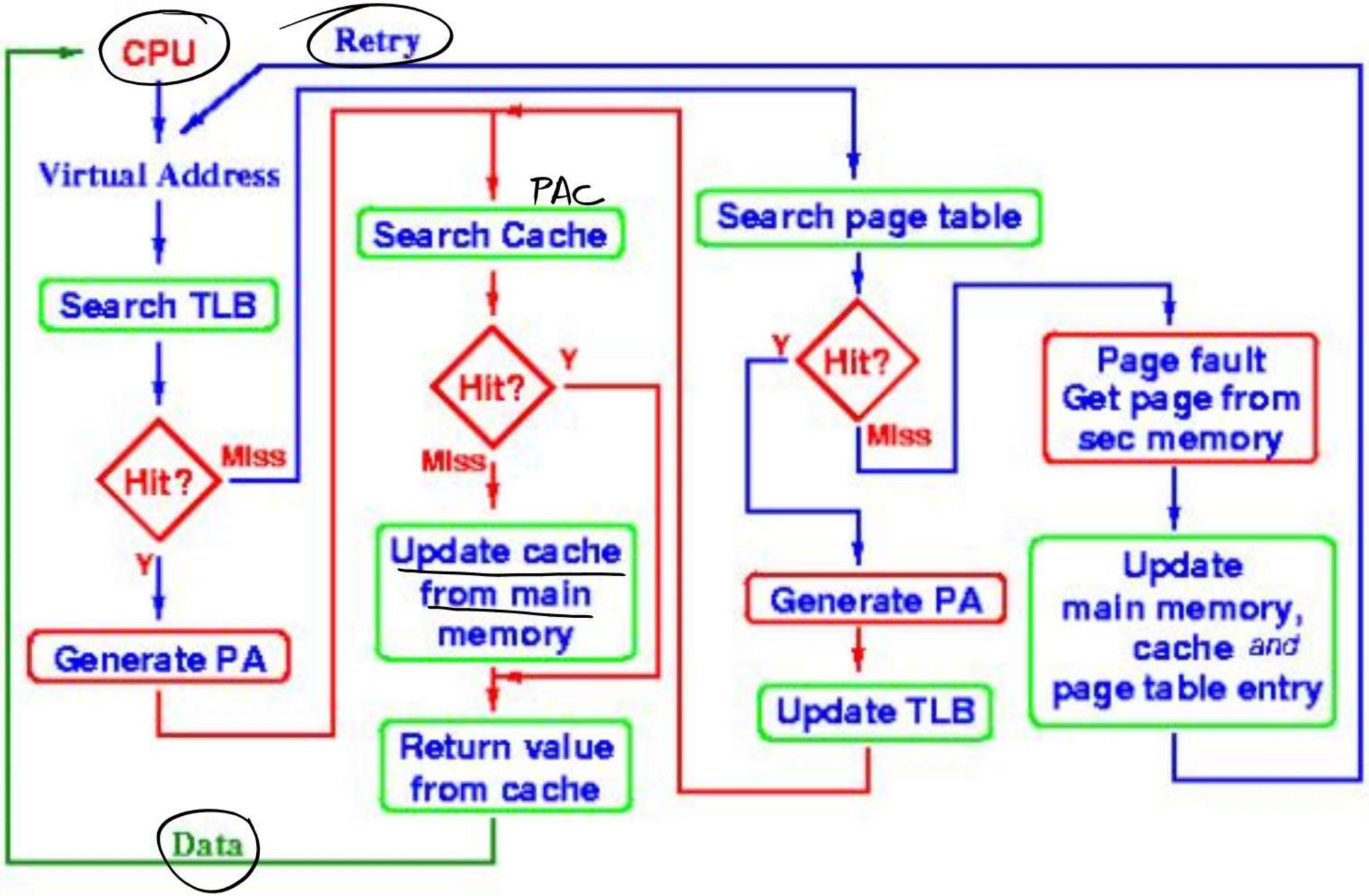
DP

V.M (D.P) with TLB



$$EMAT_{TLB} = x\,[c + m] + (1-x)\,[c + m + m]$$

$$P * \delta + (1-P)\,m$$


CPU
Retry
Virtual Address
Search TLB
Hit?
Miss
Y
Generate PA
Data
PAC
Search Cache
Hit?
Y
Miss
Update cache from main memory
Return value from cache
Search page table
Y
Hit?
Miss
Generate PA
Update TLB
Page fault
Get page from sec memory
Update main memory, cache and page table entry

Q.

In a virtual memory system the address space specified by the address lines of the CPU must be larger than the physical memory size and smaller than the secondary storage size.

A. smaller, smaller

B. smaller, larger

C. larger, smaller

D. larger, larger

Q. The total size of address space in a virtual memory system is limited by:

A. Length of MAR

B. Available secondary storage

C. Available main memory

D. None

Q. The essential content(s) in each entry of a page table is/are

Compulsory

A. virtual page number.

B. page frame number.

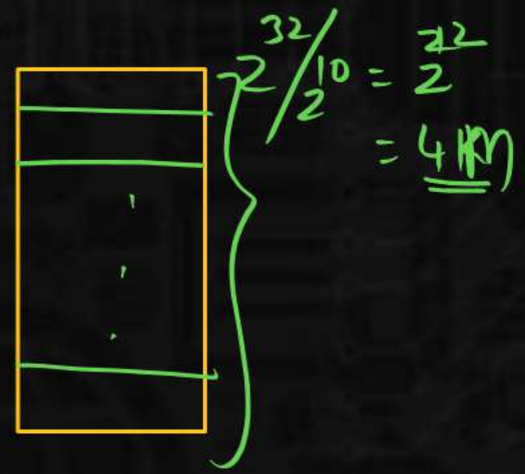
C. both virtual page number and page frame number,

D. access right information.

Optional

Q.

In a system with 32 bit virtual addresses and 1KB page size, use of one-level page tables for virtual to physical address translation is not practical because of



A. the large amount of internal fragmentation

B. the large amount of external fragmentation

C. the large memory overhead in maintaining page tables

D. the large computation overhead in the translation process

Q. Suppose the time to service a Page fault is on the average 10 milliseconds, while a Memory Access takes 1 microsecond. Then a 99.99% Hit ratio results in Average Memory Access Time of _____.

V.M

$\$ = 10\,ms$

$m = 1\,\mu s$

$1-P = 0.9999$

$P = 0.0001$ (0.01%)

$EMAT = 0.0001 \times 10 \times 10^{-3} + 0.9999 \times 1 \times 10^{-6}$

$1 \times 10^{-6} + 0.9999 \times 10^{-6}$

$= (1.9999\,\mu s) \sim 2\,\mu s$

$m = 1\,\mu s$

$\$ = 10\,ms$

$P = 10\%$

$1-P = 90\%$

$EMAT = 0.1 \times 10 \times 10^{-3} + 0.9 \times 10^{-6}$

$= 1 \times \frac{10^{-3} \times 10^{-3}}{10^{-3}} + 0.9 \times 10^{-6}$

$= 1000\,\mu s + 0.9\,\mu s$

$= 1000.9\,\mu s \approx 1\,ms$

Q. If an Instruction takes 'i' microseconds and with a Page Fault takes an additional 'j' microseconds, the Effective Instruction Time if on the average a page fault occurs every 'k' instructions is _____.

$P = 1/k \Rightarrow (i+j)$

$1-P = 1-\frac{1}{k} \Rightarrow 'i'$

$E.I.T = \frac{1}{k}(i+j) + \left(1-\frac{1}{k}\right) i$

$= \frac{i}{k} + \frac{j}{k} + i - \frac{i}{k}$

$= \left(i + j/k\right)$

Q. Assume that we have a Demand-Paged memory. It takes 8 milliseconds to service a page fault if an empty frame is available or if the replaced page is not modified, and 20 milliseconds if the replaced page is not modified. Memory-access time is 100 nanoseconds. Assume that the page to be replaced is modified 70 percent of the time. What is the acceptable page-fault rate for an effective access time of no more than 2000 nanoseconds?

$$EMAT = P * 8 + (1-P) * m$$

$$2000ns = P * [0.7 * 20ms + 0.3 * 8ms] + (1-P)\,100ns$$

Q. Consider a process executing on an operating system that uses demand paging. The average time for a memory access in the system is M units if the Corresponding memory page is available in memory, and D units if the memory Access causes a page fault. It has been experimentally measured that the average Time taken for a memory access in the process is X units. Which one of the Following is the correct expression for the page fault rate experienced by the Process?

A. (D – M)/(X – M)

B. (X – M)/(D – M)

C. (D – X)/(D – M)

D. (X – M)/(D – X)

$EMAT = P * S + (1-P)\,m$

$X = P * D + (1-P)M$

$P = \frac{X-m}{D-m}$

Q.

Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20ns. Each page transfer to/ from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read in from disk. TLB update time is negligible. The average memory access time in ns (round off to 1 decimal places) is _____.

(154.5 ~ 155 ns)

H/W

E.M.A.T =

PW PYQ Series G 2023

II: Page Replacement

a) Page-Reference String: { Set of Successively unique Pages, referred in the given list of V.A's }

PageSize: 100

Pr_i : V.A's ⟨ 701; 723; 856; 203; 208; 549; 586; 705; 892; 001; 122 ..

7 ; 7 ; 8 ; 2 ; 2 ; 5 ; 5 ; 7 ; 8 ; 0 ; 1

701

V.A: | P | d |

7 , 1

VA's

V.A.S

0
1
2
99
100
199
200
299

P_0
P_1
P_2

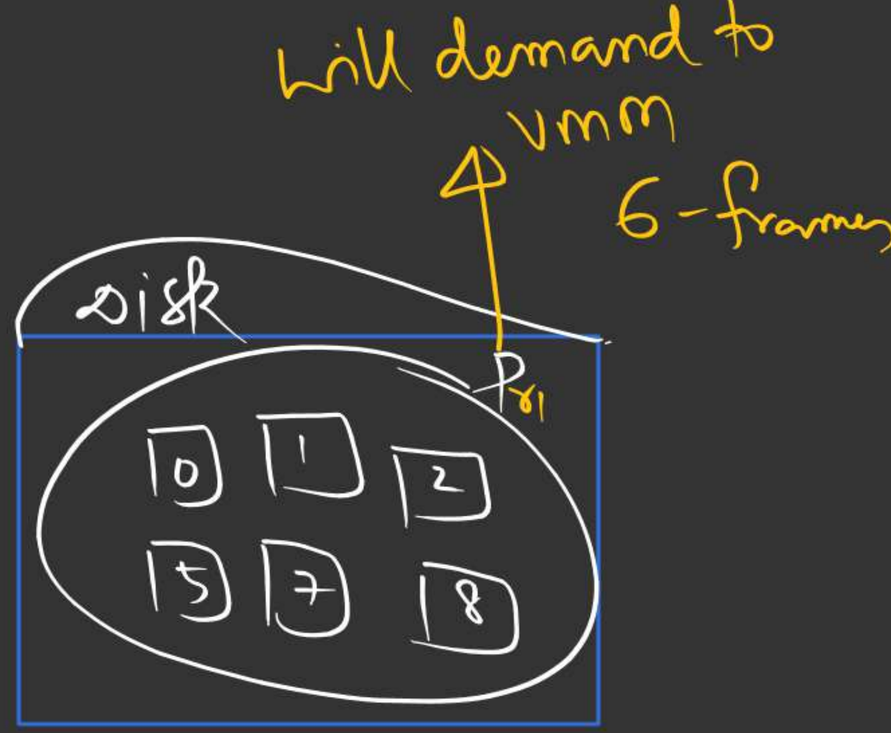
$P = VA / PS$

$d = VA \% PS$

Ref String = ⟨ 7; 8; 2; 5; 7; 8; 0; 1 ⟩

Ref. String

Length (L)	No. of unique Pages (n)
8	<0,1,2,5,7,8> = 6



Frame Allocation/Distribution Policies

: ⟶ 'n' - processes

⟶ demand of each Process for frames : s_i

⟶ Frames alloc by : a_i ?

⟶ Total demand : $D = \sum_{i=1}^{n} s_i$

⟶ Available Frames : M

$(m \leq D)$

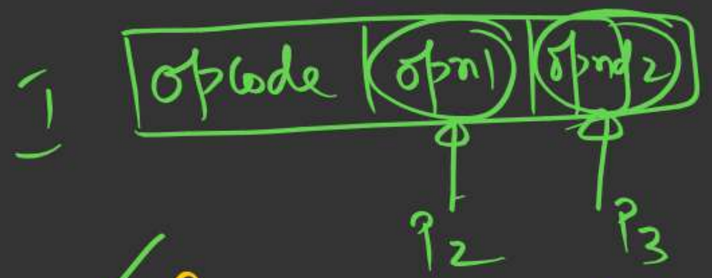
$M = 30$ ⟨Avail⟩

$n = 5$;

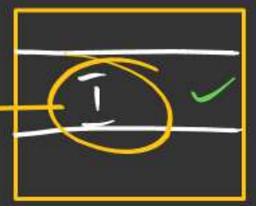
P_i	s_i	a_i Equal $a_i = m/n$	a_i Proportionate $a_i = (s_i/D)m$	$a_i = \frac{s_i}{2}$ 50%
P_1	10	6	$(\frac{10}{70}) \times 30$	5
P_2	5	6	$(\frac{5}{70} \times 30)$	2
P_3	25	6	$(\frac{25}{70} \times 30)$	10
P_4	12	6	—	6
P_5	18	6	—	7
D	70			

(Minimum no. of frames to be allocated to a Process)

→ Process should be able to execute one Instn successfully



Instruction Architecture



Page

Frame

Instruction format

1 Addrs 2 Addrs 3 Addrs

Addressing Modes

Direct Indirect

Q.

The minimum number of page frames that must be allocated to a running process in a virtual memory environment is determined by

A. The instruction set architecture

B. Page size

C. Physical memory size

D. Number of processes in memory

* PAGE-REPLACEMENT TECHNIQUES/ALGORITMS

Ref. string: < 7 ; 0 ; 1 ; 2 ; 0 ; 3 ; 0 ; 4 ; 2 ; 3 ; 0 ; 3 ; 2 ; 1 ; 2 ; 0 ; 1 ; 7 ; 0 ; 1 >

$\ell = 20$;

$n = \langle 0,1,2,3,4,7 \rangle = 6$

Pure D.P

~~7~~	2	2	~~2~~	4	4	~~4~~	0	0	~~0~~	7	7	7
0	~~0~~	3	3	~~3~~	2	2	~~2~~	1	1	~~1~~	0	0
1	1	~~1~~	0	0	~~0~~	3	3	~~3~~	2	2	~~2~~	1

1) First-IN-First-out

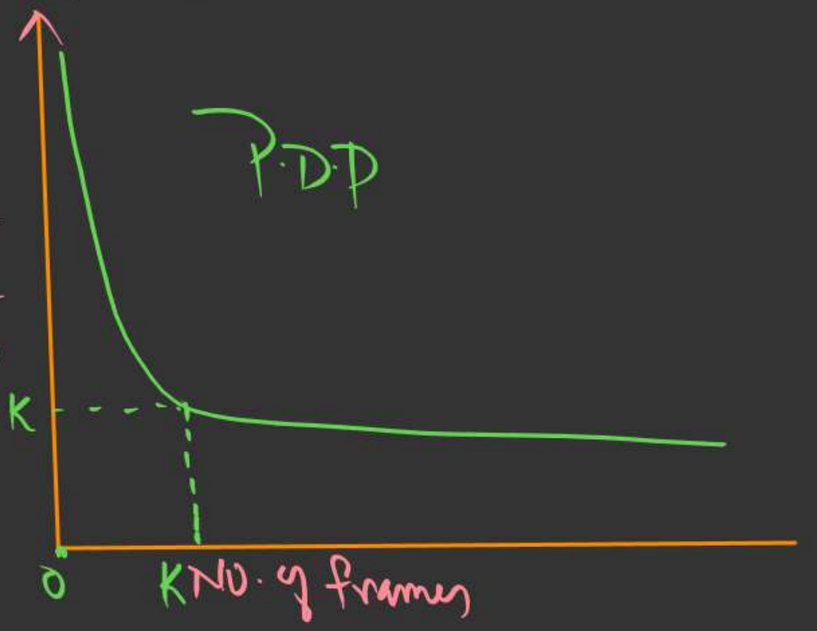
FIFO:

3F → 15 $\left(\frac{15}{20} = 75\%\right)$ frames

Criteria: T.o.L

P	f	VII	T.o.L
0			
1			
2			
:			
7			

4F → 10 $\left(10/20 = 50\%\right)$




THANK YOU
GW
SOLDIERS !