Branch : CSE & IT Batch : English

Computer Organisation and Architecture

Machine Instructions and Addressing Mode

DPP

[MCQ]

1. Which of the following is primitive instruction in the CPU?

(a)

opcode	Address
4 bits	6 bits

(b)

opcode	Address-1	Address-2
4 bits	4 bits	4 bits

(c)

opcode	Address
4 bits	2 bits

(d)

opcode	Address-1	Address-2
2 bits	12 bits	8 bits

[NAT]

2. Consider a hypothetical system which support only-2 address instructions. If size of the instruction is 28 bit and size of each address is 10 bits then, the maximum number of instructions the system can support_____.

[NAT]

3. Consider a digital computer which support 64 3-address instruction. If the size of each address is 14 bits, then the instruction is of _____ bytes.

[MCQ]

4. The correct sequence in Fetch-Execute cycle is:

(a) Decode, Fetch, Execute

(b) Fetch, Execute, Decode

(c) Fetch, Decode, Execute

(d) None of the above

[MCQ]

5. Consider a system which supports 2 - address instructions only. The system has 2^P K bytes of memory. If there are 'q' distinct instructions supported by system then, what is the size of instruction?

(a) (q + p) bits

(b) [logq + 2 (P + 10)] bits

(c) (logq + 2P) bits

(d) log (p + q) bits

[MCQ]

6. Consider a system which support 2 - address instructions add 1-address instruction both. Suppose, the system has 6 bits instruction and 2 - bits addresses. If there are three 2 - address in the system then, maximum and minimum how many 1 - address instruction the system can support?

(a) 15, 1 (b) 4, 1

(c) 16, 0 (d) None

[MCQ]

7. Consider a PC - relative mode type branch instruction, which takes branch on addresses 680 in memory. The instruction has offset value 420. What is the address of this instruction in memory. If each instruction is stored in memory on 2 - locations?

(a) 258 (b) 280

(c) 282 (d) 260

[MCQ]

8. Consider a 6 - word instruction which is of the following type:

opcode	Mode-1	Mode-2	Address-1	Address-2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand of size 2 - words, each address is of 2 word and main memory takes 20 ns for each word access. What is the different between fetch cycle of instruction time and execution cycle of instruction time?

[Note : Register access time is negligible.]

(a) 260 ns (b) 20 ns

(c) 40 ns (d) 120 ns

[MCQ]

9. Consider a computer with 34 bits instruction and 14 bits addresses. If there are 60 2 - address instruction and 65000 1 - address instruction then, how many maximum 0 - address instruction can be formulated?

(a) 65536 K (b) 8576 K

(c) 16384 K (d) None

[MCQ]

10. If an opcode is of 4 bit then, how many maximum minimum type of instruction supported by CPU?

(a) 15, 1 (b) 15, 0

(c) 16, 1 (d) 16, 0

Answer Key

1. **(d)**
2. **(256)**
3. **(6)**
4. **(c)**
5. **(b)**
6. **(b)**
7. **(a)**
8. **(c)**
9. **(b)**
10. **(c)**

Hints & Solutions

1. (d)

Sol. Instruction with small opcode is known as primitive instruction in the CPU.

Therefore, Option (d) is right.

2. (256)

Sol. Instruction size = 28 bits

2-address format:

opcode	Address-1	Address-2
8 bits	10 bits	10 bits

Maximum opcode = 2^8

Maximum number of instructions = 256

3. (6)

Sol. Opcode = log64

= 6 bits

3-address format:

opcode	Address-1	Address-2	Address-3
8 bits	14 bits	14 bits	4 bits

Instruction size = 6 + 3 × 14

= 48 bits

= 6 bytes.

4. (c)

Sol. The correct sequence is

Instruction fetch

Instruction decode

Execution

Therefore, Option (c) is right.

5. (b)

Sol. Memory size = 2^P k bytes

= 2^P × 210 bytes

= 2^{p+10} bytes

Address size = P + 10 bits (each)

Number of instructions = q distinct

Opcode = $\log_2 q$

2-address format:

opcode	Address-1	Address-2
log q	P + 10	P + 10

Instruction size = log q + 2 (p + 10)

logq + 2 (P + 10) bits

Therefore, option (b) is right.

6. (b)

Sol. 2-address format:

opcode	Address-1	Address-2
2 bits	2 bits	2 bits

Number of opcodes = 4

Unused opcode = 4 – 3 = 1

1 -address format:

opcode	Address-1
4 bits	2 bits

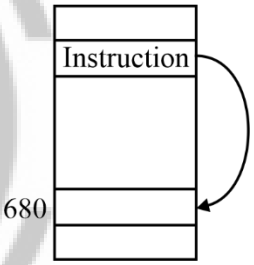
Maximum 1-address = 1 × 2^2 = 4

Minimum 1-address = 1

7. (a)

Sol. Target address = 680

Offset (relative location) = 420



Target address = PC value + offset

680 = PC + 420

PC = 680 – 420

PC = 260

PC hold next instruction address

Instruction address = 260 – 2 (2-location)

= 258

8. (c)

Sol. Fetch cycle:

Operand = 2-word

Address = 2-word

1 word fetch time = 20 ns

6 words fetch time = 6 × 20 = 120 ns

Execution cycle:

In register indirect mode first operand will take = 1 memory access

= 2 word = 2 × 20 = 40 ns

Second operand = 2 memory

$= 2 \times 2 \times 20 = 80$ ns

For write back 1 memory access

$= 1 \times 2 \times 20 = 40$ ns

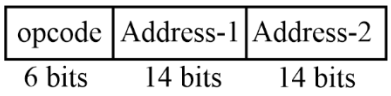
Total execution time = 40 + 80 + 40 = 160 ns

Difference = 160 – 120 = 40 ns

Hence, option (c) is correct.

9. (b)

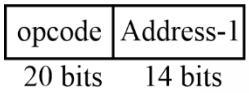
Sol. 2 - Address Format:



Number of opcodes = $2^6 = 64$

Unused opcode = 64 – 60 = 4

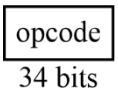
1 - Address Format:



Maximum opcode = $4 \times 2^{14} = 65536$

Unused opcode – 65536 – 65000 = 536

0 - Address Format:



0 - address opcode = $2^{14} \times 536 = 8576$ k

10. (c)

Sol. Opcode = 4bits

Maximum operation = $2^4 = 16 = 16$ (16 instruction)

Minimum = 1 (Always)

Therefore, option (c) is right.