CS & IT



ENGINERING

Computer Organization and Architecture

Instructions Pipelining

DPP Discussion



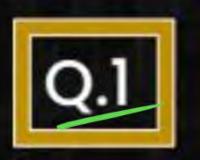
By- Vijay Agarwal sir



TOPICS TO BE COVERED

01 Question

02 Discussion



Consider a non-pipelined processor with 25 ns cycle time is divided into 5 stages with latencies of 5ns, 7ns, 3ns, 6ns and 4ns. If the pipeline latch latency is 1 ns then the maximum clock frequency to be applied is 125 MHz



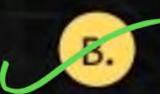
Consider a 4-stage pipeline with delays of 320, 260, 340 and 300 respectively. Inter stage buffer delay is 10 ns, register uses constant clock rate, then what is the total time taken to process 2000 data items on this pipelined system ____ (in micro seconds)



700.05



142.05



701.05





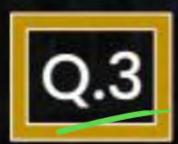
None of these



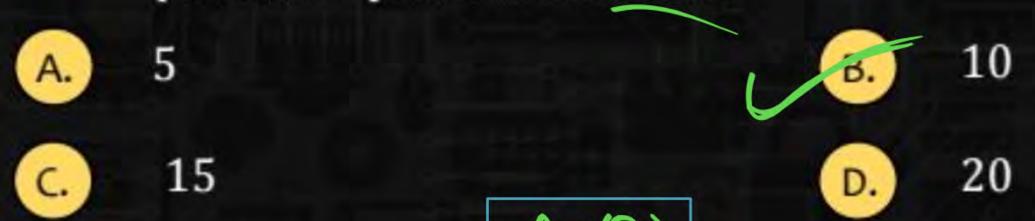
Stage Delay =
$$(220ng, 260ng, 300ng)$$

Buller Delay = $10ngec$
 $tp = max(Stage + Ruller) \Rightarrow 340 + 10 \Rightarrow tp = 350ngec$
 $K = 4. n = 2000$

ETPIPE = $(k + (n-1))tp$



Assume a 5-segment single cycle processor (non-pipelined) and a 5-segment pipelined processor. Cycle time of non-pipelined processor is 10 times that of pipelined processor. Assume also that there are no stalls in the pipelined processor then what is the speed up achieved over non-pipelined processor if pipelined processor phase time is 2ns?



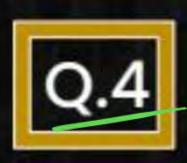
In Pipeline Processor. Cycletime = 2 ns.

Cycle time of Non pipeline processor is

10 times more that at Pipeline Processor.

In Nonpipeline Processor cycletime(tn) = 2×10 = 20 ngec

$$S = \frac{tn}{tp} = \frac{20}{2} = (10) Amg$$



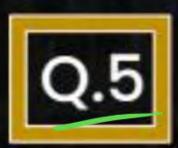
Consider a pipelined machine X operating at 1 GHz that has speed up factor of 5 and operating upto 60% efficiency, then how many segments are present in the machine X? _____ [MCQ]





= S S: Speed up Fortor

k: Number of Stages



Consider a machine with frequencies of instruction, type of with instructions, and cycles. Given below.



Instruction type	Frequency	Cycles
Load	40%	1
Store	15%	2
Branch	20%	2
ALU	25%	2

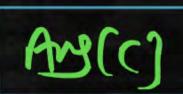
What is the average CPI?

[MCQ]



2.0





В. 1.5



3.0

1.6 Cycle [is cycle Injec]

ET= 1.6x Ingec = 1.6 mec



Consider 5 stage of two processors x and y have the following latencies:



Type	IF	ID	EX	M14	WB
$\widehat{\mathbf{x}}$	400	500	450	650	200
y)	300	250	200	290	240

Also consider that each pipeline costs 20ps extra for the register between pipeline stages. Which of the following pairs of tuples represent the cycle time, latency of one instruction and the throughput for a pipelined processor for both types x and y?

[MCQ]

k=5, n=1ET ab I I not in Pipeline PX EX = [k+(n-1)]tx $\Rightarrow (s+(n-1)) \times 670 \Rightarrow 5 \times 670$

ETx = 3350 Ps.

ET of L Inst" in Pipeline for Py ETy=(k+(n-1)) try =(5+(1-1)) x 820 B = 5x320 Ps

Ely = 1600 PS

Throughputy = 47 = 1320

670, 3350, 1/670

320, 1600, 1₃₂₀.

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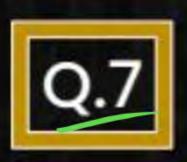


$$(670,3350, \frac{1}{670})$$
 $(320,1600, \frac{1}{320})$

$$\left(670,3350, \frac{1}{3350}\right) \left(320,1600, \frac{1}{1600}\right)$$

$$\left(3350,670, \frac{1}{3350}\right) \left(1600,320, \frac{1}{1600}\right)$$

D. None of the above



Consider the sequence of instruction and a 5-stage pipeline (IF, ID, EX, MEM, and WB).



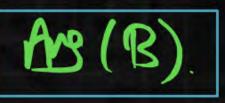
	Opcode	Destination	Source1	Source 2
I ₁ :	ADD	R ₂	R ₃	R ₄ (1 st instruction to enter the pipeline)
I2:	SUB	R ₃	R ₄	R ₂
I ₃ :	MUL	R ₂	R ₃	R ₄ (last instruction to enter the pipeline)

How many RAW data hazards does the ID stage need to detect for this instruction sequence?

[MCQ]



1



3.

2



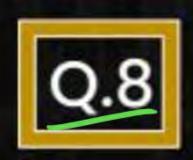
3

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Data Hazard Data Dependency

- 1 RAW Hozards True Data Dep.
- (2) WAR Hozoords Anti Dep.
- 3 WAW Hazards Output Dep.

But in the Question asking Only RAW Data Hazards.



Consider a 5-stage pipelined processor having instruction fetch (IF), instruction decode (ID), instruction execution (IE), memory access (MA) and write back (WB) segments. The segments mentioned takes 1 clock cycle each for any instructions. Consider the given code fragment below.

Instruction	Meaning of instruction		
I ₀ : load R ₂ , [100]	$//R_2 = MEM [100]$		
I ₁ : load R ₄ , 5[R ₃]	$/(R_4) = MEM[R_3 + 5]$		
I ₂ : MUL R ₅ , R ₂ , R ₄	$//R_5 = R_2 \times R_4$		
I ₃ : DIV R ₆ , R ₂ , R ₅	$/(R_6) = R_2 / R_5$		
I ₄ : SUB R ₇ , R ₅ , R ₆	$//R_7 = R_5 - R_6$		

Avg(1B)

What is the number of clock cycle needed to execute the above sequence of instruction?

