Branch : CSE & IT Batch : English

Computer Organization and Architecture

ALU and Control Unit

DPP

1. [MCQ]
The sequence of events that happiness during typical fetch operation is-

(a) PC → MAR → Memory →MDR → IR

(b) PC → Memory →MDR → IR

(c) PC → Memory → IR

(d) PC → MAR → Memory → IR

2. [MCQ]
Which set of instruction transfer the memory word specified by the effective address to AC or Load to AC?

(a) DR ←[MAR]
AC ←AC + DR , E← Cout, SC ← O

(b) DR ← [MAR]
AC ← DR, SC ← O

(c) [MAR] ← AC, SC ← O

(d) DR ← [MAR]
AC ← AC^ DR, SC ←O

3. [MCQ]
Consider a CPU with 128 instructions in the instruction set, where each operation needs 8 cycles. If 60 control signals needed to be generated by the control unit. If signal address field format is used then what is the minimum size of the control word, if horizontal micro programming is used for control unit?

(a) 128 (b) 67

(c) 17 (d) 70

4. [NAT]
Consider a single address field format is used for branch control logic. Assume that the control word is 64 bits wide. The control portion of the micro instruction format is divided in two field.

A micro-operation field of 24 bits specified the micro-operations to be performed. An address selection field specifies a condition, based on the flags, that will cause a micro-instruction branch. There are 16 flags. How many bits are there in address bits?

5. [MCQ]

Which of the following statement is false about CISC architecture?

(a) CISC machine instructions may include complex addressing modes, which requires many clock cycles to carry out.

(b) CISC control unit are typically micro programmed allowing the instruction set to be more flexible.

(c) In the CISC instruction set, all arithmetic/logic instruction must be register based.

(d) None of the above.

[MCQ]

6. Which of the following is the micro program of indirect operand fetch cycle?

(a) t_1 : MAR ← IR [Address]
t_2 : MBR ← M [MAR]
t_3 : AC ← MBR

(b) t_1 : MAR ← (PC)
t_2 : MBR ← Memory
PC ← (PC) + 1
t_3 : IR ← MBR

(c) t_1 : MAR ← (IR (Address)
t_2 : MBR ← Memory
t_3 : MAR ← MBR
t_4 : MBR ← Memory
t_5 : Accumulator ← MBR

(d) None of the above

7. [NAT]
For the operand fetch using indirect addressing mode, how many number of cycles are required to bring the operand in the CPU?

8. [NAT]

Consider a micro-programmed control unit design which supports 7 groups of mutually exclusive control signals.

Groups	Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
Control Signals	2	10	4	1	18	23	6

How many more control bits are required using horizontal micro-programming over vertical micro-programming?

9. [MCQ]

Consider a hypothetical control unit, which supports 512 bytes of control word memory. If the control word is 20 bits long and hardware contains 4 flags and supports 16 branch conditions, what is the maximum number of control signals that can be generated at a time using horizontal micro-programming and vertical micro-programming respectively?

(a) 1,1 (b) 32,32

(c) 32, 1 (d) 1, 32

10. [MCQ]

Vertical micro-programming, horizontal micro-programming and hardwired control are used for control unit design. Which among them has highest and lowest operational speed respectively?

(a) Highest: Hardwired control

(b) Highest: Vertical micro-programming

(c) Lowest: Vertical micro-programming

(d) Lowest: Horizontal micro-programming

Answer Key

1. **(a)**
2. **(b)**
3. **(d)**
4. **(36 to 36)**
5. **(c)**
6. **(c)**
7. **(4)**
8. **(43)**
9. **(c)**
10. **(**a, c**)**

Hints & Solutions

1. (a)

Mirco – operation of fetch instruction:

1. PC→ MAR
2. [MAR]→ MBR
   PC + 1 → PC
3. [MBR] → IR

2. (b)

LDA AC load to AC instruction transfer the memory word specified by the effective address to AC

T_1: MDR ← [MAR]

T_2: AC ← MDR, SC ← O

3. (d)

Total number of cycles = 128 inst. × 8 cycles
= 2^{10} cycles.

Or we can say

Total number of micro-operations = 2^{10}

Bits needed for addressing control memory = $\log 2^{10}$ = 10

Minimum size of control word = 60 + 10 = 70

4. (36 to 36)

In a single address field, the option for next address are as follows:

1. Address field.
2. Instruction register code.
3. Next sequential address.

The address-selection signals determine which option is selected. The approach reduces the number of address field to one.

There are total 16 flags. Hence 4 bits are needed in the address selection bit.

64 – (24 + 4) = 36 bits are needed in the address field.

5. (c)

In RISC instruction set all arithmetic/logic must be register based but not in CISC.

6. (c)

Mirco program of indirect operand fetch cycle:

t_1 : MAR ← (IR Address)

t_2 : MBR ← Memory

t_3 : MAR ← MBR

t_4 : MBR ← Memory

t_5 : Accumulator ← MBR

7. (4)

The microprogram for operand fetch using indirect addressing mode is as follows:

t_1 : MAR ← IR [Address]

t_2: MBR ← Memory

Thus, in these two cycles effective address i.e., the address of the operand is brought to the CPU.

t_3 : MAR ← MBR

t_4: MBR ← Memory

These, two cycles are required to bring operand from memory to the CPU.

So, total 4 cycles are required.

8. (43)

For vertical Micro programming:

Micro-Instruction format:

Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
$\log_2 2$	$\log_2 10$	$\log_2 4$	$\log_2 1$	$\log_2 18$	$\log_2 23$	$\log_2 6$

Total control bits required = 1 + 4 + 2 + 1 + 5 + 5 + 3.
= 21 bits

[For horizontal micro-programming]

Micro instruction format:

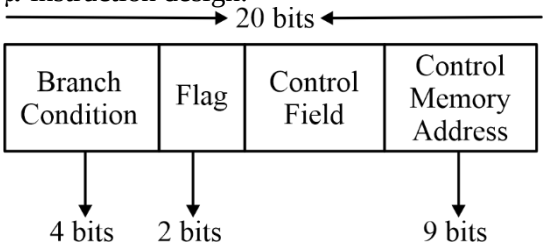
Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
2	10	4	1	18	23	6

Total bits required = 2 + 10 + 4+1+18 + 23 + 6
= 64 bits

So, horizontal micro programming requires, 64-21 = 43, more bits.

9. (c)

μ-instruction design:



Control word memory = 512 bytes

So, control memory address field require = 9 bits

Number of flags = 4

So, number of flag bits required = 2

Number of branch conditions = 16

So, number of branch condition bits required = 4

Number of bits required for control field = 20 - (4 + 2 + 9) = 5

Therefore, number of control signals that can be generated = 25 = 32 In Horizontal micro-programming for each control signal 1 bit is there, So, all control signals can be activated at a time.

∴ Maximum degree of parallelism for horizontal microprogramming = 32

∴ In vertical microprogramming only 1 control signal can be activated at a time.

∴ Maximum degree of parallelism for vertical micro-programming = 1

∴ Option (c) is correct.

10. (a, c**)**

Highest: hardwired control

Lowest: vertical micro-programming.

- In hardwired, control logic is implemented using gates and flipflops. So, it is fastest.
- In horizontal microprogramming for each control signal a separate bit is used.
- In vertical microprogramming, control signals are expressed in form of encoded binary format.

Thus, a decoder is used.

So, for 'n' control signals log bits are used so it has slowest operational speed.