CS & IT ENGINEERING

Computer Organization and Architecture

ALU and Control Unit

DPP – Discussion

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01 Question

02 Discussion

Q.1

The sequence of events that happiness during typical fetch operation is-

[MCQ]

A. PC → MAR → Memory → MDR → IR

B. PC → Memory → MDR → IR

C. PC → Memory → IR

D. PC → MAR → Memory → IR

Ans (A)

Fetch cycle : To Fetch the Instruction from Mem to CPU (IR)

PC → MAR (Why in MAR, MAR Connected to Address Line)

MAR → Memory → MBR (MDR/DR) (∵ MBR Connected to Data line of the Bus)

MBR/MDR → IR

Q.2 Which set of instruction transfer the memory word specified by the effective address to AC or Load to AC? **[MCQ]**

A. $DR \leftarrow [MAR]$
$AC \leftarrow AC + DR, E \leftarrow Cout, SC \leftarrow 0$

B. $DR \leftarrow [MAR]$
$AC \leftarrow DR, SC \leftarrow 0$

C. $[MAR] \leftarrow AC, SC \leftarrow 0$
Memory write (Storing)

D. $DR \leftarrow [MAR]$
$AC \leftarrow AC \wedge DR, SC \leftarrow 0$

Ans (B)

I_i : LOAD AC
$\Downarrow$ $AC \in M[x]$
Memory Read.

STORE : Memory write

Q.3

Consider a CPU with 128 instructions in the instruction set, where each operation needs 8 cycles. If 60 control signals needed to be generated by the control unit. If signal address field format is used then what is the minimum size of the control word, if horizontal micro programming is used for control unit? [MCQ]

A. 128

B. 67

C. 17

D. 70

Ans (D)

Total No. of Instⁿ = 128.

Cycles per Instⁿ = 8 Cycle
(#uoperⁿ/Instⁿ)

Total # uoperation/uInstⁿ = 128 × 8 uoperⁿ/uInstⁿ/CW

$= 2^7 \times 2^3 \Rightarrow 2^{10}$ CW. $\Rightarrow$ 1KCW.

Control Memory = 1024 CW

CAR | AR | NIA = 10bit

CW = 60 + 10

= 70bit

60 Control Signal

Horizontal uprogramming $\Rightarrow$ 60 CS $\Rightarrow$ 60bits

Q.4

Consider a single address field format is used for branch control logic. Assume that the control word is 64 bits wide. The control portion of the micro instruction format is divided in two field.

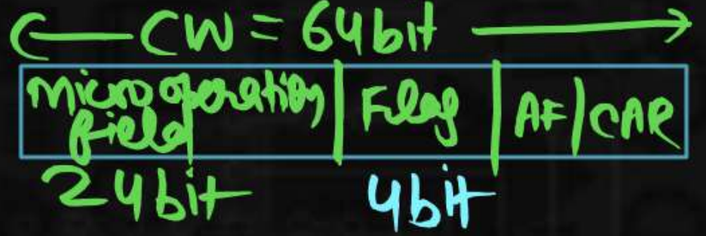
A micro-operation field of 24 bits specified the micro-operations to be performed. An address selection field specifies a condition, based on the flags, that will cause a micro-instruction branch. There are 16 flags. How many bits are there in address bits?

[NAT]

$2^n \geq \log_2 16$

16 Flag

4bit



Address field $= 64 - (24 + 4)$

$= 64 - 28$

$= 36$ Ans

Ans (36).

Q.5

Which of the following statement is false about CISC architecture?

[MCQ]

A. CISC machine instructions may include complex addressing modes, which requires many clock cycles to carry out.

B. CISC control unit are typically micro programmed allowing the instruction set to be more flexible.

RISC : Hardwired
CISC : Micro Programmed

C. In the CISC instruction set, all arithmetic/logic instruction must be register based.

False

In RISC : More Number of Register
↳ & ALU Operation on Register Content

D. None of the above.

Ans [C]

Q.6

Which of the following is the micro program of indirect operand fetch cycle? [MCQ]

A. t_1 : MAR ← IR [Address]
t_2 : MBR ← M [MAR]
t_3 : AC ← MBR

B. t_1 : MAR ← (PC)
t_2 : MBR ← Memory
PC ← (PC) + 1
t_3 : IR ← MBR

C. t_1 : MAR ← (IR (Address)
t_2 : MBR ← Memory
t_3 : MAR ← MBR
t_4 : MBR ← Memory
t_5 : Accumulator ← MBR

D. None of the above

Ans (C)

(a) t_1 MAR ∈ IR[AF]
t_2: MBR ∈ M(MAR)
t_3: AC ∈ MBR

its Mem Direct AM.

(b) Fetch cycle

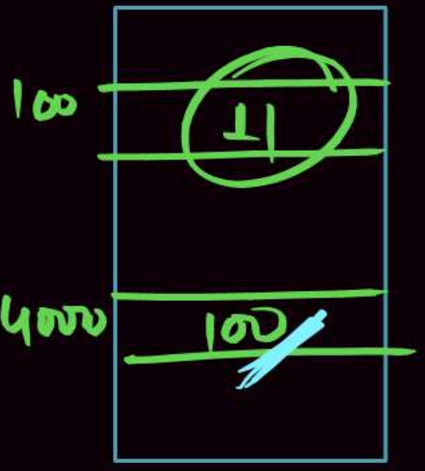
t_1 MAR ∈ PC
t_2 MBR ∈ memory
PC ∈ PC+1
t_3 IR ∈ MBR

} Only Instn Fetch

LOAD @40000

AC ∈ M[[40000]]
M(100)

AC ∈ 11



(c)
t_1 MAR ∈ IR[AF]
t_2 MBR ∈ mem ; eg 100
t_3 MAR ∈ MBR
t_4 MBR ∈ memory (11 in MBR)
t_5 AC ∈ MBR

Mem Indirect AM

Q.7

In the operand fetch using indirect addressing mode micro-program, how many number of cycles are required to bring the operand in the CPU?

[NAT]

t_1 MAR ← IR[AF]

t_2 MBR ← Memory ; (EA)

t_3 MAR ← MBR

t_4 (DATA) MBR ← M(MAR)
[CPU Reg]

Ans (4)

Q.8

Consider a micro-programmed control unit design which supports 7 groups of mutually exclusive control signals.

Groups	Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
Control Signals	2	10	4	1	18	23	6
	1	4	2	1	5	5	3

Horizontal = 64 bit
= 21 bits

How many more control bits are required using horizontal micro-programming over vertical micro-programming? [NAT]

Vertical NCS ⇒ $\log_2 N$ bit

Horizontal NCS ⇒ N bit

Horizontal μprog = 64 bit

Vertical μprog = 21 bit

64 - 21 = 43 bits Ans

Ans(43)

Q.9

Following is the expression for control signal Z, present in a hardware:

$Z = T_1 (I_1 + I_4) + T_2 + T_3 + T_4 (I_1 + I_2 + I_3 + I_4)$

Given that the system has 5 different instructions I_1, I_2, I_3, I_4, I_5 and each instruction has 4 micro-operations T_1, T_2, T_3, T_4. During the execution of instruction I_5 in which micro-operation the control signal is enabled in the hardware? [MCQ]

A. T_1 and T_2

B. T_2 and T_3

C. T_1, T_2, T_3 and T_4

D. No solution

$Z = T_1(I_1+I_4) + T_2 + T_3 + T_4(I_1+I_2+I_3+I_4)$

$T_2 / I_1 I_2 I_3 I_4$ → I_5

$T_3 / I_1 I_2 I_3 I_4$ → I_5

Ans (B)

If I_5 is enable in T_4

$T_4 / (I_1+I_2+I_3+I_4+I_5)$

T_4

Q.10

Vertical micro-programming, horizontal micro-programming and hardwired control are used for control unit design. Which among them has highest and lowest operational speed respectively?

[MSQ]

Speed : Hardwired CU > Horizontal Uprog. CU > Vertical Uprog CU

Flexibility : Vertical > Horizontal > Hardwired

A. Highest: Hardwired control

B. Highest: Vertical micro-programming

C. Lowest: Vertical micro-programming

D. Lowest: Horizontal micro-programming

Ans (a & c)


THANK YOU GW
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