Branch : CSE & IT **Batch : English**

Computer Organization & Architecture
Instructions pipelining

DPP

[NAT]

1. Consider a non-pipelined processor with 25 ns cycle time is divided into 5 stages with latencies of 5ns, 7ns, 3ns, 6ns and 4ns. If the pipeline latch latency is 1 ns then the maximum clock frequency to be applied is _____ MHz

[MCQ]

2. Consider a 4-stage pipeline with delays of 320 ns, 260 ns, 340 ns and 300 ns respectively. Inter stage buffer delay is 10 ns, register uses constant clock rate, then what is the total time taken to process 2000 data items on this pipelined system _____ (in micro seconds)

(a) 700.05 (b) 701.05
(c) 142.05 (d) None of these

[MCQ]

3. Assume a 5-segment single cycle processor (non-pipelined) and a 5-segment pipelined processor. Cycle time of non-pipelined processor is 10 times that of pipelined processor. Assume also that there are no stalls in the pipelined processor then what is the speed up achieved over non-pipelined processor if pipelined processor phase time is 2ns?

(a) 5 (b) 10
(c) 15 (d) 20

[MCQ]

4. Consider a pipelined machine X operating at 1 GHz that has speed up factor of 5 and operating upto 60% efficiency, then how many segments are present in the machine X? _____

(a) 5 (b) 6
(c) 7 (d) 9

[MCQ]

5. Consider a machine with frequencies of instruction, type of instructions, and cycles. Given below.

Instruction type	Frequency	Cycles
Load	40%	1
Store	15%	2
Branch	20%	2
ALU	25%	2

What is the average CPI?

(a) 2.0 (b) 1.5
(c) 1.6 (d) 3.0

[MCQ]

6. Consider 5 stage of two processors x and y have the following latencies:

Type	IF	ID	EX	MA	WB
x	400	500	450	650	200
y	300	250	200	290	240

Also consider that each pipeline costs 20ps extra for the register between pipeline stages. Which of the following pairs of tuples represent the cycle time, latency of one instruction and the throughput for a pipelined processor for both types x and y?

(a) $\left(670, 3350, \frac{1}{670}\right)\left(320, 1600, \frac{1}{320}\right)$

(b) $\left(670, 3350, \frac{1}{3350}\right)\left(320, 1600, \frac{1}{1600}\right)$

(c) $\left(3350, 670, \frac{1}{3350}\right)\left(1600, 320, \frac{1}{1600}\right)$

(d) None of the above

[MCQ]

7. Consider the sequence of instruction and a 5-stage pipeline (IF, ID, EX, MEM, and WB).

	Opcode	Destination	Source1	Source 2
I_1:	ADD	R_2	R_3	R_4 (1^{st} instruction to enter the pipeline)
I_2:	SUB	R_3	R_4	R_2
I_3:	MUL	R_2	R_3	R_4(last instruction to enter the pipeline)

How many RAW data hazards does the ID stage need to detect for this instruction sequence?

(a) 1 (b) 2

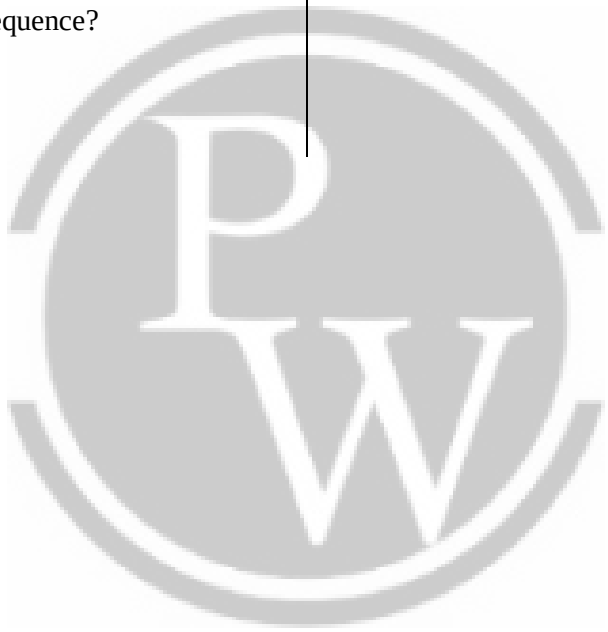
(c) 3 (d) 4

[NAT]

8. Consider a 5-stage pipelined processor having instruction fetch (IF), operand fetch (ID), instruction execution (IE), memory access (MA) and write back (WB) segments. The segments mentioned takes 1 clock cycle each for any instructions. Consider the given code fragment below.

Instruction	**Meaning of instruction**
I_0: load R_2, [100]	//R_2 = MEM [100]
I_1: load R_4, 5[R_3]	//R_4 = MEM [R_3 + 5]
I_2: MUL R_5, R_2, R_4	//R_5 = R_2 × R_4
I_3: DIV R_6, R_2, R_5	//R_6 = R_2 / R_5
I_4: SUB R_7, R_5, R_6	//R_7 = R_5 -R_6

What is the number of clock cycle needed to execute the above sequence of instruction?



Answer Key

1. **(125)**
2. **(b)**
3. **(b)**
4. **(d)**
5. **(c)**
6. **(a)**
7. **(b)**
8. **(18)**

Hints & Solutions

1. (125)

Sol. Largest delay = 7 + 1 = 8 ns

$f_{max} = \frac{1}{8}$ ns = 125 MHz

2. (b)

Sol. pipeline time (t_p) = (n + k – 1) × T_{seg}

Where n is the number of instruction, k is the number of segment/stages and T_{seg} is maximum delay in segment.

= (2000 + 4 – 1) × (340 + 10) ns

= (2003) × (350) ns

= 701.05 μs

3. (b)

Sol. Given,

For non-pipelined processor, cycle time is 10 times more than that of pipelined machine's cycle time.

Cycle time for pipelined machine is 2 ns.

∴ Cycle time for non-pipelined machine is 20 ns

$$\text{Speed up} = \frac{t_n}{t_p} \Rightarrow \frac{\cancel{20}^{10}}{\cancel{2}} = 10 \text{ ns}$$

∴ option (b) is correct.

4. (d)

Sol. $\eta = \frac{\text{speed up}}{\text{number of stages}}$

$\frac{60}{100} = \frac{5}{k}$

$k = \frac{5}{0.6} \Rightarrow 8.33$

= 9 stages

Therefore, if we take 9 stages then the efficiency would be 0.6.

5. (c)

Sol. $\text{Average CPI} = \frac{\sum_{i=1}^{n} \text{instruction frequency}_i \times \text{CPI}_i}{\sum_{i=1}^{n} \text{instruction frequency}_i}$

$= \frac{0.4\times1 + 0.15\times2 + 0.2\times2 + 0.25\times2}{1} = 1.6$

6. (a)

Sol. **For non-pipelined processor**

Cycle time: There is no pipelining, so the cycle time instructions will be going through all the stages each cycle.

So, x : Cycle time = 2200 ps

y : Cycle time : 1280 ps

The latency for an instruction is also the same. Since each instruction takes 1 cycle to go from beginning fetch to end of write back/Throughput is also $\frac{1}{\text{Cycle}}$ instruction per second.

For pipelined processor of

Cycle time: in this we take time of longest stage.

Type x: In this MM takes 650ps and there is 20ps overhead so in total 670 is cycle time.

Type y: In this IF takes 300 ps and there is overhead of 20 ps so in total 320 is the cycle time.

Latency: It is total time taken to execute an instruction.

Type x : 670 × 5 = 3350 ps

Type y : 320 × 5 = 1600 ps

Throughput: it is the number of instructions executed per unit time and also throughput calculated considering large number of instructions.

Type x : 1 instruction per 670 ps = $\frac{1}{670}$

Type y : 1 instruction per 320 : $\frac{1}{320}$.

7. (b)

Sol. $I_1 \rightarrow I_2$ on R_2

$I_2 \rightarrow I_3$ on R_3

∴ for a given program and pipeline, there are 2 hazards.

8. (18)

Sol. RAW dependency between

$I_0 - I_2$, $I_1 - I_2$, $I_2 - I_3$, $I_3 - I_4$

Cycles	IF	ID	EX	MA	WB
C_1	I_0				
C_2	I_1	I_0			
C_3	I_2	I_1	I_0		
C_4		I_2	I_1	I_0	
C_5	I_3	I_2	-	I_1	I_0
C_6	-	I_2			I_1
C_7	-	I_2			
C_8	I_4	I_3	I_2		
C_9	-	I_3		I_2	
C_{10}	-	I_3			I_2
C_{11}	-	I_3			
C_{12}		I_4	I_3		
C_{13}		I_4		I_3	
C_{14}		I_4			I_3
C_{15}		I_4			
C_{16}			I_4		
C_{17}				I_4	
C_{18}					I_4