Branch : CSE & IT Batch : English

Computer Organization and Architecture

Introduction to COA

DPP

1. [MCQ]

Consider 64 bit hypothetical CPU which support 256 KB memory space processer is enhanced with word addressable memory. How many address pins are saved in enhanced CPU to refer the memory?

(a) 1 (b) 2

(c) 3 (d) 4

2. [MCQ]

How many 128×8 bit RAMs are required to design 32K × 32 bit RAM ?

(a) 512 (b) 1024

(c) 128 (d) 32

3. [MCQ]

Consider 32 bits hypothetical CPU which supports word addressable memory used to execute the following code. The code starting address is 2000.

Instruction	**Size in bytes**
I_1	16
I_2	12
I_3	16
I_4	12
I_5	8
I_6	8

During the execution of I_4 Instruction what would be the value present in the program counter (PC).

(a) 2011 (b) 2013

(c) 2014 (d) 2018

4. [MCQ]

Match the column I with column II and select the correct answer.

	Column -I		Column -II
A.	Program counter (PC)	(i)	Contain the instruction currently being executed by CPU
B.	Memory Address Register (MAR)	(ii)	That contain temporary result or first operand of ALU operation
C.	Instruction Register (IR)	(iii)	Contain the starting address of the next instruction to be fetch.
D.	Accumulator (AC)	(iv)	Contain the address of memory location used for either read or write operation.

(a) A- (iii) B-(i) C – (iv) D-(ii)

(b) A- (iii) B-(iv) C – (ii) D-(i)

(c) A- (ii) B-(iv) C – (i) D-(iii)

(d) A- (iii) B-(iv) C – (i) D-(ii)

5. [MCQ]

What does the following program produce when run on an 8085 microprocessor ?

```
LDA   8000 H (Load)
MVI   B, 30 H
ADD   B
STA   8001 H (Store)
```

(a) Read a number from input port and store it in memory.

(b) Read a number from input device with address 8000H and store it in memory at location.

(c) Read a number from memory at location 8000H and store it in memory location 8001H.

(d) None of these

6. [MCQ]

Consider 64 bits hypothetical CPU which supports byte addressable memory used to execute the following code. The code starting address is 1000.

Instruction	Size of bytes
I_1	2
I_2	4
I_3	4
I_4	4
I_5	2
I_6	6

During the execution of I_5 Instruction. What would be the value present is the program counter (PC).

(a) 1014 (b) 1015

(c) 1016 (d) 1021

7. [NAT]

To execute a program, instructions has to be brought from memory using bus to CPU. If the bus has 8 lines then almost one 8-bit (1byte) can be transferred at a time.

The how many memory access are required in this cases to transfer a 32 bit instruction from memory to the CPU?

8. [MCQ]

Consider the statements

S_1: In little endian, lower address contain lower byte and higher address contain higher byte.

S_2: In big Endian, lower address contain higher byte and higher address contain lower byte.

(a) Only S_1 is true

(b) Only S_2 is true

(c) Both S_1 & S_2 are true

(d) Neither S_1 nor S_2 is true.

9. [MCQ]

Consider the statements

S_1: Accumulator Stores the results of calculations made by ALU.

S_2: Program counter keeps track of the memory location of the current instruction by which process is currently dealing with.

(a) Only S_1 is true

(b) Only S_2 is true

(c) Both S_1 & S_2 are true

(d) Neither S_1 nor S_2 is true.

10. [MSQ]

Which of the statements is/are true?

(a) Memory address register stores the memory locations in instruction that needed to be fetched from memory.

(b) Memory data register stores the instruction fetched from memory or any data that is to be transferred to and stored in memory.

(c) Instruction register stores the most recently fetched instruction.

(d) Instructions buffer register contains the instruction which are not to be executed immediately.

Answer Key

1. **(c)**
2. **(b)**
3. **(c)**
4. **(d)**
5. **(c)**
6. **(c)**
7. **(4 to 4)**
8. **(c)**
9. **(a)**
10. **(a,b,c,d)**

Hints & Solutions

1. (c)

By default memory is byte addressable

Memory space = 256 KB

$= 2^{18}$ Bytes

$\boxed{\text{Address pins} = 18}$

In enhanced processor

Word size = 64 bit

Memory space = 256 × k × 8 bits

$= 2^{15} \times 64$ bits

$\boxed{\text{Address pins} = 15}$

Saved address pins = 18 – 15

= 3

2. (b)

$$\text{Number of RAMS required} = \frac{32k \times 32 \text{bits}}{128 \times 8 \text{ bits}}$$

$$= \frac{2^{15} \times 2^5}{2^7 \times 2^3} = 2^{10} = 1024$$

3. (c)

Word size = 32 bits

= 4 bytes

= 1 w

Instruction	Size in bytes
I_1	16 (4w) 2000 – 2003
I_2	12 (3w) 2004 – 2006
I_3	16 (4w) 2007 – 2010
I_4	12 (3w) 2011 – 2013
I_5	8 (2w) $\boxed{2014}$ – 2015
I_6	8 (2w) 2016 – 2017
	2018

During the execution of I_4 instruction program counter will hold the address I_5 Instruction.

Ans = 2014

4. (d)

A → (iii) B → (iv)

C → (i) D → (ii)

5. (c)

The given program will read a number from memory at location 8000H and store it in memory location 8001 H.

6. (c)

Memory is byte addressable!

Instruction	Size in bytes
I_1	2 1000 – 1001
I_2	4 1002 – 1005
I_3	4 1006 – 1009
I_4	4 1010 – 1013
I_5	2 1014 – 1015
I_6	6 $\boxed{1016}$ – 1021

During the execution of I_5 instruction the program counter will hold the start address of I_6 instruction.

$\boxed{\text{Ans.} = 1016}$

7. (4)

As me have 8 data lines in dataline, at a point of time or in a cycle, 8 bits data can be transferred, So if we want to access 32 bits then $\frac{32}{8} = 4$ cycles are required so 4 memory access.

8. (c)

Both the given statement are true about memory address interpretation.

9. (a)

S_1 (True): Accumulators stores the results of calculations made by ALU.

S_2(False): Program counter keeps track of the memory location of the next instruction to be deals with but not the current instruction.

10. (a, b, c, d)

(a) **True:** Memory address stores the memory location of instruction that are needed to be fetched from memory.

(b) **True:** Memory data register stores the instruction fetched from memory or any data that is to be transferred to and stored in memory.

(c) **True:** Current instruction register stores the most recently fetched instructions.

(d) **True:** Instruction buffer register contains the instructions which are not to executed immediately.

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