



COMPUTER SCIENCE

Computer Organization and Architecture

Instruction Pipelining

Lecture_02

Vijay Agarwal sir





TOPICS
TO BE
COVERED

o1

Pipelining Concepts

Pipeline

Execution time in Pipeline

& in Non pipeline

Speed up Factor [Performance Gain]

Uniform Delay Pipeline

Non Uniform Delay Pipeline

Pipelining Strategy

Similar to the use of
An assembly line in a
Manufacturing plant

To apply this concept
To instruction
Execution we must
Recognize that an
Instruction has a
Number of stages



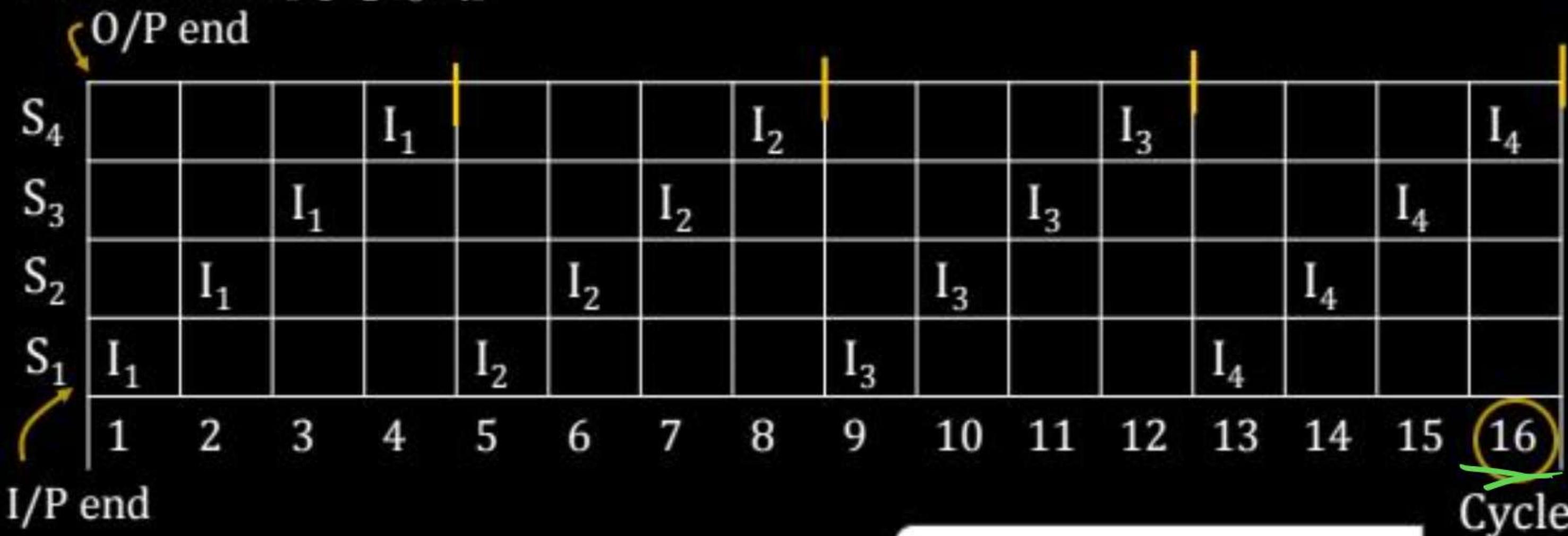
New inputs are
Accepted at one end
Before previously
Accepted inputs
Appear as output at
The other end

- Pipelining is a mechanism which is used to improve the performance of the system in which task (Instruction) are executed in overlapping manner.
- Pipelining is a decomposition technique that means the problem is divided into sub problem & Assign the sub problem to the pipes then operate the pipe under the same clock.

Let us consider 4 segment pipeline used to execute 4 instructions the execution sequence as:

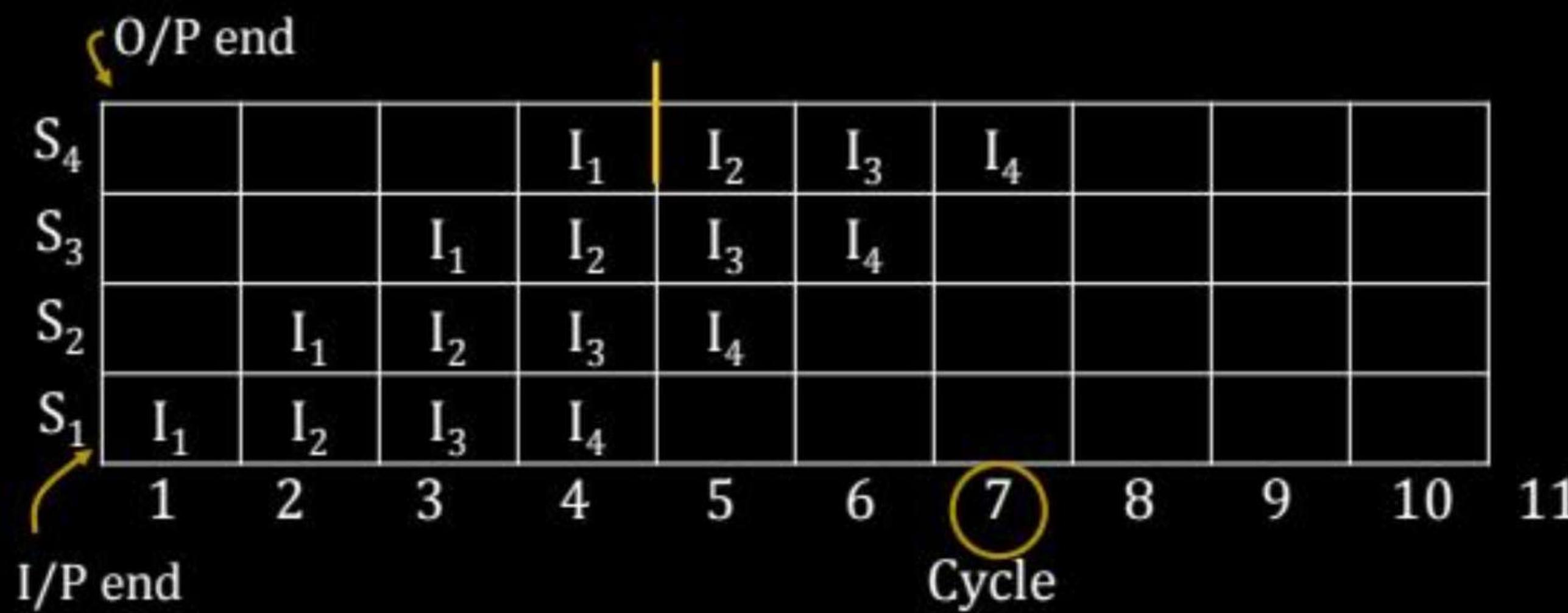
Segment/stages = $[S_1 \ S_2 \ S_3 \ S_4]$

Instruction: $[I_1 \ I_2 \ I_3 \ I_4]$



$n = 4, t_n = 4$, Non pipeline

Non-PIPELINE



PIPELINE

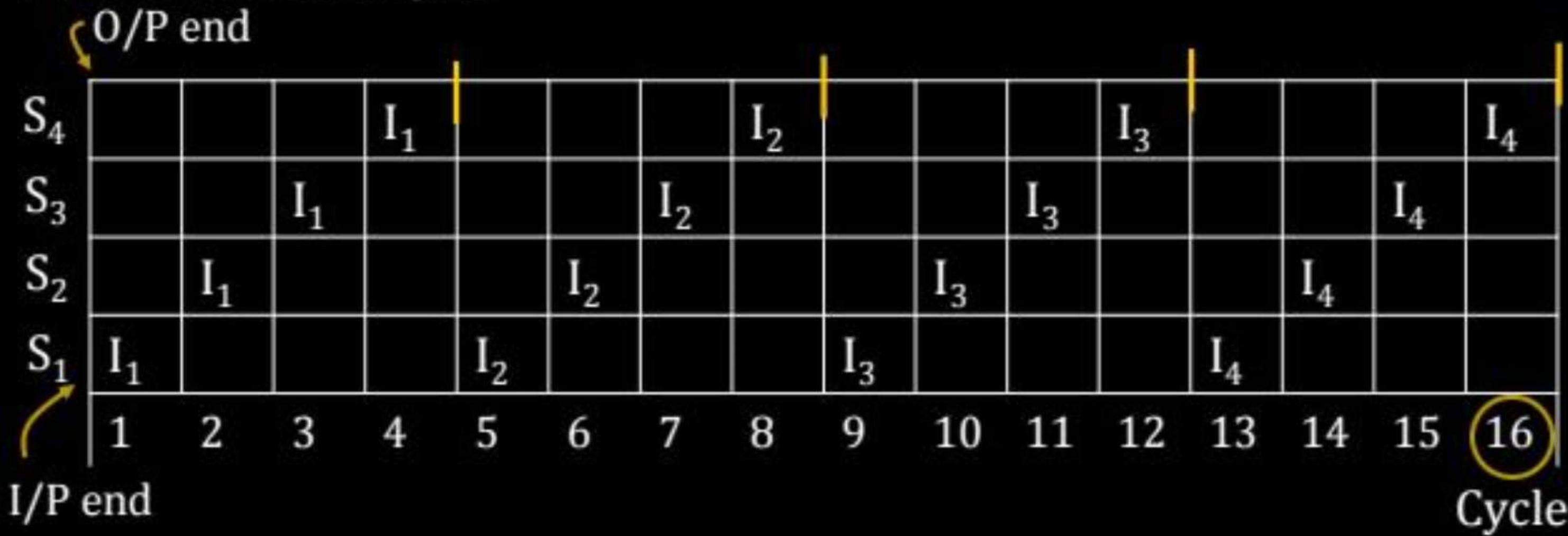
 $k = 4$ $n = 4$

PIPELINE

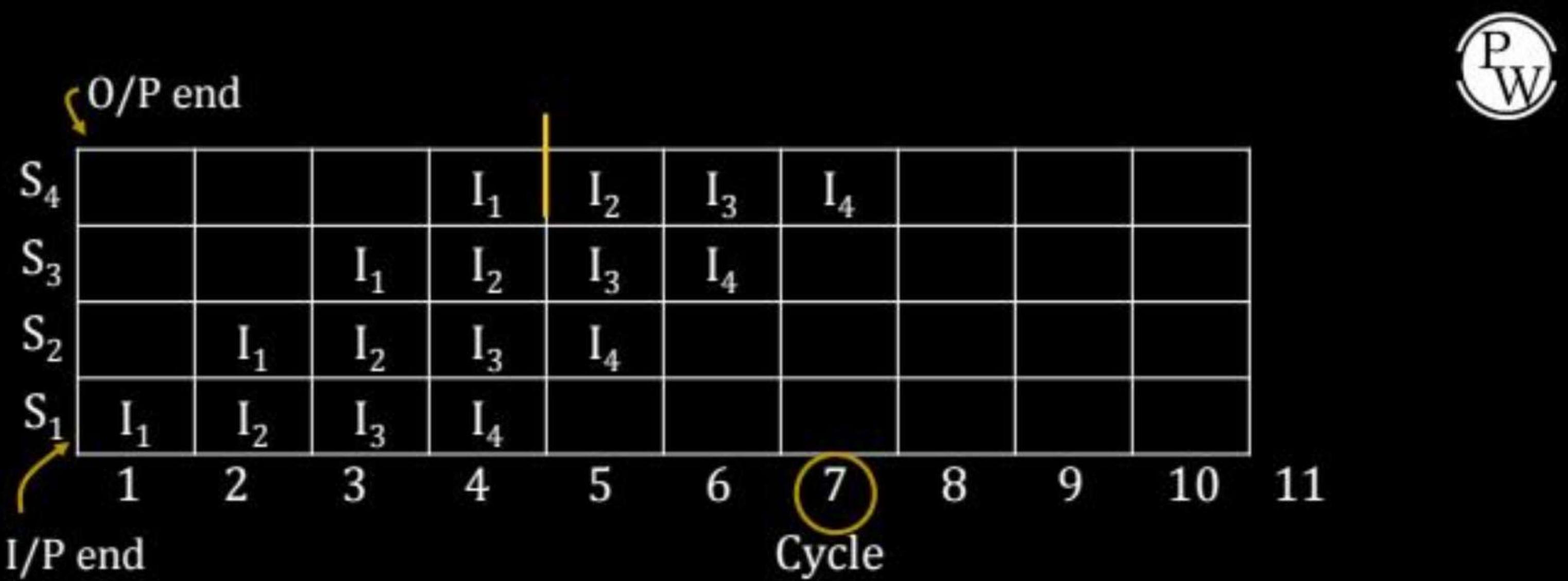
Let us consider 4 segment pipeline used to execute 4 instruction the execution sequence as: PIPELINING

Segment/stages = $[S_1 \ S_2 \ S_3 \ S_4]$

Instruction: $[I_1 \ I_2 \ I_3 \ I_4]$



$$n = 4, t_n = 4, \text{ Non pipeline}$$

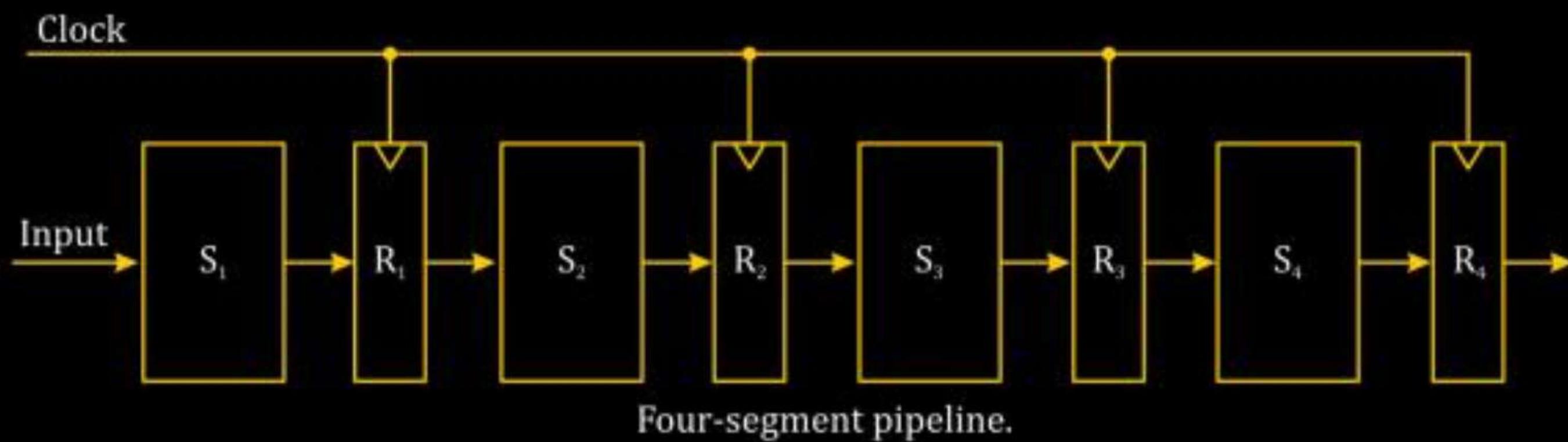


PIPELINE

$k = 4$

$n = 4$

PIPELINE Design



PIPELINE Performance Evaluation

Now consider the case where a k -segment pipeline with a clock cycle time t_p , is used to execute n tasks.

The first task T_1 requires a time equal to kt_p , to complete its operation since there are k segments in the pipe.

The remaining $n - 1$ tasks emerge from the pipe at the rate of one task per clock cycle and they will be completed after a time equal to $(n - 1)t_p$.

Therefore, to complete n tasks using a k -segment pipeline requires $k + (n - 1)$ clock cycles.

Space-time diagram for pipeline.

Segment:

	1	2	3	4	5	6	7	8	9	→ Clock Cycles
1	T_1	T_2	T_3	T_4	T_5	T_6				
2		T_1	T_2	T_3	T_4	T_5	T_6			
3			T_1	T_2	T_3	T_4	T_5	T_6		
4				T_1	T_2	T_3	T_4	T_5	T_6	

For example, the diagram of Fig. 9-4 shows four segments and six tasks. The time required to complete all the operations is $4 + (6 - 1) = 9$ clock cycles, as indicated in the diagram.

So, to complete n tasks using a k -segment pipeline is:

$$\text{ET pipe} = k + (n - 1) \text{ clock cycles}$$

$$ET_{PIPE} = [k + (n - 1)] t_p$$

So, to complete n tasks in Non-pipeline is:

$$\text{ET Non-pipeline} = n * t_n$$

Speed up factor = $\frac{\text{ET}_{\text{NP}}}{\text{ET}_{\text{PIPELINE}}}$

$$S = \frac{n t_n}{[k + (n-1)] t_p}$$

$$S = \frac{nt_n}{(k+n-1)t_p}$$

As the number of tasks increases, n becomes much larger than $k - 1$, and $k + n - 1$ approaches the value of n . Under this condition, the speedup becomes

$$S = \frac{t_n}{t_p}$$

$$\eta = \frac{S}{K}$$

η : efficiency

S: speed up factor

K: No. of stages/segment

Additional Stages

- ❑ Fetch Instruction (FI)
 - ❖ Read the next expected Instruction into a buffer.
- ❑ Decode Instruction (DI)
 - ❖ Determine the opcode and the operand specifiers.
- ❑ Calculate operands(CO)
 - ❖ Calculate the effective address of each source operand.
 - ❖ This may involve displacement, register indirect or other forms of address calculations.
- ❑ Fetch Operands(FO)
 - ❖ Fetch each operand from memory.
 - ❖ Operands in register need not be fetched.
- ❑ Executed Instruction(EI)
 - ❖ Perform the indicated operation and store the result, if any, in the specified destination operand location
- ❑ Write Operand(WO)
 - ❖ Store the result in memory

	Time →													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	FI	DI	CO	FO	EI	WO								
Instruction 2		FI	DI	CO	FO	EI	WO							
Instruction 3			FI	DI	CO	FO	EI	WO						
Instruction 4				FI	DI	CO	FO	EI	WO					
Instruction 5					FI	DI	CO	FO	EI	WO				
Instruction 6						FI	DI	CO	FO	EI	WO			
Instruction 7							FI	DI	CO	FO	EI	WO		
Instruction 8								FI	DI	CO	FO	EI	WO	
Instruction 9									FI	DI	CO	FO	EI	WO

Timing Diagram for Instruction pipeline operation

$$ET_{PIPE-LINE} = [k + (n-1)] t_p$$

$$ET_{NONPIPE-LINE} = n t_n$$

$$S = \frac{n t_n}{[k + (n-1)] t_p}$$

When n is very large \textcircled{a} Not given

$$S = \frac{t_n}{t_p}$$

(Rate of DIP)

$$\text{Throughput} = \frac{n}{[k + (n-1)] t_p}$$

$$\text{Throughput} = \frac{1}{t_p}$$

Non Uniform Delay

$$t_p = \max(\text{Stage Delay})$$

If Buffer Delay is given

$$t_p = \max \left[(\text{Stage Delay} + \text{Buffer Delay}) \right]$$

Uniform Delay PIPELINE

$$t_p = \text{Stage Delay}$$

If Buffer Delay is given

$$t_p = \text{Stage Delay} + \text{Buffer Delay}$$

Q. 1

Consider an instruction pipeline which has speed up factor 20 while operate with 80% efficiency. What could be the number of stages in the pipeline?

Soln

$$S = 20$$

$$\eta = 80\%$$

$$\eta = \frac{S}{K}$$

$$80\% = \frac{20}{K}$$

$K = 25$ Ans

$$K = \frac{20}{0.80} \times 100 = 25$$

A pipeline is having speed up factor as 10 and operating with efficiency of 80%. What will be the number of stages in the pipeline?

A 10

B 13

C 8

D None

$$S = 10$$
$$\eta = 80\%$$

$$\eta = \frac{S}{K}$$

$$80 = \frac{10}{K}$$

$$K = \frac{10}{80} \times 100 = 12.5$$

Avg(B)

K = 13 Avg

Q. 2

4 segment pipeline have the respective stage delay of 10ns, 15ns, 20ns and 30ns. What is the efficiency of the pipeline when very large number of task are executed?

Solv 2

$$\# \text{Stages} (k) = 4$$

$$t_P = \text{maximum} (10, 15, 20, 30)$$

$$t_P = 30 \text{ sec.}$$

$$t_n = 10 + 15 + 20 + 30$$

$$t_n = 75$$

$$S = \frac{t_n}{t_P} = \frac{75}{30} = 2.5$$

$$\eta = \frac{S}{K} \Rightarrow \frac{2.5}{4} = 0.625$$

$$= 62.5\% \text{ Ans}$$

Q. 3

A 4 segment instruction pipeline has the respective stage delay of 8ns, 11ns 20ns, 2ns respectively. The interface register are used between the stages have a delay of 2ns. What is the approx. speed up factor when very large number of task are pipelined?

Sol'n 3

$$t_p = \max \left(\text{Stage Delay} + \text{Buffer Delay} \right)$$

$$\Rightarrow (8, 11, 20, 2) + 2 \text{ ns}$$

$$t_p = 22 \text{ nsec.}$$

$$t_n = 8 + 11 + 20 + 2$$

$$t_n = 41 \text{ nsec.}$$

$$S = \frac{t_n}{t_p} = \frac{41}{22} = 1.86$$

$$S = 1.8 \text{ Ans}$$

(Note)

In Non pipeline we Not Using Buffer Delay bcz
in Non pipeline we are Not Storing the Intermediate Result.

Q. 4

Consider 4 stage pipeline with the respective stage delay of 20ns, 80ns, 50ns and 10ns. In the enhancement process of the pipeline largest stage is split into 2 equal stage delay.

- (i) What is speed up between new and old design?
- (ii) What is the clock frequency of new pipeline?

$k = 4$

Stage Delays = 20ns, 80ns, 50ns, 10ns

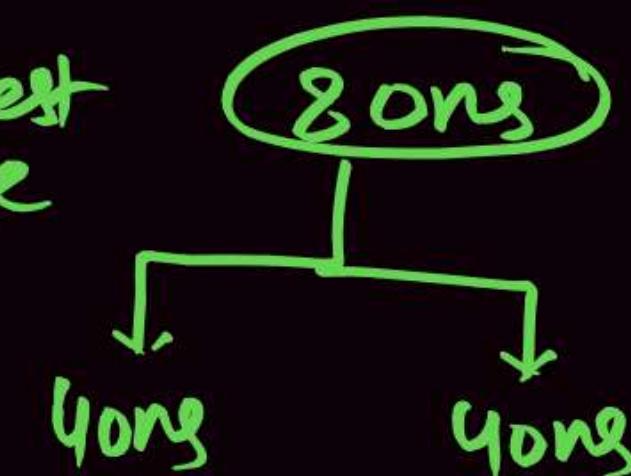
$$t_{p_{old}} = \max(20, 80, 50, 10)$$

$t_{p_{old}}$ 80 ns

(i) Ans (1.c)

(ii) Ans (20MHz)

New Design : \rightarrow largest stage



[20, 40, 40, 50, 10]

$$t_{P_{\text{new}}} = \max(20, 40, 40, 50, 10)$$

$$t_{P_{\text{new}}} = 50 \text{ nsec}$$

(ii) $t_{P_{\text{new}}} = 50 \text{ nsec}$
(cycle time)

$$\frac{\text{Speedup Factor}}{\text{}} = \frac{ET_{\text{old}}}{ET_{\text{new}}} = \frac{80}{50} = 1.6$$

$$S = 1.6 \quad \underline{\text{Ans}}$$

$$\text{Frequency} = \frac{1}{T} \text{ (cycle time)}$$

$$\begin{aligned} & \frac{1}{50 \times 10^{-9}} \Rightarrow \frac{1}{50} \times 10^9 \\ & = \frac{1000}{50} \times 10^6 = 20 \text{ MHz} \quad \underline{\text{Ans}} \end{aligned}$$

Q. 5

The stage delays in 5 stage pipeline are 900, 600, 550, 450 and 400 nanoseconds. The largest stage delay is replaced with a functionally equivalent design involving two stages with respective stage delay 440 and 460 nanoseconds. What is the throughput increase of the pipeline?

- (a) 25%
- (b) 33.3%
- (c) 50%
- (d) Does not change

Ans(c)

OLD Design : 900, 600, 550, 450, 400 ns

$$tp_{\text{old}} = \max(900, 600, 550, 450, 400)$$

$$tp_{\text{old}} = 900 \text{ ns}$$

$$1 \text{ Instn taken} = 900 \times 10^{-9} \text{ sec}$$

In 1 sec
(Per time Unit)
the #Instn executed = $\frac{1}{900 \text{ ns}}$

$$\text{Throughput}_{\text{old}} = \frac{1}{900}$$

New Design: 440, 460, 600, 550, 450, 400 ns

$$tp_{\text{new}} = \max(440, 460, 600, 550, 450, 400)$$

$$tp_{\text{new}} = 600 \text{ ns}$$

$$\text{Throughput}_{\text{new}} = \frac{1}{tp} = \frac{1}{600 \text{ ns}}$$

$$\text{Throughput}_{\text{new}} = \frac{1}{600}$$

(Profit & Loss
CHAPTER)

% of Increment in the
Throughput = $\frac{\text{New} - \text{OLD}}{\text{OLD}}$

$$\Rightarrow \frac{\frac{1}{600} - \frac{1}{900}}{\frac{1}{900}} \Rightarrow \frac{\frac{1}{6} - \frac{1}{9}}{\frac{1}{9}}$$

$$\Rightarrow \frac{9-6}{54} \times \frac{9}{1}$$

$$\Rightarrow \frac{3}{54} \times \frac{9}{1} = \frac{27}{54} = \frac{1}{2} = 50\%$$

GATE-QUESTIONS

Q. 1

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

[GATE-2004: 2 Marks]

$$t_p = \max(\frac{\text{Stage Delay} + \text{Buffer Delay}}{\text{Delay}}) = \frac{160 + 5}{K(\# \text{Stages})} = 165 \text{ nsec}$$

$$\text{Stage Delays} = (150, 120, 160, 140)$$

A 120.4 microseconds

B 160.5 microseconds

C 165.5 microseconds

D 590.0 microseconds

$$\text{Buffer Delay} = 5 \text{ nsec} \quad n = 1000$$

$$ET_{\text{PIPELINE}} = [k + (n-1)] t_p \Rightarrow [4 + (1000-1)] \times 165 \times 10^{-9}$$

$$\Rightarrow \frac{1003 \times 165 \times 10^{-9}}{\Rightarrow 165.5 \times 10^{-6}}$$

165.5 Microsecond.

Q. 2

We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time.

How much time can be saved using design D2 over design D1 for executing 100 instructions? [GATE-2005: 2 Marks]

- A 214 nseconds
- B 202 nseconds
- C 86 nseconds
- D -200 nsecond

Ans(B).

Design D₁

$$k=5$$

$$t_p: \max(3, 2, 4, 2, 3)$$

$$n=100$$

$$\boxed{t_p = 4 \text{nsec}}$$

$$ET_{PIPE} = [k + (n-1)] t_p$$

$$\Rightarrow [5 + (100-1)] \times 4$$

$$= 104 \times 4$$

$$\boxed{D_1 \quad ET_{PIPE} = 416 \text{nsec.}}$$

Design D₂

$$k=8 \quad t_p=2 \text{nsec} \quad n=100$$

$$ET_{D_2} = [k + (n-1)] t_p$$

$$\Rightarrow [8 + (100-1)] \times 2 \Rightarrow 107 \times 2$$

$$\boxed{ET_{D_2} = 214 \text{nsec}}$$

$$\begin{aligned} \text{Time Saved} &= 416 - 214 \\ &= 202 \text{nsec.} \end{aligned}$$

~~Q. 3~~

~~freq~~

A nonpipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is [GATE-2008: 2 Marks]

- A 4.5
- B 4.0
- C 3.33
- D 3.0

Ans [C].

Non Pipeline

100 MHz

$$\text{Cycle time} = \frac{1}{100 \times 10^6} \text{ sec} \Rightarrow \frac{1}{10^8} \times \frac{10}{10}$$

$$\Rightarrow 10 \times 10^{-9}$$

$t_n = 10 \text{ nsec}$

X

$$t_n = 2.5 + 1.5 + 2 + 1.5 + 2.5$$

$t_n = 10 \text{ nsec}$

X Wrong Bcz
Non Pipeline
is given

Non Pipeline
is given

Pipeline

Stage Delays : 2.5, 1.5, 2, 1.5, 2.5 nsec

$$\text{Buffer Delay} = 0.5$$

$$t_p = \max \left(\begin{array}{l} \text{Stage Delay} + \text{Buffer Delay} \\ 2.5 + 0.5 \end{array} \right)$$

$t_p = 3 \text{ nsec}$

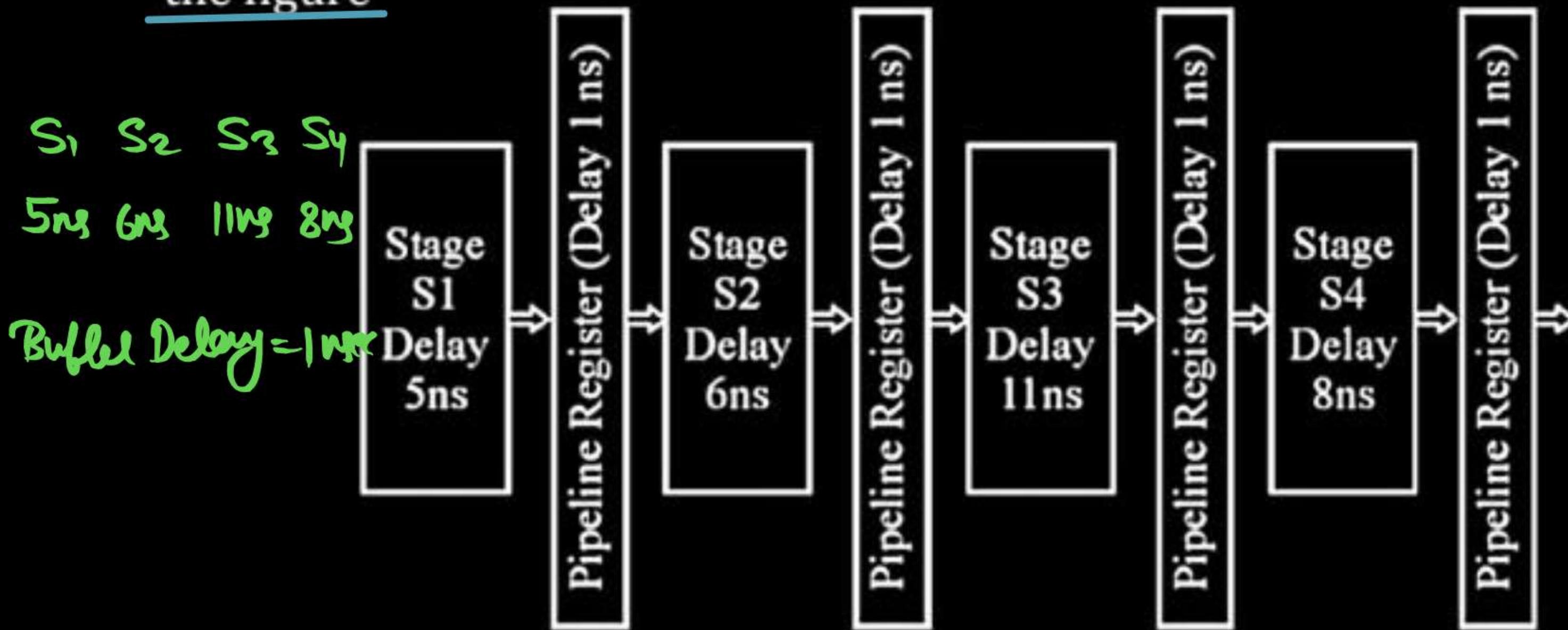
$$S = \frac{t_n}{t_p} = \frac{10}{3}$$

$S = 3.33$

Avg

Q. 4

Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure



$S_1 \ S_2 \ S_3 \ S_4$
 5ns 6ns 11ns 8ns & Buffer Delay = 1nscc
 Delay = 1nscc

$$t_p = \max \left(\frac{\text{Stage Delay}}{11+1} + \frac{\text{Buffer Delay}}{1} \right)$$

$$t_p = 12 \text{ nsec}$$

$$t_n = 5 + 6 + 11 + 8$$

$$t_n = 30 \text{ nsec}$$

$$S = \frac{t_n}{t_p}$$

$$= \frac{30}{12} = 2.5 \text{ Avg}$$

What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

[GATE-2011: 2 Marks]

A 4.0

B 2.5

C 1.1

D 3.0

A five-stage pipeline has stage delays of 150, 120, 150, 160 and 140 nanoseconds. The registers that are used between the pipeline stages have a delay of 5 nanoseconds each.

The total time to execute 100 independent instructions on this pipeline, assuming there are no pipeline stalls, is 17160 nanoseconds.

Stage Delay = 150, 120, 150, 160, 140 nsec. [GATE-2021(Set-1)-CS: 2M]

Buffer Delay = 5 nsec

$$t_p = \max \left[(\text{Stage Delay} + \text{Buffer Delay}) \right]$$

$$t_p = 165 \text{ nsec}$$

$$k = 5, \quad n = 100.$$

$$\begin{aligned} ET_{PIPE} &= (k + (n - 1)) t_p \\ &= (5 + (100 - 1)) \times 165 \\ &= 104 \times 165 \end{aligned}$$

$$ET_{PIPE} = 17160 \text{ nsec. Ans}$$

Consider a 3-stage pipelined processor having a delay of 10 ns (nanoseconds), 20 ns, and 14 ns, for the first, second, and the third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also assume that one instruction is fetched every cycle.

The total execution time for executing 100 instructions on this processor is

2040 ns. Avg

$s_1 \ s_2 \ s_3$

[GATE-2023-CS: 1M]

$k=3,$

$n=100$

Stage Delay = 10ns, 20ns, 14nssec.

$$\begin{aligned} ET_{PIPE} &= (k + (n-1)) t_p \\ &= [3 + (100-1)] \times 20 \\ &= 102 \times 20 \end{aligned}$$

$ET_{PIPE} = 2040 \text{ nsec.}$

Avg

Instruction execution in a processor is divided into 5 stages. Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Back (WB). These stages take 5, 4, 20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns.

Two pipelined implementations of the processor are contemplated:

- (I) a naive pipeline implementation (NP) with 5 stages and
- (II) an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is 1.5. Ans

[GATE-2017(Set-1)-CS: 2M]

NP

Stage Delay : 5, 4, 20, 10, 3

Buffer Delay = 2 nsec

$$t_P = \max \left(\frac{\text{Stage Delay}}{20+2} + \text{Buffer Delay} \right)$$

$$t_P = 22 \text{ nsec}$$

$$\begin{aligned} K &= 5 \\ n &= 20 \end{aligned}$$

$$\begin{aligned} ET_{NP} &= [K + (n-1)] t_P \\ &= [5 + (20-1)] \times 22 \\ &= 24 \times 22 \end{aligned}$$

$$ET_{NP} = 528 \text{ nsec.}$$

$\frac{P_{EP}}{P_{NP}}$

E.P [Efficient Pipeline]

$$\text{Stage Delay} = [5, 4, 19, 8, 10, 3]$$

$$\text{Bubble Delay} = 2n_3 \quad (12+2)$$

$$t_P = 14 \text{ nsec}$$
 $k=6$ $n=20.$

$$\begin{aligned} ET_{EP} &= [k + (n-1)] t_P \\ &= [6 + (20-1)] \times 14 \\ &= 25 \times 14 \end{aligned}$$

$$ET_{EP} = 350 \text{ nsec.}$$

$$\text{Speed Up factor} = \frac{\text{Performance of EP}}{\text{Performance of NP}}$$

$$\Rightarrow \frac{ET_{NP}}{ET_{EP}}$$

$$= \frac{528}{350}$$

$$S = 1.5 \quad \text{Ans}$$

MCQ

Q. 8



Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

P1: Four -stage pipeline with stage latencies (1ns, 2 ns, 2 ns, 1 ns.) $t_p = 2 \text{ ns}$

P2: Four-stage pipeline with stage latencies 1ns, 1.5 ns, 1.5 ns, 1.5 ns. $t_p : 1.5 \text{ ns}$

P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns. 1 ns. $t_p = 1 \text{ ns}$

P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns. $t_p = 1.1 \text{ ns}$

Which processor has the highest peak clock frequency?

[GATE-2014(Set-3)-CS: 1M]

A P1

B P2

$$\text{freq} \propto \frac{1}{\text{Time}}$$

C P3

D P4

Ans (C).

$$P_1 : t_p = \max(1, 2, 2, 1)$$

$$t_p = \underline{2 \text{ nsec}}$$

$$P_2 : t_p = \max(1, 1.5, 1.5, 1.5)$$

$$t_p = \underline{1.5 \text{ nsec}}$$

$$P_3 : t_p = \max(0.5, 1, 1, 0.6, 1)$$

$$t_p = \underline{1 \text{ nsec}}$$

$$P_4 : t_p = \max(0.5, 0.5, 1, 1, 1.1)$$

$$t_p = \underline{1.1 \text{ nsec}}$$

Frequency $\propto \frac{1}{\text{Time}}$

P_3 having the lowest time

So P_3 frequency Highest.

The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is 33.3 percent.

$$t_p = \max(800, 500, 400, 300)$$

$$t_p = 800 \text{ PS}$$

$$\text{Throughput} = \frac{1}{800}$$

[GATE-2016(Set-1)-CS: 2M]

New Design

$$t_{p\text{new}} = (600, 350, 500, 400, 300)$$

$$t_{p\text{new}} = 600 \text{ PS}$$

$$\text{Throughput}_{\text{new}} = \frac{1}{600}$$

% increment in throughput = $\frac{\text{New} - \text{Old}}{\text{Old}}$

$$= \frac{\frac{1}{600} - \frac{1}{800}}{\frac{1}{800}} \Rightarrow \frac{\frac{1}{6} - \frac{1}{8}}{\frac{1}{8}}$$

$$\Rightarrow \frac{8-6}{48} \times \frac{8}{1}$$

$$\Rightarrow \frac{2 \times 8}{48} = \frac{16}{48} = \frac{1}{3}$$

= 33.333...% Avg

Avg(33.333...%)

Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is ____.

[GATE-2015(Set-1)-CS: 2M]

MCQ Q. 11

Consider a 4-stage pipeline processor. We want to execute a loop:
For($i=1; i \leq 1000; i++$) { I1, I2, I3, I4} where the time taken (in ns) by instruction I1 to I4 for stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

The Output of I1 for $i=2$ will be available after ?

[GATE-2004-CS: 2M]

A 11ns

B 12ns

C 13ns

D 28ns

MCQ Q. 12

Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
for (i = 1 to 2) {I1; I2; I3; I4;}

[GATE-2009-CS: 2M]

A 16

B 23

C 28

D 30

Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies τ_1 , τ_2 , and τ_3 such that $\tau_1 = 3\tau_2/4 = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is _____ GHz, ignoring delays in the pipeline registers.

[GATE-2016(Set-2)-CS: 2M]

NAT Q. 14

Consider two processors P_1 and P_2 executing the same instructions set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1 . If the clock frequency of P_1 is 1GHz, then the clock frequency of P_2 (in GHz) is _____.

[GATE-2014(Set-1)-CS: 2M]

MCQ Q. 15



Consider the following processor design characteristics:

- I. Register-to-register arithmetic operations only.
- II. Fixed-length instruction format.
- III. Hardwired control unit.

Which of the characteristics above are used in the design of a RISC processor?

[GATE-2018-CS: 1M]

A I and II only

B II and III only

C I and III only

D I, II and III

Consider a machine with 40 MHz processor which has run a benchmark program. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count. What will be the effective CPI, MIPS rate, and execution time.

Instruction Type	Instruction Count	Cycles/ Instructions
Integer arithmetic	45000	1
Data Transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

-  A CPI:3.55; MIPS: 30; Execution time:1.87 ms
-  B CPI:1.55; MIPS: 25.8; Execution time:3.87 ms
-  C CPI:5.60; MIPS: 45.8; Execution time:2.87 ms
-  D CPI:2.55; MIPS: 35.8; Execution time:4.87 ms

Which of the following is not a form of main memory ?

- A Instruction cache
- B Instruction register
- C Instruction opcode
- D Translation look-aside buffer

Q.

COA 2017: CS

NIC PYQ SERIES

PW

In a 10-bit computer instruction format, the size of address field is 3-bits. The computer uses expanding OP code technique and has 4 two-address instructions and 16 one-address instructions. The number of zero address instructions it can support is

A 256

C 640

B 356

D 756

A micro programmed control unit

- (A) is faster than a hardwired unit
- (B) Facilitates easy implementation of a new instruction
- (C) is useful when small programs are to be run
- (D) All of the above

**THANK
YOU!**

