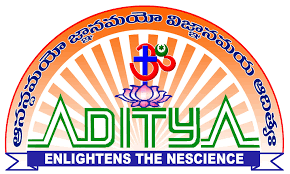
**ADITYA ENGINEERING COLLEGE(A)**

(Approved by AICTE, Accredited by NAAC with ‘A’ Grade, Recognized by UGC under the sections 2(f) and 12(b) of UGC Act 1956)



**LABORATORY MANUAL**

**ELECTRONIC CIRCUIT ANALYSIS LAB**

Regulations : AR 20

Course Code : 201EC4L02

Semester : IV

**Department of**

**Electronics and Communication Engineering**

Prepared by

**Mr. M. Neeladri, Assoc. Prof.**

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## 

## 

**ELECTRONIC CIRCUIT ANALYSIS LAB**

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**LIST OF EXPERIMENTS**

**Part-A: Design & Simulation in Simulation Laboratory using Multisim or PSPICE or**

**Equivalent Simulation Software**

1. Two Stage RC Coupled Amplifier
2. RC Phase Shift Oscillator
3. Class-A Power Amplifier
4. Voltage series feedback amplifier
5. Single Tuned Voltage Amplifier

**Part-B: List of Experiments has to be performed using hardware**

1. Two Stage RC Coupled Amplifier

2. RC Phase Shift Oscillator

3. Class-A Power Amplifier

4. Single Tuned Voltage Amplifier

5. Voltage-Series Feedback Amplifier

**List of Augmented Experiments**

**(Any two of the following experiments can be performed)**

1. Three Stage RC Coupled Amplifier

2. Darlington pair amplifier

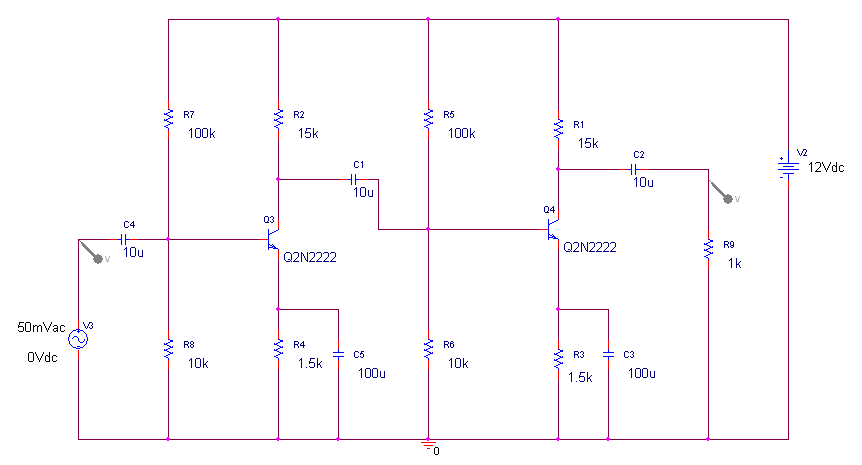
3. Colpitt's oscillator

4. Bootstrapped emitter follower

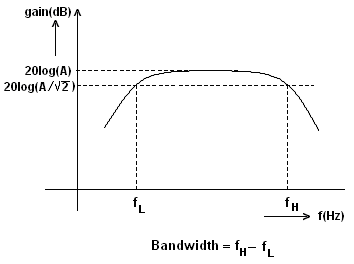
**ELECTRONIC CIRCUIT ANALYSIS SOFTWARE**

**1. TWO STAGE RC COUPLED AMPLIFIER**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

TWO STAGE RC COUPLED AMPLIFIER

**AIM:** To obtain the frequency response of two stage RC coupled amplifier using P-spice software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N2222 | 2 |
| RESISTORS | 100kΩ | 2 |
| 10kΩ | 2 |
| 15kΩ | 2 |
| 1.5kΩ | 2 |
| 1kΩ | 1 |
| CAPACITORS | 100μF | 2 |
| 10μF | 3 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC-coupled amplifier. Frequency response of an amplifier is defined as the variation of gain with respective frequency.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 1000mega
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Max. Gain in dB |  |
|  |  |  |
| 2 | 3dB Gain |  |
|  |  |  |
| 3 | Lower Cutoff Frequency |  |
|  |  |  |
| 4 | Upper Cutoff Frequency |  |
|  |  |  |
| 5 | Bandwidth |  |
|  |  |  |

The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases. At low frequencies the reactance of coupling capacitor CC is quite high and hence very small part of signal will pass through from one stage to the next stage. At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies. At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, where as inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier goes for simulation settings and set the analysis type as AC sweep/noise, start frequency, end frequency, points/decade.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Calculate the gain using the formula 20log 10(Vo/Vi).
6. Set the lower &higher cutoff frequency and calculate the bandwidth.

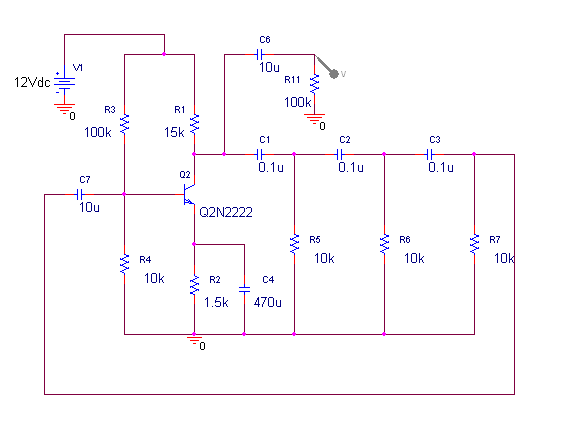
**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

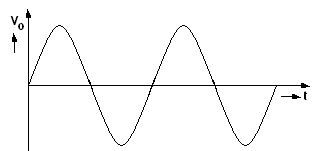
**RESULT:**

**2. RC PHASE SHIFT OSCILLATOR**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

RC PHASE SHIFT OSCILLATOR

**AIM:** To observe the operation of RC phase shift oscillator using P-spice software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N2222 | 1 |
| RESISTORS | 100kΩ | 2 |
| 10kΩ | 4 |
| 15kΩ | 1 |
| 22kΩ | 1 |
| 1.5kΩ | 1 |
| CAPACITORS | 0.1μF | 3 |
| 10uF | 2 |
| 470μF | 1 |
| SOURCES | Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

An oscillator is a device which generates an alternative voltage. This may also be defined as a circuit which generates an AC output signal without requiring any externally applied input signal. The oscillator converts DC energy into AC energy at a very high frequency. So the function of an oscillator is opposite to that of a rectifier which converts AC power into DC power. The essential requirement is that there must be 1800 phase shift around the feedback network and loop gain should be greater than unity. The 1800 phase shift in feed back signal can be achieved by a suitable RC network consisting of three RC sections. Here RC network produces a phase shift of 1800 between input and output voltages. Since CE amplifier produces a phase of 1800 , the total phase change becomes 3600 or 00 which is essential requirement of sustained oscillations. The RC phase shift networks serve as frequency determining circuit. Since only at single frequency the net phase shift around the loop will be 3600, a sinusoidal waveform at this frequency is generated.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : Time domain
* RUN TIME :1.6
* MAXIMUM STEP SIZE :1m
* START SAVING DATA :1.45

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Peak to peak amplitude |  |
|  |  |  |
| 2 | Time period |  |
|  |  |  |
| 3 | Frequency |  |
|  |  |  |

**CALCULATIONS:**

Frequency f = f=

Where k = =

R =

C =

f=

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier, go for simulation settings and set the analysis type as time domain (transient), run to time, maximum step size etc.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Set the minimum and maximum points of the waves.

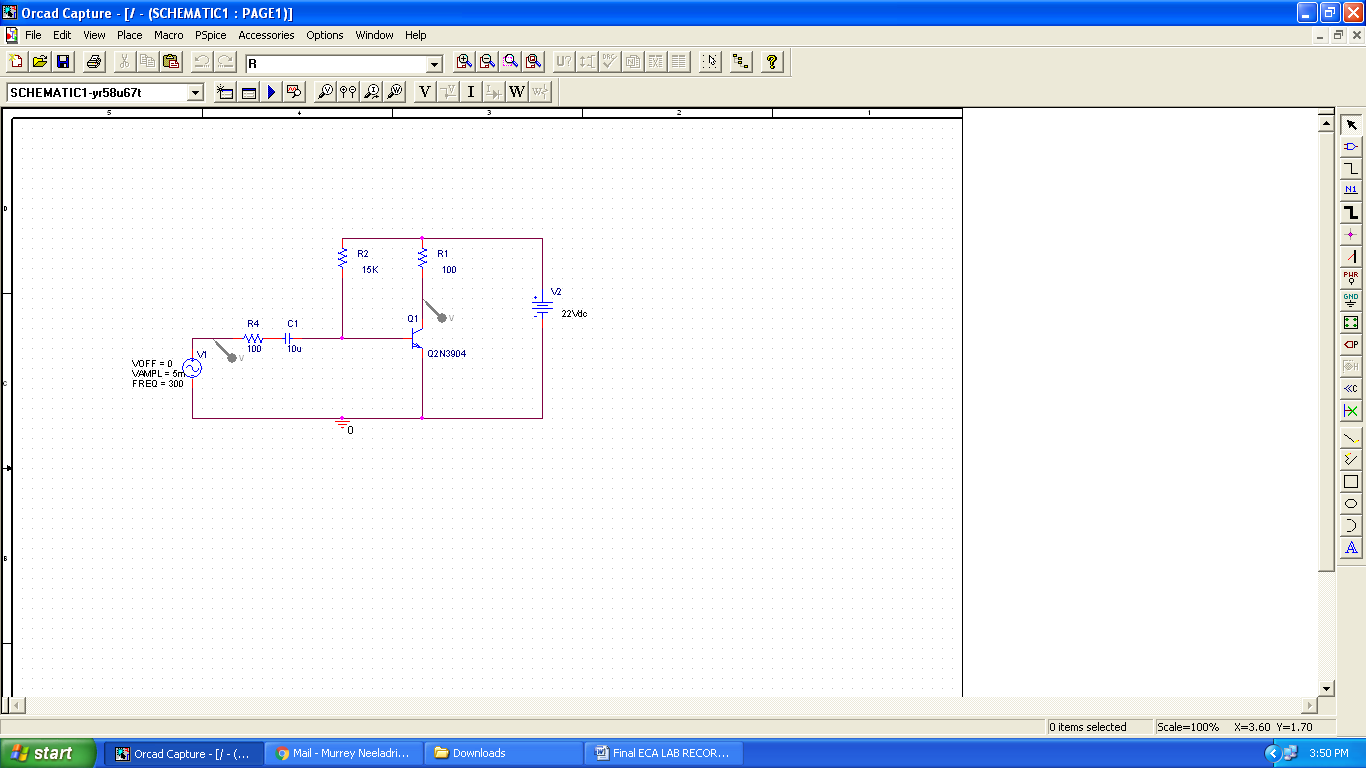
**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

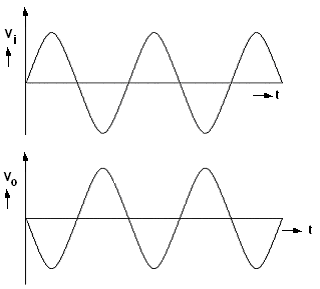
**RESULT:**

**3. CLASS A POWER AMPLIFIER**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

CLASS A POWER AMPLIFIER

**AIM:** To observe the operation of class A power amplifier using P-spice software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N3904 | 1 |
| RESISTORS | 15kΩ | 1 |
| 100Ω | 2 |
| CAPACITORS | 10μF | 1 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

The main function of the [Power Amplifier](http://www.amazon.com/gp/aws/cart/add.html?ASIN.1=007164024X&Quantity.1=1&AWSAccessKeyId=AKIAIOB4VMPIMBIMN7NA&AssociateTag=basicelecttut-20), which are also known as a “large signal amplifier” is to deliver power, which is the product of voltage and current to the load. Basically a power amplifier is also a voltage amplifier the difference being that the load resistance connected to the output is relatively low, for example a loudspeaker of 4 or 8Ωs resulting in high currents flowing through the collector of the transistor. The power amplifier is said to be class A amplifier if the Q-point and the input signal are selected such that the output signal is obtained for full input cycle. For this class position of the Q-point is approximately at the mid point of the load line.For all the values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an ac signal is applied, the collector current flows for 3600 (full cycle) of the input signal. In other words, the angle of the collector current flow is 3600 i.e. one full cycle.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : Time domain
* RUN TIME : 1.6
* MAXIMUM STEP SIZE : 100u
* START SAVING DATA :1.58

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Input voltage(Peak to peak) |  |
|  |  |  |
| 2 | output voltage(Peak to peak) |  |
|  |  |  |
| 3 | Phase shift |  |
|  |  |  |

**CALCULATIONS:**

Efficiancy (ῃ) = \* 100

Pac =

Pdc =Vcc Ic =

Efficiency (ῃ) = \* 100

Efficiancy (ῃ)

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier, go for simulation settings and set the analysis type as time domain (transient), run to time, maximum step size etc.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Observe whether the waveforms are out of phase or not.
6. Set the minimum and maximum points of the waves.

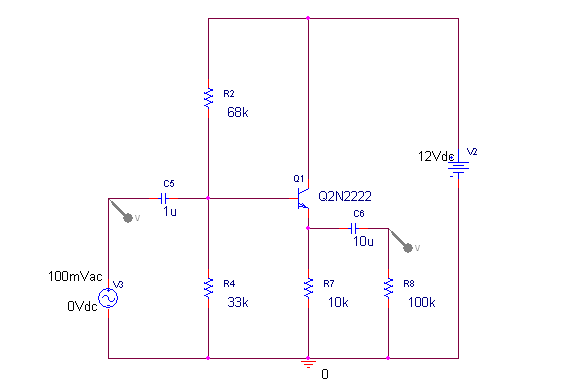
**PRECAUTIONS:**

1. Connect the circuit without any loose connections.
2. Use the components with proper values.
3. Ground the circuit properly.

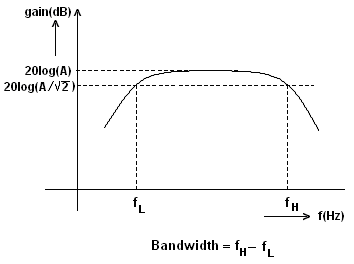
**RESULT**

**4. VOLTAGE SERIES FEEDBACK AMPLIFIER**

**CIRCUIT DIAGRAM:**



**MODEL GRAPH:**



Expt.No: Date:

**VOLTAGE SERIES FEEDBACK AMPLIFIER**

**AIM:** To plot the frequency response of voltage series feedback amplifier using P-spice software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| EQUIPMENT/COMPONENT | SPECIFICATIONS | QUANTITY |
| TRANSISTOR | Q2N2222 | 1 |
| RESISTORS | 33kΩ | 1 |
| 68kΩ | 1 |
| 10kΩ | 1 |
| 100kΩ | 1 |
| CAPACITORS | 1μF | 1 |
| 10μF | 1 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback.The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 100 giga
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Max. Gain in dB |  |
|  |  |  |
| 2 | 3dB Gain |  |
|  |  |  |
| 3 | Lower Cutoff Frequency |  |
|  |  |  |
| 4 | Upper Cutoff Frequency |  |
|  |  |  |
| 5 | Bandwidth |  |
|  |  |  |

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier goes for simulation settings and set the analysis type as AC sweep/noise, start frequency, end frequency, points/decade.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Calculate the gain using the formula 20log 10(Vo/Vi).
6. Set the lower &higher cutoff frequency and calculate the bandwidth.

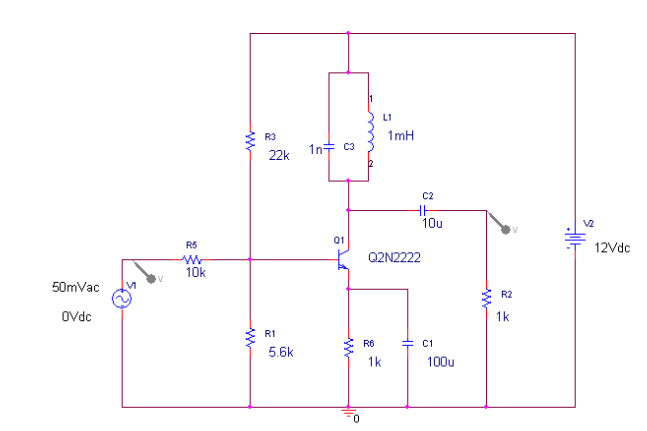
**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

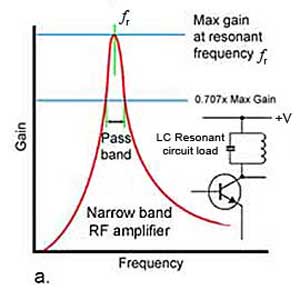
**RESULT**

**5. SINGLE TUNED AMPLIFIER**

**CIRCUIT DIAGRAM:**



**MODEL GRAPH:**



Expt.No: Date:

**SINGLE TUNED AMPLIFIER**

**AIM:** To plot the frequency response characteristics of single tuned amplifier.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N2222 | 1 |
| RESISTORS | 22k | 1 |
| 5.6k,10k | 1 |
| 1k | 2 |
| CAPACITORS | 10uf | 1 |
| 100uf | 1 |
| INDUCTORS | 1mH | 1 |
| SOURCES | Vdc(12V) | 1 |
| Vac(50mV,0Vdc) | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:** Amplifiers which amplify a specific frequency or narrow band of frequencies are called Tuned amplifiers. Tuned amplifiers are mostly used for the amplification of high or radio frequencies. It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single. Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at resonant frequency and very small impedance all other frequencies.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 1000mega
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Output values** |
|  |  |  |
| 1. | Maximum gain |  |
|  |  |  |
| 2. | Lower cutoff frequency |  |
|  |  |  |
| 3. | Upper cutoff frequency |  |
|  |  |  |
| 4. | Bandwidth |  |
|  |  |  |

**CALCULATION**:

Frequency f =

Frequency f

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. After connecting the circuit of the amplifier, apply an AC input voltage of 40mv.
3. Observe the input and output waveforms on CRO.
4. Take the readings of input and output waveforms.
5. Draw the waveforms on graph sheet.

**PRECAUTIONS:**

1. Connect the circuit without any loose connections.
2. Verify the circuit before switch ON the supply.

**RESULT:**

**SIMULATION SETTINGS**

|  |  |  |  |
| --- | --- | --- | --- |
| **Analysis Type - AC Sweep Noise** | | | |
| **Name of the Experiment** | **Start**  **Frequency** | **End**  **Frequency** | **Decade Points** |
| Two Stage RC Coupled Amplifier | 1 | 1000mega | 20 |
| Voltage Series Feedback Amplifier | 1 | 1000giga | 20 |
| Single Tuned Amplifier | 1 | 1000giga | 20 |
| Three Stage RC Coupled Amplifier | 1 | 1000mega | 20 |
| **Analysis Type - Time Domain** | | | |
| **Name of the Experiment** | **Run Time** | **Start saving data after** | **Maximum step size** |
| RC Phase Shift Oscillator | 1.6 s | 1.45 s | 1 ms |
| Class A Power Amplifier | 1.6 s | 1.58 s | 100 u |
| Colpitts Oscillator | 1.402 s | 1.4 s | 10 u |

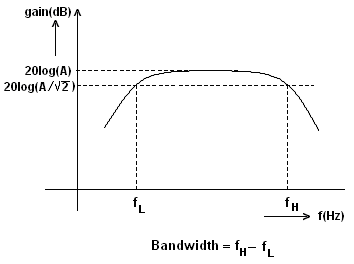
**ELECTRONIC CIRCUIT ANALYSIS HARDWARE**

**1. TWO STAGE RC COUPLED AMPLIFIER**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

TWO STAGE RC COUPLED AMPLIFIER

**AIM:** To obtain the frequency response, output impedance and Q-point of two stage RC coupled amplifier.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | BC107 | 2 |
| RESISTORS | 33K,3.3K, 1.5K,330ohms | 2 |
| CAPACITORS | 100 uf | 2 |
| 10uf | 3 |
| CATHODE RAY OSCILLOSCOPE |  | 1 |
| FUNCTION GENERATOR |  | 1 |
| REGULATED POWER SUPPLY | Vdc(12V, 6V) | 1 |
| BREAD BOARD |  | 1 |
| CONNECTING WIRES |  | few |

**THEORY:**

As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC-coupled amplifier. Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases

**OBSERVATIONS:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S. No | Vi(V) | Freq. (Hz) | Vo(V) | Av=Vo/Vi | Gain =20log (Av) |
| 1.  2.  3.  4.  5.  6.  7.  8.  9.  10.  11.  12..  13.  14.  15. | 50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV |  |  |  |  |

At low frequencies the reactance of coupling capacitor CC is quite high and hence very small part of signal will pass through from one stage to the next stage. At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies. At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, where as inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. After connecting the circuit of the amplifier, apply an input voltage of 50mv.
3. Now by varying the frequency on function generator observe the output on CRO.
4. Take the readings and calculate the gain using the formula 20log10 (Vo/Vi).
5. Draw the graph on semi log graph sheet.
6. Set the lower &higher cutoff frequency and calculate the bandwidth using the formula

### BW = fH – fL

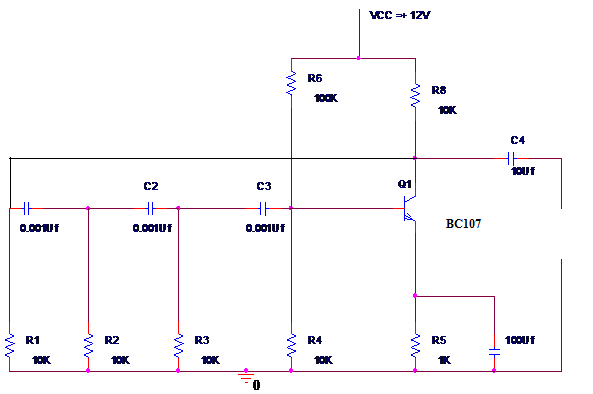
**PRECAUTIONS:**

1. Connect the circuit without any loose connections.
2. Verify the circuit before switch ON the supply.

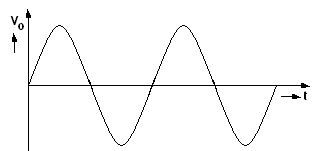
**RESULT:**

**2. RC PHASE SHIFT OSCILLATOR**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

RC PHASE SHIFT OSCILLATOR

**AIM:** To observe the operation and to find the frequency of the RC-phase shift oscillator.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | BC107 | 2 |
| RESISTORS | 10k | 5 |
| 1k | 1 |
| 100k | 1 |
| CAPACITORS | 10uf 100uf | 1 |
| 0.001uf | 3 |
| CATHODE RAY OSCILLOSCOPE |  | 1 |
| REGULATED POWER SUPPLY | Vdc(12V) | 1 |
| BREAD BOARD |  | 1 |
| CONNECTING WIRES |  | few |

**THEORY:**

An oscillator is a device which generates an alternative voltage. This may also be defined as a circuit which generates an AC output signal without requiring any externally applied input signal. The oscillator converts DC energy into AC energy at a very high frequency. So the function of an oscillator is opposite to that of a rectifier which converts AC power into DC power.

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Peak to peak amplitude |  |
|  |  |  |
| 2 | Time period |  |
|  |  |  |
| 3 | Frequency |  |
|  |  |  |

**CALCULATIONS:**

Frequency f = f=

Where k = =

R =

C =

f=

The essential requirement is that there must be 1800 phase shift around the feedback network and loop gain should be greater than unity. The 1800 phase shift in feed back signal can be achieved by a suitable RC network consisting of three RC sections. Here RC network produces a phase shift of 1800 between input and output voltages. Since CE amplifier produces a phase of 1800 , the total phase change becomes 3600 or 00 which is essential requirement of sustained oscillations. The RC phase shift networks serve as frequency determining circuit. Since only at single frequency the net phase shift around the loop will be 3600, a sinusoidal waveform at this frequency is generated. These oscillators are used for audio frequency ranges. LC tuned circuits at low frequencies becomes to much bulky and expensive and moreover they suffer from frequency instability and poor waveform.

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. Observe the output of the circuit on the CRO and the measure the frequency of the o/p waveform.
3. The theoretical value is calculated by using the formula



where K=Rc/R

1. Compare it with the theoretical frequency.

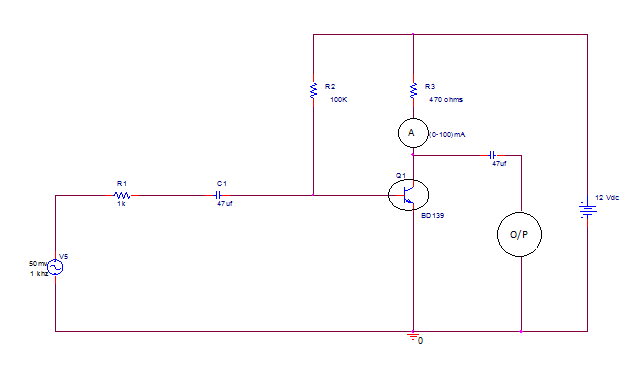
PRECAUTIONS:

1. Connect the circuit without any loose connections.
2. Verify the circuit before switch ON the supply.

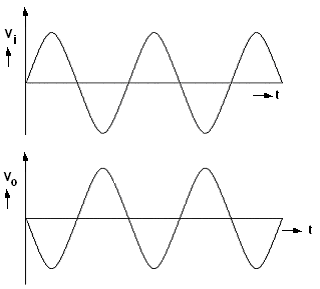
**RESULT:**

**3. CLASS -A POWER AMPLIFIER**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

CLASS A POWER AMPLIFIER

**AIM:** To observe the efficiency and Q-point of series fed class A power amplifier.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | BD139 | 1 |
| RESISTORS | 1k | 1 |
| 100k | 1 |
| 470 Ohms | 1 |
| CAPACITORS | 47uf | 2 |
| CATHODE RAY OSCILLOSCOPE |  | 1 |
| FUNCTION GENERATOR | 50mV,1Khz | 1 |
| REGULATED POWER SUPPLY | Vdc(12V) | 1 |
| AMMETER | (0-100)mA | 1 |
| BREADBOARD |  | 1 |
| CONNECTING WIRES |  | few |

**THEORY:** The power amplifier is said to be class A amplifier if the Q-point and the input signal are selected such that the output signal is obtained for full input cycle. For this class position of the Q-point is approximately at the mid point of the load line.For all the values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an ac signal is applied, the collector current flows for 3600 (full cycle) of the input signal. In other words, the angle of the collector current flow is 3600 i.e. one full cycle.

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Peak to peak amplitude |  |
|  |  |  |
| 2 | Time period |  |
|  |  |  |
| 3 | Frequency |  |
|  |  |  |

**CALCULATIONS:**

Efficiancy (ῃ) = \* 100

Pac = =

Pdc =Vcc Ic =

Efficiency (ῃ) = \* 100

Efficiancy (ῃ)

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. After connecting the circuit of the amplifier, apply an input voltage of 50mv.
3. Observe the input and output waveforms on CRO.
4. Take the readings of input and output waveforms and calculate efficiency.
5. Draw the waveforms on graph sheet.

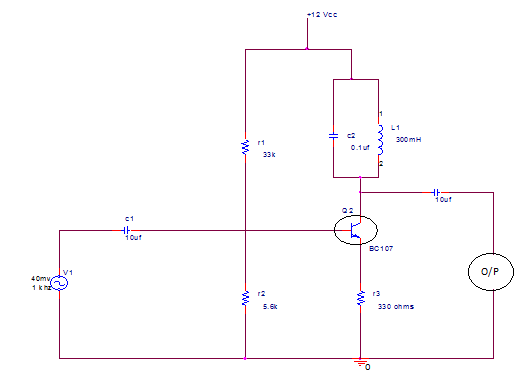
**PRECAUTIONS:**

1. Connect the circuit without any loose connections.
2. Verify the circuit before switch ON the supply.

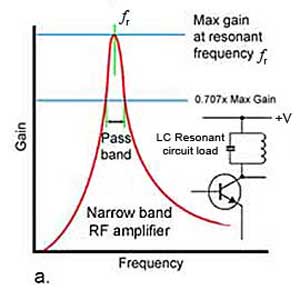
**RESULT:**

**4. SINGLE TUNED AMPLIFIER**

**CIRCUIT DIAGRAM:**



**MODEL GRAPH:**



Expt.No: Date:

**SINGLE TUNED AMPLIFIER**

**AIM:** To plot the frequency response characteristics of single tuned amplifier.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | BC107 | 1 |
| RESISTORS | 33k | 1 |
| 5.6k | 1 |
| 330ohms | 1 |
| CAPACITORS | 10uf | 2 |
| 0.1uf | 1 |
| INDUCTORS | 300mH | 1 |
| SOURCES | Vdc(12V) | 1 |
| Vac(40mV,1Khz) | 1 |
| GROUND |  | 1 |

**THEORY:**

Amplifiers which amplify a specific frequency or narrow band of frequencies are called Tuned amplifiers. Tuned amplifiers are mostly used for the amplification of high or radio frequencies. It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single. Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at resonant frequency and very small impedance all other frequencies.

**OBSERVATIONS:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S. No | Vi(V) | Freq. (Hz) | Vo(V) | Av=Vo/Vi |
| 1.  2.  3.  4.  5.  6.  7.  8.  9.  10.  11.  12..  13.  14.  15. | 50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV  50mV |  |  |  |

**CALCULATIONS:**

Frequency f =

Frequency f

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.

2. After connecting the circuit of the amplifier, apply an AC input voltage of 40mv.

3.Observe the input and output waveforms on CRO.

4**.** Take the readings of input and output waveforms.

5. Draw the waveforms on graph sheet.

**PRECAUTIONS:**

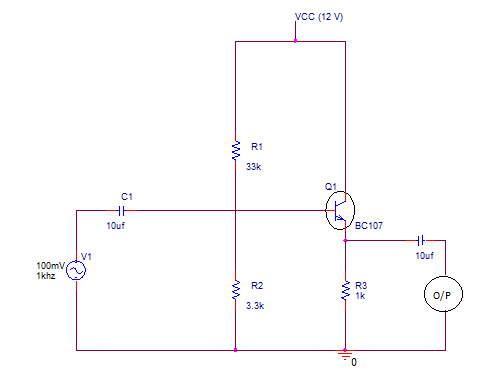
1. Connect the circuit without any loose connections.

2. Verify the circuit before switch ON the supply.

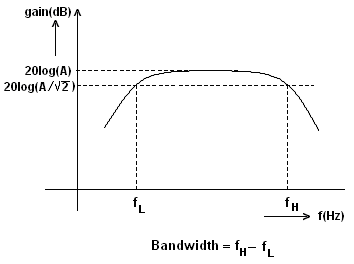
**RESULT:**

**5. VOLTAGE SERIES FEEDBACK AMPLIFIER**

**CIRCUIT DIAGRAM:**



**MODEL GRAPH:**



Expt.No: Date:

**VOLTAGE SERIES FEEDBACK AMPLIFIER**

**AIM:** To plot the frequency response and output impedance of voltage series feedback amplifier.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| EQUIPMENT/COMPONENT | SPECIFICATIONS | QUANTITY |
| TRANSISTOR | BC107 | 1 |
| RESISTORS | 33kΩ | 1 |
| 3.3kΩ | 1 |
| CAPACITORS | 10μF | 2 |
| SOURCES | Function generator | 1 |
| DC power supply | 1 |
| CRO |  | 1 |

**THEORY:**

When any increase in the output signal results into the input in such a way as to cause the decrease in the output signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that by proper use of this, there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. This disadvantage of the negative feedback is that the voltage gain is decreased.

**OBSERVATIONS:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S. No | Vi(V) | Freq (Hz) | Vo(V) | Av=Vo/Vi | Gain =20log (Av) |
| 1.  2.  3.  4.  5.  6.  7.  8.  9.  10.  11.  12..  13.  14.  15. | 100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV  100mV |  |  |  |  |

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.

2. After connecting the circuit of the amplifier, apply an input voltage of 50mv.

3. Now by varying the frequency on function generator observe the output on CRO.

4. Take the readings and calculate the gain using the formula 20log10 (Vo/Vi).

5. Draw the graph on semi log graph sheet.

6. Set the lower &higher cutoff frequency and calculate the bandwidth using the formula

### BW = fH – fL

**PRECAUTIONS:**

1. Connect the circuit without any loose connections.

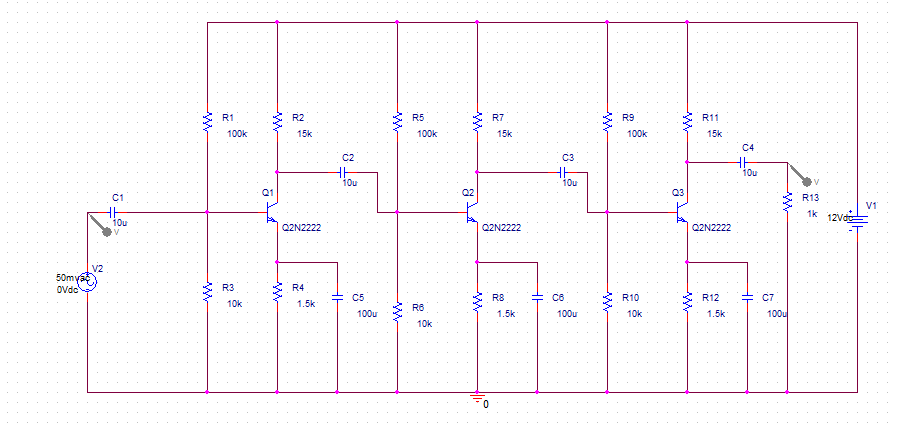
2. Verify the circuit before switch ON the supply.

**RESULT:**

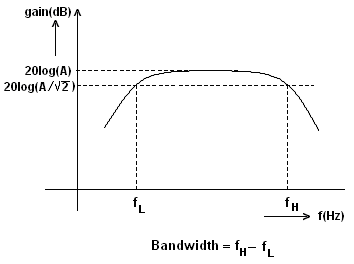
**ELECTRONIC CIRCUIT ANALYSIS AUGMENTED EXPERMENTS**

**1. THREE STAGE RC COUPLED AMPLIFIER USING PSPICE**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

THREE STAGE RC COUPLED AMPLIFIER

**AIM:** To obtain the frequency response of three stage RC coupled amplifier using P-spice software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N2222 | 3 |
| RESISTORS | 100kΩ | 3 |
| 10kΩ | 3 |
| 15kΩ | 3 |
| 1.5kΩ | 3 |
| 1kΩ | 1 |
| CAPACITORS | 100μF | 3 |
| 10μF | 4 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

As the gain provided by a single stage amplifier is usually not sufficient to drive the load, so to achieve extra gain multi-stage amplifier are used. In multi-stage amplifiers output of one-stage is coupled to the input of the next stage. The coupling of one stage to another is done with the help of some coupling devices. If it is coupled by RC then the amplifier is called RC-coupled amplifier. Frequency response of an amplifier is defined as the variation of gain with respective frequency.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 1000mega
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Max. Gain in dB |  |
|  |  |  |
| 2 | 3dB Gain |  |
|  |  |  |
| 3 | Lower Cutoff Frequency |  |
|  |  |  |
| 4 | Upper Cutoff Frequency |  |
|  |  |  |
| 5 | Bandwidth |  |
|  |  |  |

The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases. At low frequencies the reactance of coupling capacitor CC is quite high and hence very small part of signal will pass through from one stage to the next stage. At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies. At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, where as inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.

2. After connecting the circuit of the amplifier goes for simulation settings and set the analysis type as AC sweep/noise, start frequency, end frequency, points/decade.

3. Place the markers.

4. Simulate the circuit and observe the output.

5. Calculate the gain using the formula 20log 10(Vo/Vi).

6. Set the lower & higher cutoff frequency and calculate the bandwidth.

**PRECAUTIONS:**

1. Connect the circuit without errors.

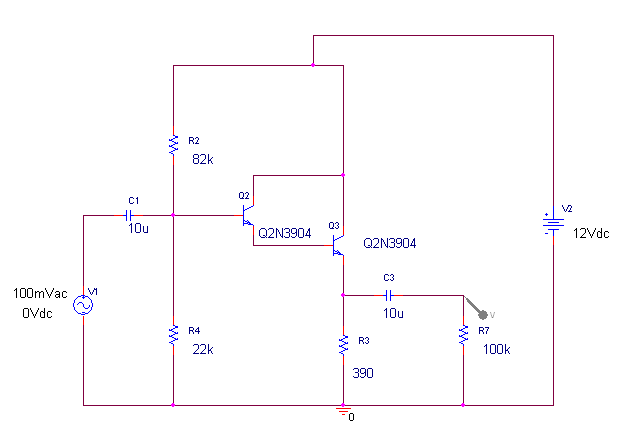
2. Use the circuit components with proper ratings.

3. Ground the circuit properly.

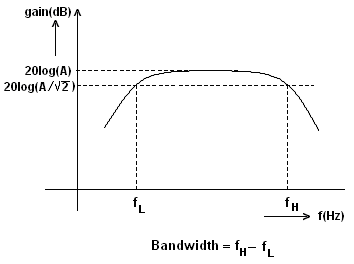
**RESULT:**

**2. DARLINGTON PAIR AMPLIFIER USING PSPICE**

**CIRCUIT DIAGRAM:**



**Model graph:**



Expt.No: Date:

**DARLINGTON PAIR AMPLIFIER**

**AIM:** To simulate the Darlington Pair amplifier in PSPICE and study the frequency response.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N3904 | 2 |
| RESISTORS | 100kΩ | 1 |
| 82kΩ | 1 |
| 22kΩ | 1 |
| 390Ω | 1 |
| CAPACITORS | 10μF | 2 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

Darlington transistor (often called a Darlington pair) is a compound structure consisting of two bipolar transistors (either integrated or separated devices) connected in such a way that the current amplified by the first transistor is amplified further by the second one. This configuration gives a much higher common/emitter current gain than each transistor taken separately and, in the case of integrated devices, can take less space than two individual transistors because they can use a *shared* collector. Integrated Darlington pairs come packaged singly in transistor-like packages or as an array of devices (usually eight) in an integrated circuit.The Darlington configuration was invented by Bell Laboratories engineer Sidney Darlington in 1953. He patented the idea of having two or three transistors on a single chip sharing a collector. A Darlington pair can be sensitive enough to respond to the current passed by skin contact even at safe voltages.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 1000mega
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Max. Gain in dB |  |
|  |  |  |
| 2 | 3dB Gain |  |
|  |  |  |
| 3 | Lower Cutoff Frequency |  |
|  |  |  |
| 4 | Upper Cutoff Frequency |  |
|  |  |  |
| 5 | Bandwidth |  |
|  |  |  |

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier goes for simulation settings and set the analysis type as AC sweep/noise, start frequency, end frequency, points/decade.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Calculate the gain using the formula 20log10 (Vo/Vi).
6. Set the lower &higher cutoff frequency and calculate the bandwidth.

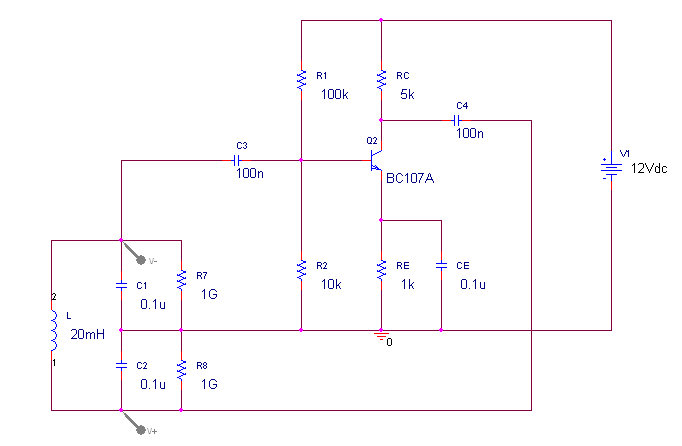
**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

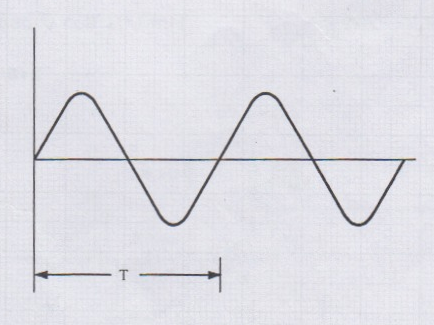
**RESULT:**

**3. COLPITT'S OSCILLATOR USING PSPICE**

**CIRCUIT DIAGRAM:**

****

**MODEL GRAPH:**

****

Expt.No: Date:

**COLPITTS OSCILLATOR**

**AIM:** To obtain the output waveform of a Colpitts oscillator using PSPICE software.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | BC107A | 1 |
| RESISTORS | 10kΩ | 1 |
| 100kΩ | 1 |
| 5kΩ | 1 |
| 1kΩ | 1 |
| 1GΩ | 2 |
| CAPACITORS | 100uF | 2 |
| 0.1μF | 2 |
| 20 µH | 1 |
| INDUCTORS | 20 mH | 1 |
| SOURCES | Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

The Colpitt’s oscillator is designed for generation of high frequency sinusoidal oscillations (radio frequencies ranging from 10KHz to 100MHz). They are widely used in commercial signal generators up to 100MHz. Colpitt's oscillator is same as Hartley oscillator except for one difference. Instead of using a tapped inductance,Colpitt's oscillator uses a tapped capacitance. The circuit diagram of Colpitt’s oscillator using BJT is shown in Fig. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R1 and R2 are two resistors which form a voltage divider bias to the transistor.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : Time domain
* RUN TIME : 1.402
* MAXIMUM STEP SIZE : 10u
* START SAVING DATA : 1.40

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Peak to peak amplitude |  |
|  |  |  |
| 2 | Time period |  |
|  |  |  |
| 3 | Frequency |  |
|  |  |  |

**CALCULATIONS:**

Frequency f = =

L=20mH Ceq **=**

Ceq =

f =

A resistor RE is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor CE is connected in parallel with RE, acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor CC blocks dc and provides an ac path from the collector to the tank circuit. The feedback network (tank circuit) consists of two capacitors C1 and C2 (in series) which placed across a common inductor L. The centre of the two capacitors is tapped (grounded). The feedback network (C1, C2 and L) determines the frequency of oscillation of the oscillator. The two series capacitors C1, and C2 form the potential divider led for providing the feedback voltage. The voltage developed across the capacitor C2 provides regenerative feedback which is essential for sustained oscillations.

Frequency f =

C =

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier, go for simulation settings and set the analysis type as time domain (transient), run to time, maximum step size etc.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Set the minimum and maximum points of the waves.

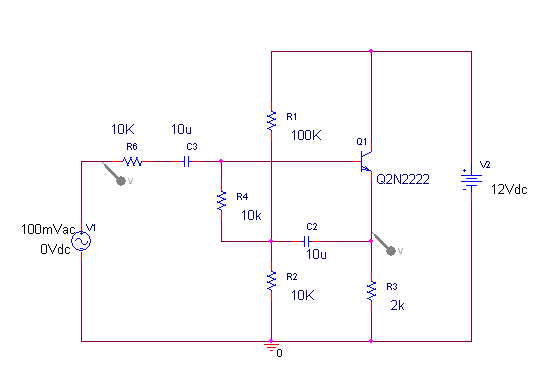
**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

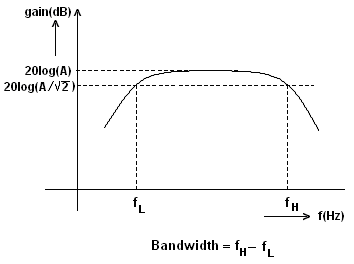
**RESULT**

**4. BOOTSTRAPPED EMITTER FOLLOWER USING PSPICE**

**CIRCUIT DIAGRAM:**

****

**MODEL GRAPH:**



Expt.No: Date:

**BOOTSTRAPPED EMITTER FOLLOWER**

**AIM:** To simulate the Bootstrapped Emitter Follower amplifier in PSPICE and study the frequency response.

**APPARATUS:**

|  |  |  |
| --- | --- | --- |
| **EQUIPMENT/COMPONENT** | **SPECIFICATIONS** | **QUANTITY** |
| TRANSISTOR | Q2N2222 | 1 |
| RESISTORS | 100kΩ | 1 |
| 10kΩ | 3 |
| 2kΩ | 1 |
| CAPACITORS | 10μF | 2 |
| SOURCES | Vac source | 1 |
| Vdc source | 1 |
| GROUND | (0) source ground | 1 |

**THEORY:**

So far, we have ignored the effect on input impedance of any base bias resistor networks shunted across the transistor input. showing an elementary single-resistor bias circuit, illustrates the problem. You will see that Rs is directly across the input . Obviously the total Rio cannot exceed RB. The conventional technique to raise the effective a.c. resistance of RB without raising its d.c. value is to boots trap it as shown in Fig. RB is replaced by two resistances RBl and RB2 of the same total resistance. Provided RBl and RB2 are large compared with RE, the transistor emitter-follower action makes the top end of RB2 move up and down with its bottom end. Thus its a.c. impedance is raised effectively by the current gain of the transistor. In [analog circuit](http://en.wikipedia.org/wiki/Analog_circuit) designs a bootstrap circuit is an arrangement of components deliberately intended to alter the[input impedance](http://en.wikipedia.org/wiki/Input_impedance) of a circuit.

**SIMULATION SETTINGS:**

* ANALYSIS TYPE : AC sweep noise
* START FREQUENCY : 1
* END FREQUENCY : 1000mega
* POINTS/DECADE : 20

**OBSERVATIONS:**

|  |  |  |
| --- | --- | --- |
| **S. No.** | **Parameter** | **Value** |
|  |  |  |
| 1 | Max. Gain in dB |  |
|  |  |  |
| 2 | 3dB Gain |  |
|  |  |  |
| 3 | Lower Cutoff Frequency |  |
|  |  |  |
| 4 | Upper Cutoff Frequency |  |
|  |  |  |
| 5 | Bandwidth |  |
|  |  |  |

Usually it is intended to increase the impedance, by using a small amount of positive [feedback](http://en.wikipedia.org/wiki/Feedback), usually over two stages. This was often necessary in the early days of [bipolar](http://en.wikipedia.org/wiki/Bipolar_junction_transistor) [transistors](http://en.wikipedia.org/wiki/Transistor), which inherently have quite a low input impedance. Because the feedback is positive, such circuits can suffer from poor stability and noise performance compared to ones that don't bootstrap. Negative feedback may alternatively be used to bootstrap an input impedance, causing the apparent impedance to be reduced.

**PROCEDURE:**

1. Connect the components as per the circuit diagram on computer using p-spice software.
2. After connecting the circuit of the amplifier goes for simulation settings and set the analysis type as AC sweep/noise, start frequency, end frequency, points/decade.
3. Place the markers.
4. Simulate the circuit and observe the output.
5. Calculate the gain using the formula 20log10 (Vo/Vi).
6. Set the lower &higher cutoff frequency and calculate the bandwidth.

**PRECAUTIONS:**

1. Connect the circuit without errors.
2. Use the circuit components with proper ratings.
3. Ground the circuit properly.

**RESULT:**