PLECS

DEMO MODEL

Synchronous Buck Converter

Last updated in PLECS 4.6.1

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1 Overview

This demonstration shows a regulated synchronous buck converter with a fixed load and switched load in parallel. Fig. 1 shows the electrical circuit schematic of the converter. A proportional integral derivative (PID) controller regulates the output voltage of the converter.

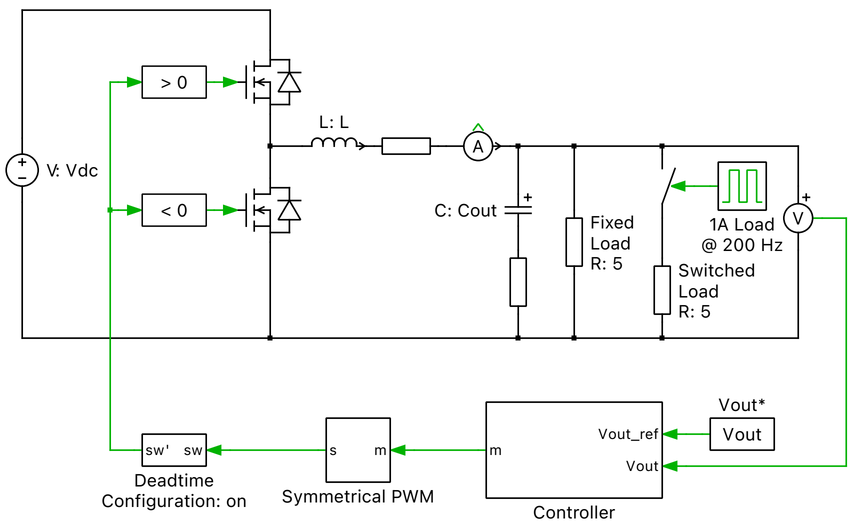

Figure 1: Synchronous buck converter

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power circuit

A synchronous buck converter topology is used to step down a $12\,\mathrm{VDC}$ input to produce $5\,\mathrm{VDC}$ at the output. The load consists of a $5\,\Omega$ fixed resistive load as well as a $5\,\Omega$ pulsed resistive load that cycles at $200\,\mathrm{Hz}$. In a synchronous buck converter the freewheeling diode is augmented by an active switch, which has the advantage of improved converter efficiency in practice, although on-resistance of the MOSFETs and thermal loss modeling have not been included in this example. As compared to a traditional buck converter, a synchronous buck converter always operates in continuous conduction mode (CCM) since current can reverse in the second MOSFET.

2.2 Controller

The high-level schematic of the controller implementation is shown in Fig. 2. The control consists of a voltage compensator and soft-start scheme to limit the inductor inrush current during startup. The soft-start scheme ramps the modulation index, m, until the output voltage reaches a defined threshold, at which point the voltage compensator generates the modulation index for closed-loop control.

In closed-loop control the output voltage is measured and compared with a $5\,\mathrm{VDC}$ set point. The sensed voltage error is the input to a Continuous PID Controller component from the PLECS Library. The controller gains are calculated using the buck converter parameters and the specified crossover frequency and phase margin [1]. The voltage controller determines the duty cycle of the FETs. The duty cycle range is limited between 1 % and 99 % by an anti-windup scheme that uses the Back-Calculation method.

The Symmetrical PWM component generates the gate signals for the MOSFETs using the modulation index from the soft-start scheme or voltage regulator. The two switches are modulated in a complementary manner. In practice, it is important not to gate both switches on at the same time to avoid shoot-through. This is prevented by introducing a dead time to delay the turn-on of the opposing switches.

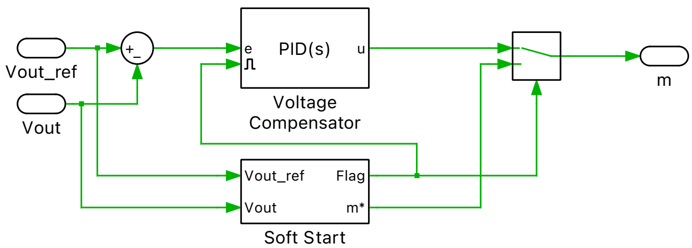

Figure 2: Top-level schematic of control system

3 Simulation

The simulation result shown in Fig. 3 demonstrates the start-up of the converter and two load current steps. During each load current change a transient in the output voltage and the response of the controller can be observed.

4 Conclusion

This model highlights a synchronous buck converter with a soft-start scheme and closed loop voltage regulation. It makes use of the Continuous PID Controller block from the PLECS component library.

References

[1] L. Corradini, Maksimović Dragan, P. Mattavelli, and R. Zane, *Digital control of high-frequency switched-mode power converters*. Hoboken, NJ: IEEE, John Wiley & Sons Inc., 2015.

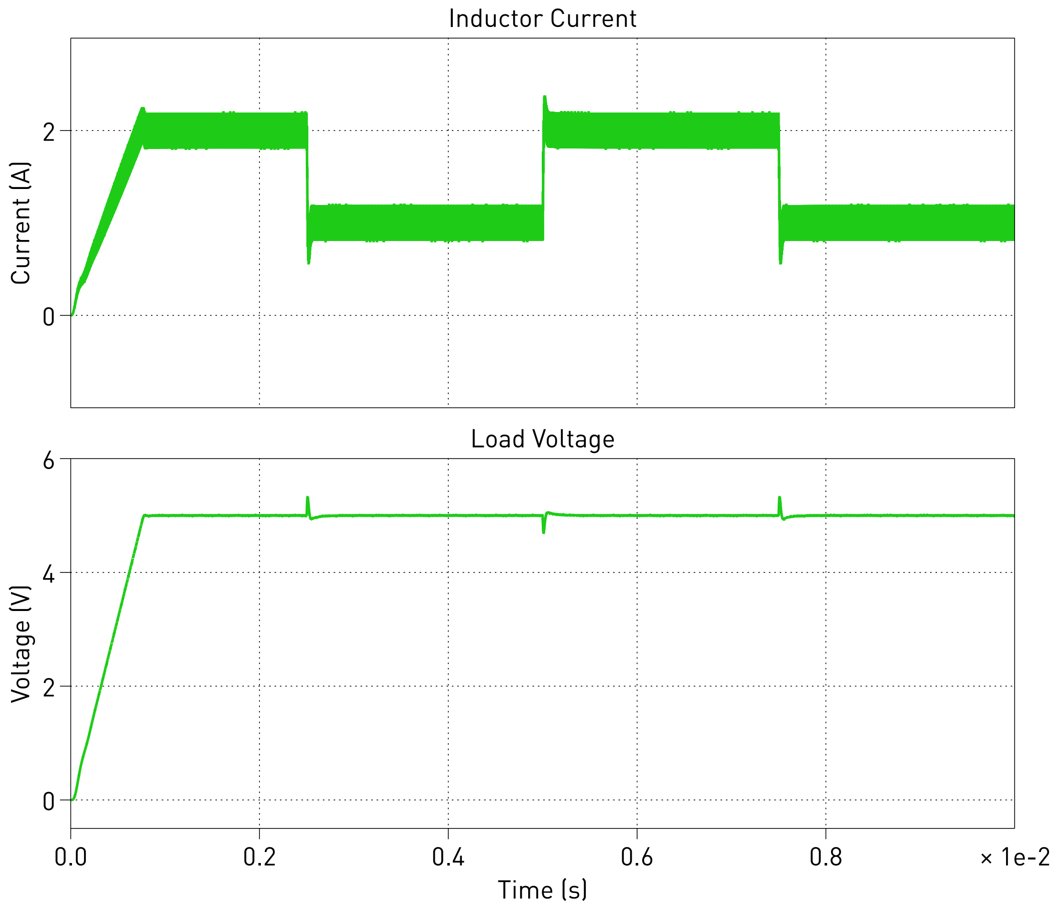

Figure 3: Simulation result of synchronous buck converter in closed loop under load step

Revision History:

PLECS 4.3.1	First release
PLECS 4.4.2	Updated the PI controller component
PLECS 4.5.5	Updated the PWM modulator
PLECS 4.6.1	Controller redisign

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