ESP32-C3-WROOM-02
ESP32-C3-WROOM-02U

Datasheet Version 1.4

2.4 GHz Wi-Fi (802.11b/g/n) and Bluetooth® 5 module

Built around ESP32-C3 series of SoCs, RISC-V single-core microprocessor

Flash up to 16 MB

15 GPIOs

On-board PCB antenna or external antenna connector

ESP32-C3-WROOM-02   ESP32-C3-WROOM-02U

ESPRESSIF

1   Module Overview

> **Note:**
>
> Check the link or the QR code to make sure that you use the latest version of this document:
> https://www.espressif.com/documentation/esp32-c3-wroom-02_datasheet_en.pdf

1.1   Features

CPU and On-Chip Memory

- ESP32-C3 embedded, 32-bit RISC-V single-core processor, up to 160 MHz
- 384 KB ROM
- 400 KB SRAM (16 KB for cache)
- 8 KB SRAM in RTC

Wi-Fi

- IEEE 802.11b/g/n-compliant
- Center frequency range of operating channel: 2412 ~ 2484 MHz
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
  Note that when ESP32-C3 series scans in Station mode, the SoftAP channel will change along with the Station channel
- 802.11mc FTM

Bluetooth®

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- Up to 15 GPIOs
  - 3 strapping GPIOs
- SPI, UART, I2C, I2S, remote control peripheral, LED PWM controller, general DMA controller, TWAI® controller (compatible with ISO 11898-1, i.e. CAN Specification 2.0), USB Serial/JTAG controller, temperature sensor, SAR ADC, general-purpose timers, watchdog timers

> **Note:**
> * Please refer to *ESP32-C3 Series Datasheet* for detailed information about the module peripherals.

Integrated Components on Module

- 40 MHz crystal oscillator
- SPI flash

Antenna Options

- ESP32-C3-WROOM-02: On-board PCB antenna

- ESP32-C3-WROOM-02U: External antenna via a connector

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V

- Operating ambient temperature:

  - 85 °C version module: −40 ~ 85 °C

  - 105 °C version module: −40 ~ 105 °C

Certification

- RF certification: See certificates

- Green certification: RoHS/REACH

Test

- HTOL/HTSL/uHAST/TCT/ESD/Latch-up

1.2   Series Comparison

ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U are two general-purpose Wi-Fi and Bluetooth LE modules. The rich set of peripherals and high performance make the two modules an ideal choice for smart homes, industrial automation, health care, consumer electronics, etc.

ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U both feature an external SPI flash. ESP32-C3-WROOM-02 comes with a on-board PCB antenna. ESP32-C3-WROOM-02U comes with a connector for an external antenna.

A wide selection of module variants are available as shown in Table 1 and 2.

Table 1: ESP32-C3-WROOM-02 (ANT) Series Comparison[1]

Ordering Code	Flash[4, 7]	Ambient Temp.[2] (°C)	Embedded Chip Revision	Size[3] (mm)
ESP32-C3-WROOM-02-N4		−40 ~ 85	v0.4	18.0 × 20.0 × 3.2
ESP32-C3-WROOM-02-H4	4 MB (Quad SPI)	−40 ~ 105	v0.4	

[1] This table shares the same notes presented in Table 2 below.

Table 2: ESP32-C3-WROOM-02U (CONN) Series Comparison

Ordering Code	Flash[4, 7]	Ambient Temp.[2] (°C)	Embedded Chip Revision	Size[3] (mm)
ESP32-C3-WROOM-02U-N4	4 MB (Quad SPI)	−40 ∼ 85	v0.4	
ESP32-C3-WROOM-02U-H4		−40 ∼ 105	v0.4	18.0 × 14.3 × 3.2

[2] Ambient temperature specifies the recommended temperature range of the environment immediately outside the Espressif module.

[3] For details, refer to Section 10.1 *Module Dimensions*.

[4] All modules can be equipped with 8 MB or 16 MB flash. For details, please contact our sales team. The flash supports:
- More than 100,000 program/erase cycles
- More than 20 years data retention time

[5] Customized version operating at −40 ∼ 105 °C is available. For details, please contact our sales team.

[6] All chip revisions have the same SRAM size, but chip revision v1.1 has around 35 KB more available space for users than chip revision v0.4. Chip revision v1.1 depends on specific ESP-IDF versions, as detailed in Compatibility Advisory for ESP32-C3 Chip Revision v1.1. For how to identify chip revisions, please refer to *ESP32-C3 Series SoC Errata*.

[7] By default, the SPI flash on the module operates at a maximum clock frequency of 80 MHz and does not support the auto suspend feature. If you have a requirement for a higher flash clock frequency of 120 MHz or if you need the flash auto suspend feature, please contact us.

Both ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U has two operating ambient temperature options: −40 ∼ 85 °C variants and −40 ∼ 105 °C variants, all embedded with the ESP32-C3 chip.

> **Note:**
>
> For more information on ESP32-C3, please refer to *ESP32-C3 Series Datasheet*.
>
> For chip revision identification, ESP-IDF release that supports a specific chip revision, and other information on chip revisions, please refer to *ESP32-C3 Series SoC Errata* > Section *Chip Revision*.

1.3   Applications

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture

- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

Contents

List of Tables

List of Figures

2   Block Diagram

Figure 1: ESP32-C3-WROOM-02 Block Diagram

Figure 2: ESP32-C3-WROOM-02U Block Diagram

3   Pin Definitions

3.1   Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 10.1 *Module Dimensions*.
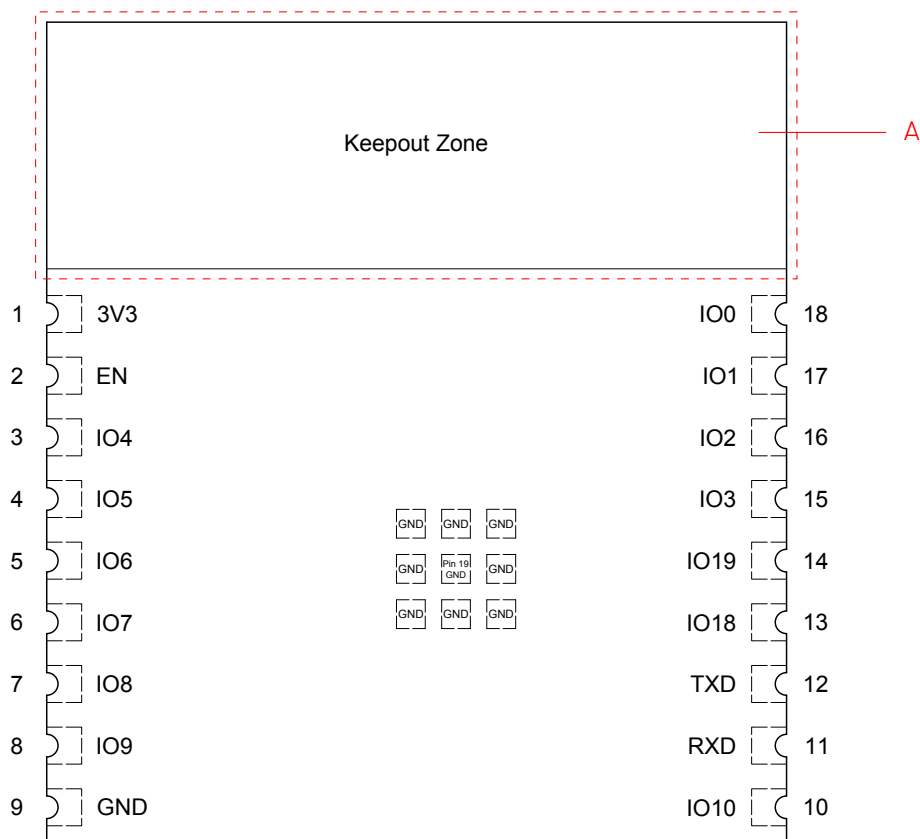
3.2   Pin Description

The module has 19 pins. See pin definitions in Table 3 *Pin Definitions*.

For peripheral pin configurations, please refer to Section 5.2 *Peripheral Description*.

Table 3: Pin Definitions

Name	No.	Type[1]	Function
3V3	1	P	Power supply

Table 3 – cont'd from previous page

Name	No.	Type[1]	Function
EN	2	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	3	I/O/T	GPIO4, ADC1_CH4, FSPIHD, MTMS
IO5	4	I/O/T	GPIO5, ADC2_CH0, FSPIWP, MTDI
IO6	5	I/O/T	GPIO6, FSPICLK, MTCK
IO7	6	I/O/T	GPIO7, FSPID, MTDO
IO8	7	I/O/T	GPIO8
IO9	8	I/O/T	GPIO9
GND	9,19	P	Ground
IO10	10	I/O/T	GPIO10, FSPICS0
RXD	11	I/O/T	GPIO20, U0RXD
TXD	12	I/O/T	GPIO21, U0TXD
IO18	13	I/O/T	GPIO18, USB_D-
IO19	14	I/O/T	GPIO19, USB_D+
IO3	15	I/O/T	GPIO3, ADC1_CH3
IO2	16	I/O/T	GPIO2, ADC1_CH2, FSPIQ
IO1	17	I/O/T	GPIO1, ADC1_CH1, XTAL_32K_N
IO0	18	I/O/T	GPIO0, ADC1_CH0, XTAL_32K_P

[1] P: power supply; I: input; O: output; T: high impedance.

4   Boot Configurations

> **Note:**
> The content below is excerpted from *ESP32-C3 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**

  - Strapping pins: GPIO2, GPIO8, and GPIO9

- **ROM message printing**

  - Strapping pin: GPIO8

  - eFuse parameters: EFUSE_UART_PRINT_CONTROL and EFUSE_USB_PRINT_CHANNEL

The default values of all the above eFuse bits are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once an eFuse bit is programmed to 1, it can never be reverted to 0. For how to program eFuse bits, please refer to *ESP32-C3 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO2	Floating	–
GPIO8	Floating	–
GPIO9	Weak pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-C3 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 5 and Figure 3.

Table 5: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_EN pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_EN is already high and before these pins start operating as regular IO pins.	3
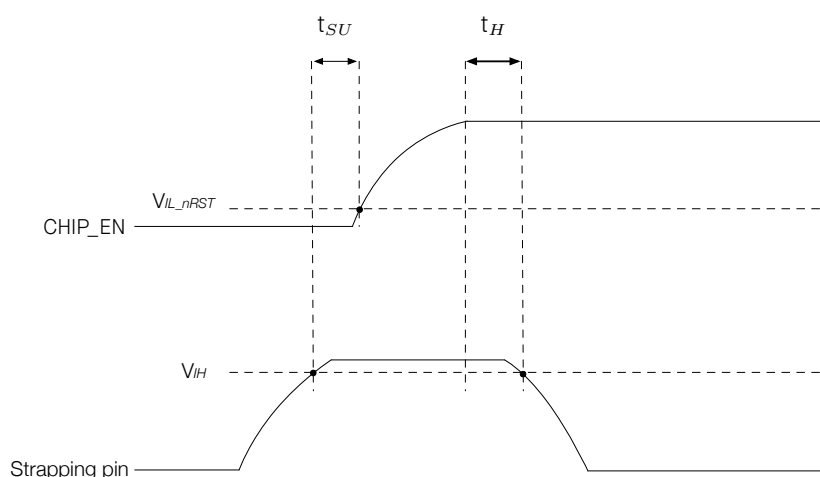
Figure 3: Visualization of Timing Parameters for the Strapping Pins

4.1   Chip Boot Mode Control

GPIO2, GPIO8, and GPIO9 control the boot mode after the reset is released. See Table 6 *Chip Boot Mode Control*.

Table 6: Chip Boot Mode Control

Boot Mode	GPIO2 [2]	GPIO8	GPIO9
SPI Boot	1	Any value	**1**
Joint Download Boot [3]	1	1	0

[1] **Bold** marks the default value and configuration.

[2] GPIO2 actually does not determine SPI Boot and Joint Download Boot mode, but it is recommended to pull this pin up due to glitches.

[3] Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

In addition to SPI Boot and Joint Download Boot modes, ESP32-C3 also supports SPI Download Boot mode. For details, please see *ESP32-C3 Technical Reference Manual* > Chapter *Chip Boot Control*.

4.2   ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- UART0
- USB Serial/JTAG controller

EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table 7 *UART0 ROM Message Printing Control*.

Table 7: UART0 ROM Message Printing Control

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8
Enabled	**0**	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

[1] **Bold** marks the default value and configuration.

EFUSE_USB_PRINT_CHANNEL controls the printing to **USB Serial/JTAG controller** as shown in Table 8 *USB Serial/JTAG ROM Message Printing Control*.

Table 8: USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Code Printing	EFUSE_DIS_USB_SERIAL_JTAG [2]	EFUSE_USB_PRINT_CHANNEL
Enabled	**0**	**0**
Disabled	0	1
	1	Ignored

[1] **Bold** marks the default value and configuration.
[2] EFUSE_DIS_USB_SERIAL_JTAG controls whether to disable USB Serial/JTAG.

5 Peripherals

5.1 Peripheral Overview

ESP32-C3 integrates a rich set of peripherals including SPI, UART, I2C, I2S, remote control peripheral, LED PWM controller, TWAI® controller, USB Serial/JTAG controller, temperature sensor, SAR ADC

To learn more about on-chip components, please refer to *ESP32-C3 Series Datasheet* > Section *Functional Description*.

> **Note:**
>
> The content below is sourced from *ESP32-C3 Series Datasheet* > Section *Peripherals*. Some information may not be applicable to ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U as not all the IO signals are exposed on the module. To learn more about peripheral signals, please refer to *ESP32-C3 Technical Reference Manual* > Section *Peripheral Signal List*.

5.2 Peripheral Description

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

5.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

5.2.1.1 UART Controller

ESP32-C3 has two UART interfaces, i.e. UART0 and UART1, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF). Both UART interfaces connect to GDMA via UHCI0, and can be accessed by the GDMA controller or directly by the CPU.

Pin Assignment

The pins connected to transmit and receive signals (U0TXD and U0RXD) for **UART0** are multiplexed with GPIO21 ~ GPIO20 via IO MUX. Other signals can be routed to any GPIOs via the GPIO matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.2 SPI Controller

ESP32-C3 has the following SPI interfaces:

- **SPI0** used by ESP32-C3's GDMA controller and cache to access in-package or off-package flash

- **SPI1** used by the CPU to access in-package or off-package flash

- **SPI2** is a general purpose SPI controller with access to a DMA channel allocated by the GDMA controller

Features of SPI0 and SPI1

- Supports Single SPI, Dual SPI, and Quad SPI, QPI modes

- Configurable clock frequency with a maximum of 120 MHz in Single Transfer Rate (STR) mode

- Data transmission is in bytes

Features of SPI2

- Supports operation as a master or slave

- Connects to a DMA channel allocated by the GDMA controller

- Supports Single SPI, Dual SPI, and Quad SPI, QPI

- Configurable clock polarity (CPOL) and phase (CPHA)

- Configurable clock frequency

- Data transmission is in bytes

- Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first

- As a master
    - Supports 2-line full-duplex communication with clock frequency up to 80 MHz
    - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 80 MHz
    - Provides six SPI_CS pins for connection with six independent SPI slaves
    - Configurable CS setup time and hold time

- As a slave
    - Supports 2-line full-duplex communication with clock frequency up to 60 MHz
    - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 60 MHz

Pin Assignment

For SPI0/1, the pins are multiplexed with GPIO12 ~ GPIO17 via the IO MUX.

For SPI2, the pins are multiplexed with GPIO2, GPIO4 ~ GPIO7, GPIO10, and JTAG interface via the IO MUX.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.3   I2C Controller

ESP32-C3 has an I2C bus interface which is used for I2C master mode or slave mode, depending on your configuration. The I2C interface supports:

- standard mode (100 Kbit/s)

- fast mode (400 Kbit/s)

- up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)

- 7-bit and 10-bit addressing mode

- double addressing mode

- 7-bit broadcast address

Pin Assignment

The pins for I2C can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.4   I2S Controller

ESP32-C3 includes a standard I2S interface. This interface can operate as a master or a slave in full-duplex mode or half-duplex mode, and can be configured for 8-bit, 16-bit, 24-bit, or 32-bit serial communication. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface connects to the GDMA controller. The interface supports TDM PCM, TDM MSB alignment, TDM standard, and PDM standard.

Pin Assignment

The pins for the I2S Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.5   USB Serial/JTAG Controller

ESP32-C3 integrates a USB Serial/JTAG controller. This controller has the following features:

- CDC-ACM virtual serial port and JTAG adapter functionality

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)

- programming in-package/off-package flash

- CPU debugging with compact JTAG instructions

- a full-speed USB PHY integrated in the chip

Pin Assignment

The pins for the USB Serial/JTAG Controller are multiplexed with GPIO18 ~ GPIO19.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.6   Two-wire Automotive Interface

ESP32-C3 has a TWAI® controller with the following features:

- compatible with ISO 11898-1 protocol (CAN Specification 2.0)

- standard frame format (11-bit ID) and extended frame format (29-bit ID)

- bit rates from 1 Kbit/s to 1 Mbit/s

- multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)

- 64-byte receive FIFO

- acceptance filter (single and dual filter modes)

- error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

Pin Assignment

The pins for the Two-wire Automotive Interface can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.7   LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller:

- Can generate digital waveform with configurable periods and duty cycle. The resolution of duty cycle can be up to 14 bits.

- Has multiple clock sources, including APB clock and external main crystal clock.

- Can operate when the CPU is in Light-sleep mode.

- Supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.1.8   Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channels of infrared remote transmission and two channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All four channels share a 192 × 32-bit memory block to store transmit or receive waveform.

Pin Assignment

The pins for the Remote Control Peripheral can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

5.2.2.1 SAR ADC

ESP32-C3 integrates two 12-bit SAR ADCs.

- ADC1 supports measurements on 5 channels, and is factory-calibrated.
- ADC2 supports measurements on 1 channel, and is not factory-calibrated.

> **Note:**
> ADC2 of some chip revisions is not operable. For details, please refer to ESP32-C3 Series SoC Errata.

Pin Assignment

The pins for the SAR ADC are multiplexed with GPIO0 ~ GPIO5, JTAG interface, SPI2 interface, and pins for external crystal or oscillator.

For more information about the pin assignment, see *ESP32-C3 Series Datasheet* > Section *IO Pins* and *ESP32-C3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

5.2.2.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of −40 °C to 125 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the operating ambient temperature.

6   Electrical Characteristics

6.1   Absolute Maximum Ratings

Stresses above those listed in Table 9 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 10 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T_{STORE}	Storage temperature	−40	105	°C

6.2   Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	Power supply voltage		3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply		0.5	—	—	A
T_A	Operating ambient temperature	85 °C version	−40	—	85	°C
		105 °C version			105	

6.3   DC Characteristics (3.3 V, 25 °C)

Table 11: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	−0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage	−0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

6.4   Current Consumption Characteristics

6.4.1   Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 12: Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @20.5 dBm	345
		802.11g, 54 Mbps, @18 dBm	285
		802.11n, HT20, MCS7, @17.5 dBm	280
		802.11n, HT40, MCS7, @17 dBm	280
	RX	802.11b/g/n, HT20	82
		802.11n, HT40	84

> Note:
> The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-C3 Series Datasheet*.

6.4.2   Current Consumption in Other Modes

Table 13: Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ	
			All Peripherals Clocks Disabled (mA)	All Peripherals Clocks Enabled (mA)[1]
Modem-sleep[2,3]	160	CPU is idle	16	21
		CPU is running	23	28
	80	CPU is idle	13	18
		CPU is running	17	22

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 14: Current Consumption in Low-Power Modes

Mode	Description	Typ (μA)
Light-sleep	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance	130
Deep-sleep	RTC timer + RTC memory	5
Power off	CHIP_EN is set to low level, the chip is powered off	1

7   RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The external antennas used for the tests on the modules with external antenna connectors have an impedance of 50 Ω.Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 ℃ ambient temperature.

7.1   Wi-Fi Radio

Table 15: Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n

7.1.1   Wi-Fi RF Transmitter (TX) Characteristics

Table 16: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	20.5	—
802.11b, 11 Mbps	—	20.5	—
802.11g, 6 Mbps	—	20.0	—
802.11g, 54 Mbps	—	18.0	—
802.11n, HT20, MCS0	—	19.0	—
802.11n, HT20, MCS7	—	17.5	—
802.11n, HT40, MCS0	—	18.5	—
802.11n, HT40, MCS7	—	17.0	—

Table 17: TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, @20.5 dBm	—	−24.5	−10
802.11b, 11 Mbps, @20.5 dBm	—	−25.0	−10
802.11g, 6 Mbps, @20 dBm	—	−23.0	−5
802.11g, 54 Mbps, @18 dBm	—	−28.0	−25
802.11n, HT20, MCS0, @19 dBm	—	−23.5	−5

Cont'd on next page

Table 17 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11n, HT20, MCS7, @17.5 dBm	—	−29.5	−27
802.11n, HT40, MCS0, @18.5 dBm	—	−26.5	−5
802.11n, HT40, MCS7, @17 dBm	—	−29.5	−27

[1] EVM is measured at the corresponding typical TX power provided in Table 16 *TX Power with Spectral Mask and EVM Meeting 802.11 Standards* above.

7.1.2   Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n/ax.

Table 18: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	−98.0	—
802.11b, 2 Mbps	—	−96.0	—
802.11b, 5.5 Mbps	—	−93.0	—
802.11b, 11 Mbps	—	−88.6	—
802.11g, 6 Mbps	—	−93.0	—
802.11g, 9 Mbps	—	−92.0	—
802.11g, 12 Mbps	—	−90.8	—
802.11g, 18 Mbps	—	−88.4	—
802.11g, 24 Mbps	—	−85.4	—
802.11g, 36 Mbps	—	−82.0	—
802.11g, 48 Mbps	—	−78.0	—
802.11g, 54 Mbps	—	−76.4	—
802.11n, HT20, MCS0	—	−93.0	—
802.11n, HT20, MCS1	—	−90.8	—
802.11n, HT20, MCS2	—	−88.2	—
802.11n, HT20, MCS3	—	−84.6	—
802.11n, HT20, MCS4	—	−81.4	—
802.11n, HT20, MCS5	—	−77.4	—
802.11n, HT20, MCS6	—	−75.4	—
802.11n, HT20, MCS7	—	−74.4	—
802.11n, HT40, MCS0	—	−90.0	—
802.11n, HT40, MCS1	—	−87.6	—
802.11n, HT40, MCS2	—	−84.8	—
802.11n, HT40, MCS3	—	−81.8	—
802.11n, HT40, MCS4	—	−78.4	—
802.11n, HT40, MCS5	—	−74.4	—
802.11n, HT40, MCS6	—	−72.6	—

Cont'd on next page

Table 18 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS7	—	−71.2	—

Table 19: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 20: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	16	—
802.11n, HT40, MCS0	—	25	—
802.11n, HT40, MCS7	—	11	—

7.2   Bluetooth 5 (LE) Radio

Table 21: Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	−24.0 ~ 20.0 dBm

7.2.1   Bluetooth LE RF Transmitter (TX) Characteristics

Table 22: Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
In-band emissions	F = F0 ± 2 MHz	—	−37.62	—	dBm
	F = F0 ± 3 MHz	—	−41.95	—	dBm
	F = F0 ± > 3 MHz	—	−44.48	—	dBm
Modulation characteristics	$\Delta f1_{avg}$	—	245.00	—	kHz
	$\Delta f2_{max}$	—	208.00	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	0.93	—	—
Carrier frequency offset	—	—	−9.00	—	kHz
Carrier frequency drift	$|f_0 - f_n|_{n=2, 3, 4, ..k}$	—	1.17	—	kHz
	$|f_1 - f_0|$	—	0.30	—	kHz
	$|f_n - f_{n-5}|_{n=6, 7, 8, ..k}$	—	4.90	—	kHz

Table 23: Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
In-band emissions	F = F0 ± 4 MHz	—	−43.55	—	dBm
	F = F0 ± 5 MHz	—	−45.26	—	dBm
	F = F0 ± > 5 MHz	—	−47.00	—	dBm
Modulation characteristics	$\Delta f1_{avg}$	—	497.00	—	kHz
	$\Delta f2_{max}$	—	398.00	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	0.95	—	—
Carrier frequency offset	—	—	−9.00	—	kHz
Carrier frequency drift	$|f_0 - f_n|_{n=2, 3, 4, ..k}$	—	0.46	—	kHz
	$|f_1 - f_0|$	—	0.70	—	kHz
	$|f_n - f_{n-5}|_{n=6, 7, 8, ..k}$	—	6.80	—	kHz

Table 24: Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
In-band emissions	F = F0 ± 2 MHz	—	−37.90	—	dBm
	F = F0 ± 3 MHz	—	−41.00	—	dBm
	F = F0 ± > 3 MHz	—	−42.50	—	dBm
Modulation characteristics	$\Delta f1_{avg}$	—	252.00	—	kHz
	$\Delta f1_{max}$	—	200.00	—	kHz
Carrier frequency offset	—	—	−13.70	—	kHz
Carrier frequency drift	$|f_0 - f_n|_{n=1, 2, 3, ..k}$	—	1.52	—	kHz
	$|f_0 - f_3|$	—	0.65	—	kHz
	$|f_n - f_{n-3}|_{n=7, 8, 9, ..k}$	—	0.70	—	kHz

Table 25: Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
In-band emissions	F = F0 ± 2 MHz	—	−37.90	—	dBm
	F = F0 ± 3 MHz	—	−41.30	—	dBm
	F = F0 ± > 3 MHz	—	−42.80	—	dBm
Modulation characteristics	$\Delta f2_{avg}$	—	220.00	—	kHz
	$\Delta f2_{max}$	—	205.00	—	kHz
Carrier frequency offset	—	—	−11.90	—	kHz
Carrier frequency drift	$\|f_0 - f_n\|_{n=1, 2, 3, ..k}$	—	1.37	—	kHz
	$\|f_0 - f_3\|$	—	1.09	—	kHz
	$\|f_n - f_{n-3}\|_{n=7, 8, 9, ..k}$	—	0.51	—	kHz

7.2.2   Bluetooth LE RF Receiver (RX) Characteristics

Table 26: Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−97	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	7	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	−4	—	dB
	F = F0 − 1 MHz	—	−4	—	dB
	F = F0 + 2 MHz	—	−29	—	dB
	F = F0 − 2 MHz	—	−31	—	dB
	F ≥ F0 + 3 MHz	—	−33	—	dB
	F ≤ F0 − 3 MHz	—	−35	—	dB
	F ≥ F0 + 4 MHz	—	−35	—	dB
	F ≤ F0 − 4 MHz	—	−37	—	dB
Image frequency	—	—	−35	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	−40	—	dB
	F = F_{image} − 1 MHz	—	−33	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	−6	—	dBm
	2003 MHz ~ 2399 MHz	—	−26	—	dBm
	2484 MHz ~ 2997 MHz	—	−25	—	dBm
	3000 MHz ~ 12.75 GHz	—	−5	—	dBm
Intermodulation	—	—	−30	—	dBm

Table 27: Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−93	—	dBm
Maximum received signal @30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	10	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	−8	—	dB
	F = F0 − 2 MHz	—	−7	—	dB
	F = F0 + 4 MHz	—	−32	—	dB
	F = F0 − 4 MHz	—	−34	—	dB
	F ≥ F0 + 6 MHz	—	−39	—	dB
	F ≤ F0 − 6 MHz	—	−39	—	dB
Image frequency	—	—	−32	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	−39	—	dB
	F = F_{image} − 2 MHz[2]	—	−8	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	−12	—	dBm
	2003 MHz ~ 2399 MHz	—	−30	—	dBm
	2484 MHz ~ 2997 MHz	—	−28	—	dBm
	3000 MHz ~ 12.75 GHz	—	−6	—	dBm
Intermodulation	—	—	−29	—	dBm

Table 28: Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−105	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	2	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	−6	—	dB
	F = F0 − 1 MHz	—	−4	—	dB
	F = F0 + 2 MHz	—	−33	—	dB
	F = F0 − 2 MHz	—	−41	—	dB
	F ≥ F0 + 3 MHz	—	−37	—	dB
	F ≤ F0 − 3 MHz	—	−46	—	dB
	F ≥ F0 + 4 MHz	—	−40	—	dB
	F ≤ F0 − 4 MHz	—	−49	—	dB
Image frequency	—	—	−40	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	−46	—	dB
	F = F_{image} − 1 MHz	—	−37	—	dB

Table 29: Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	−101	—	dBm
Maximum received signal @30.8% PER	—	—	10	—	dBm
Co-channel C/I	—	—	3	—	dB

Table 29 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	−6	—	dB
	F = F0 − 1 MHz	—	−7	—	dB
	F = F0 + 2 MHz	—	−34	—	dB
	F = F0 − 2 MHz	—	−37	—	dB
	F ≥ F0 + 3 MHz	—	−38	—	dB
	F ≤ F0 − 3 MHz	—	−40	—	dB
	F ≥ F0 + 4 MHz	—	−40	—	dB
	F ≤ F0 − 4 MHz	—	−42	—	dB
Image frequency	—	—	−40	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	−45	—	dB
	F = F_{image} − 1 MHz	—	−38	—	dB

8   Module Schematics

This is the reference design of the module.
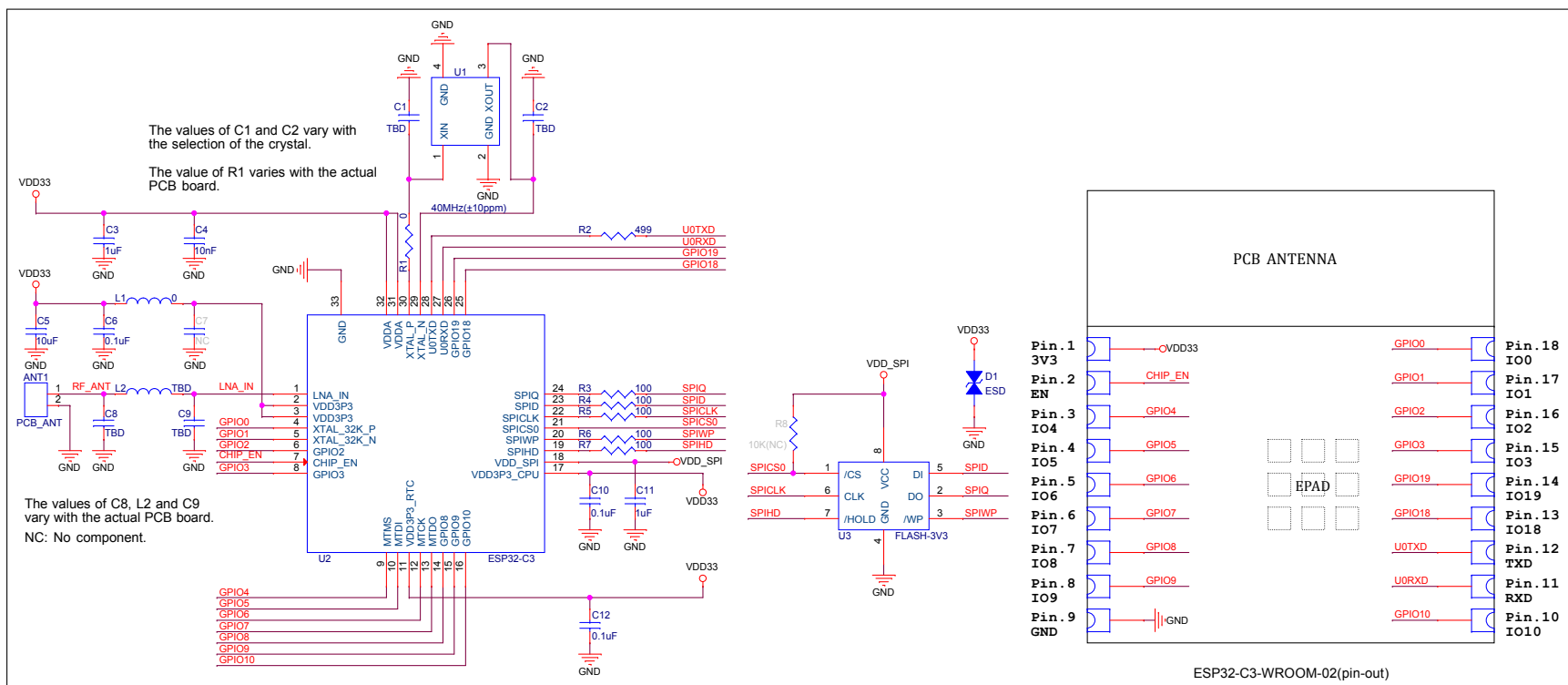
Figure 4: ESP32-C3-WROOM-02 Schematics
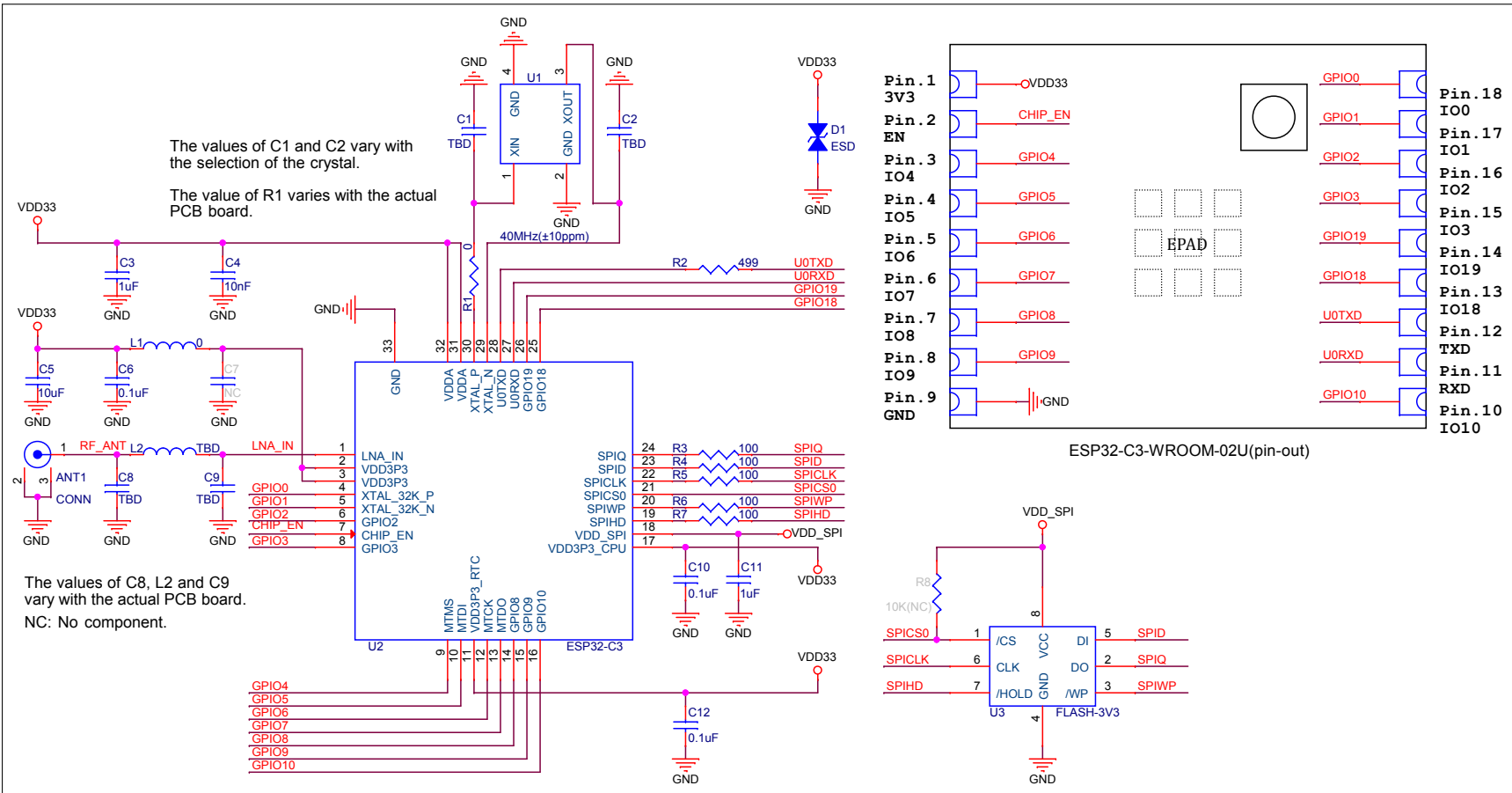
Figure 5: ESP32-C3-WROOM-02U Schematics

9 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

Figure 6: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.

- To ensure that the power supply to the ESP32-C3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-C3's power-up and reset sequence timing diagram, please refer to *ESP32-C3 Series Datasheet* > Section *Power Supply*.

# 10   Physical Dimensions

10.1   Module Dimensions
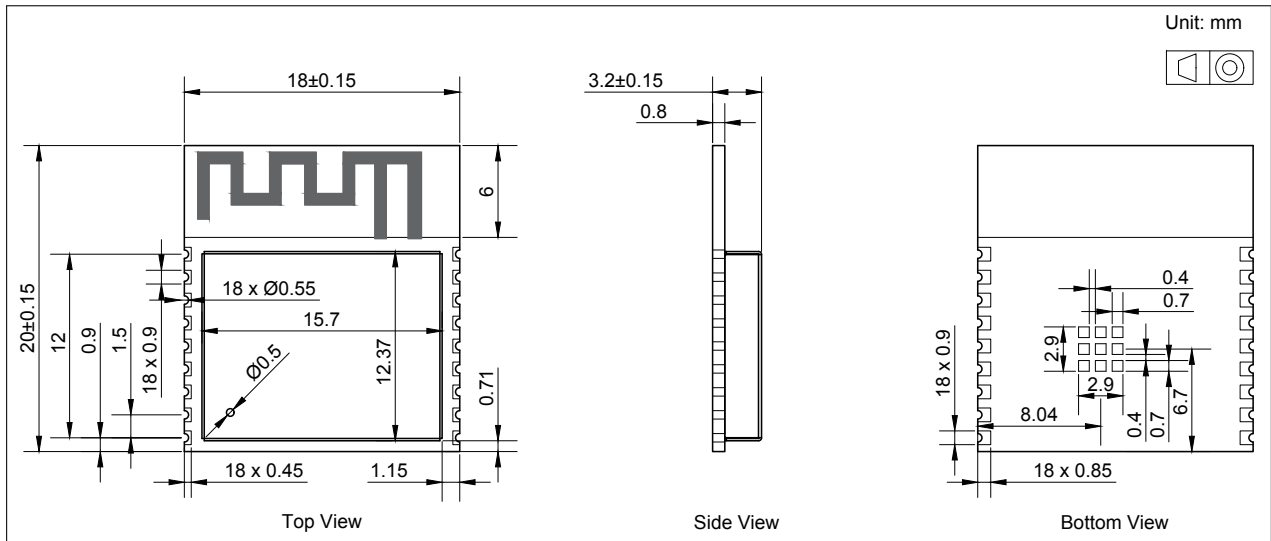
Figure 7: ESP32-C3-WROOM-02 Physical Dimensions
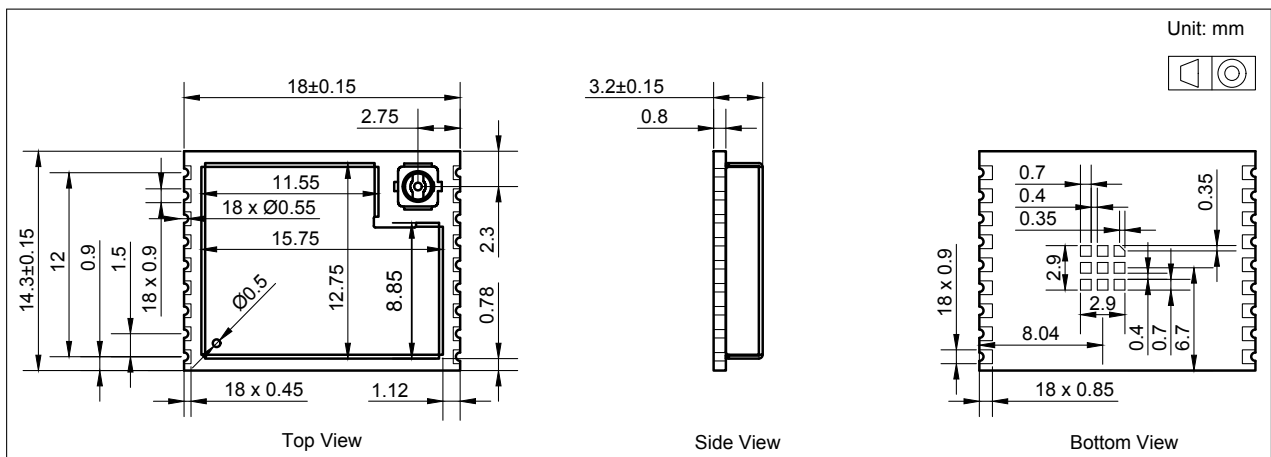
Figure 8: ESP32-C3-WROOM-02U Physical Dimensions

> **Note:**
>
> For information about tape, reel, and product marking, please refer to *Espressif Module Packaging Information*.

10.2   Dimensions of External Antenna Connector

ESP32-C3-WROOM-02U uses the first generation external antenna connector as shown in Figure 9 *Dimensions of External Antenna Connector*. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose

- MHF I connector from I-PEX

- AMC connector from Amphenol
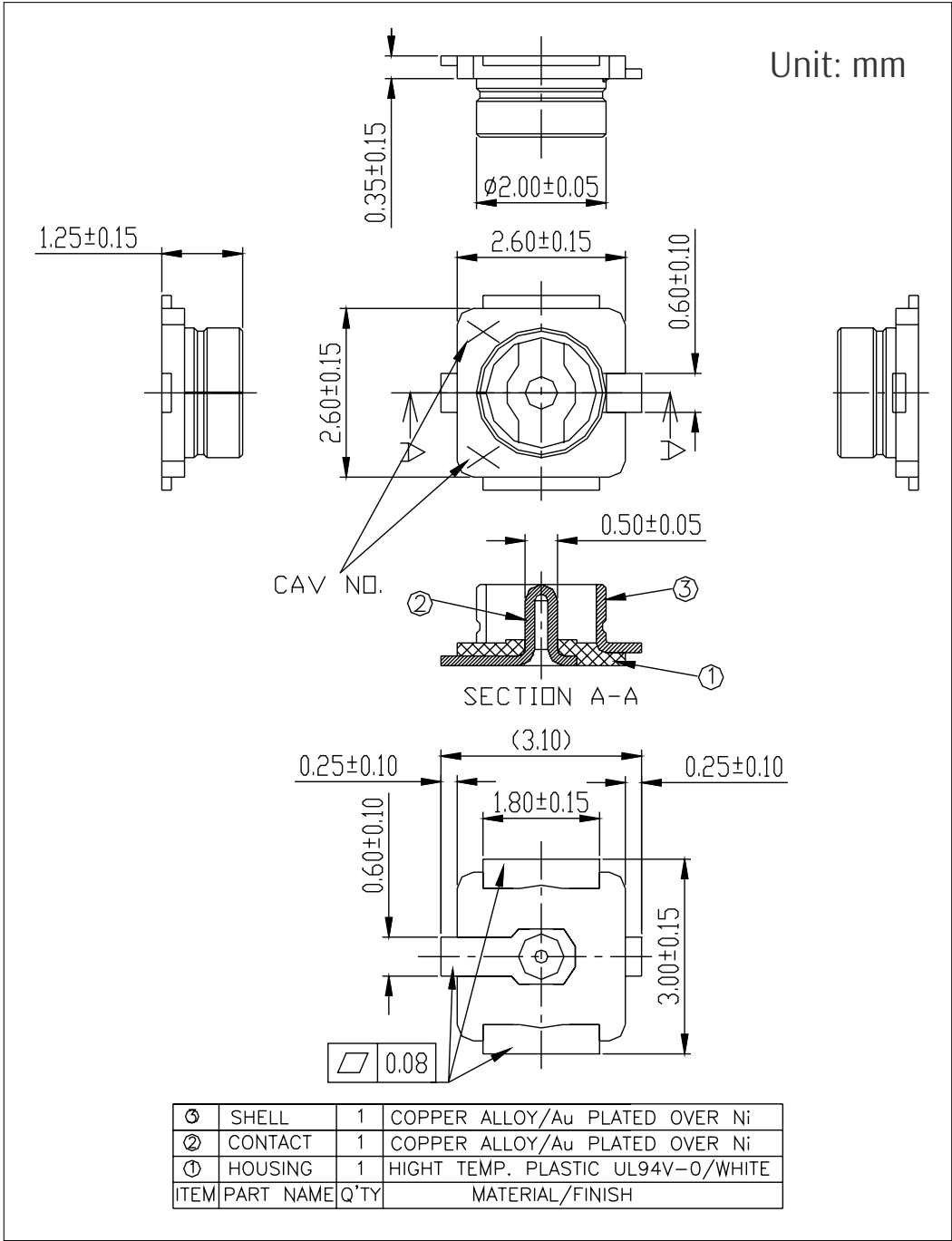
Figure 9: Dimensions of External Antenna Connector

11 PCB Layout Recommendations

11.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 10 *ESP32-C3-WROOM-02 Recommended PCB Land Pattern* and Figure 11 *ESP32-C3-WROOM-02U Recommended PCB Land Pattern*.

- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 10 and Figure 11. You can view the source files for ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U with Autodesk Viewer.

- 3D models of ESP32-C3-WROOM-02 and ESP32-C3-WROOM-02U. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).
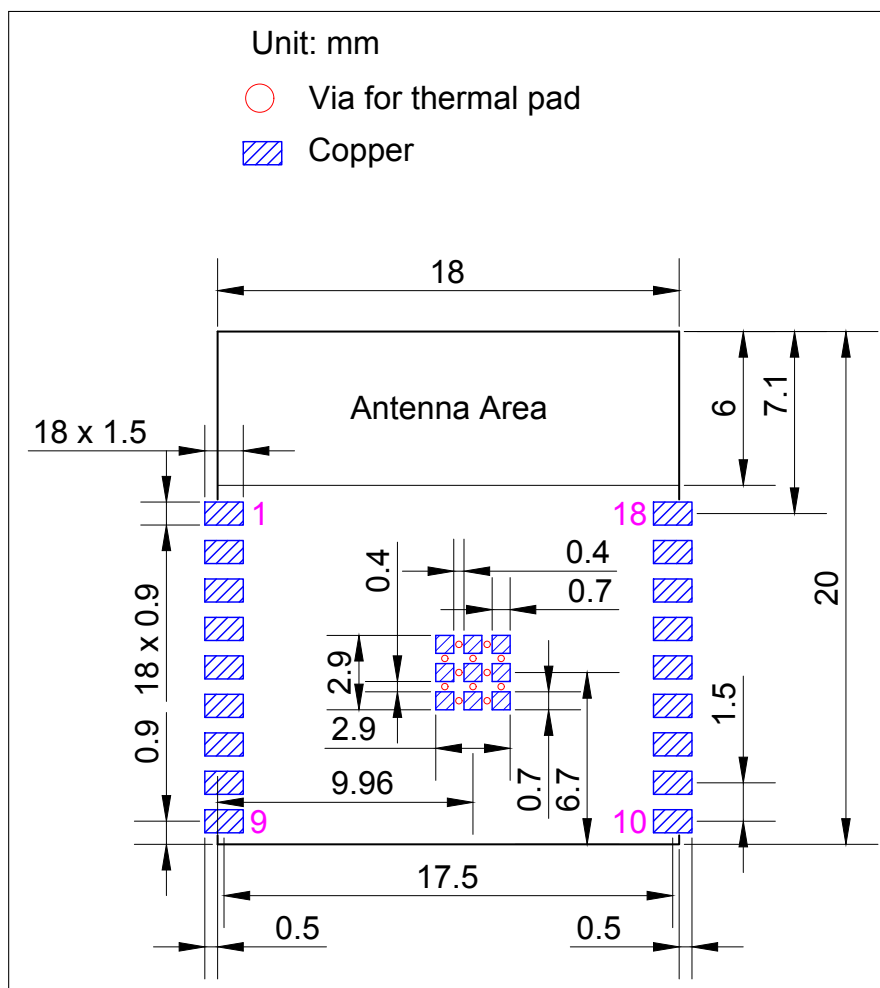
Figure 10: ESP32-C3-WROOM-02 Recommended PCB Land Pattern
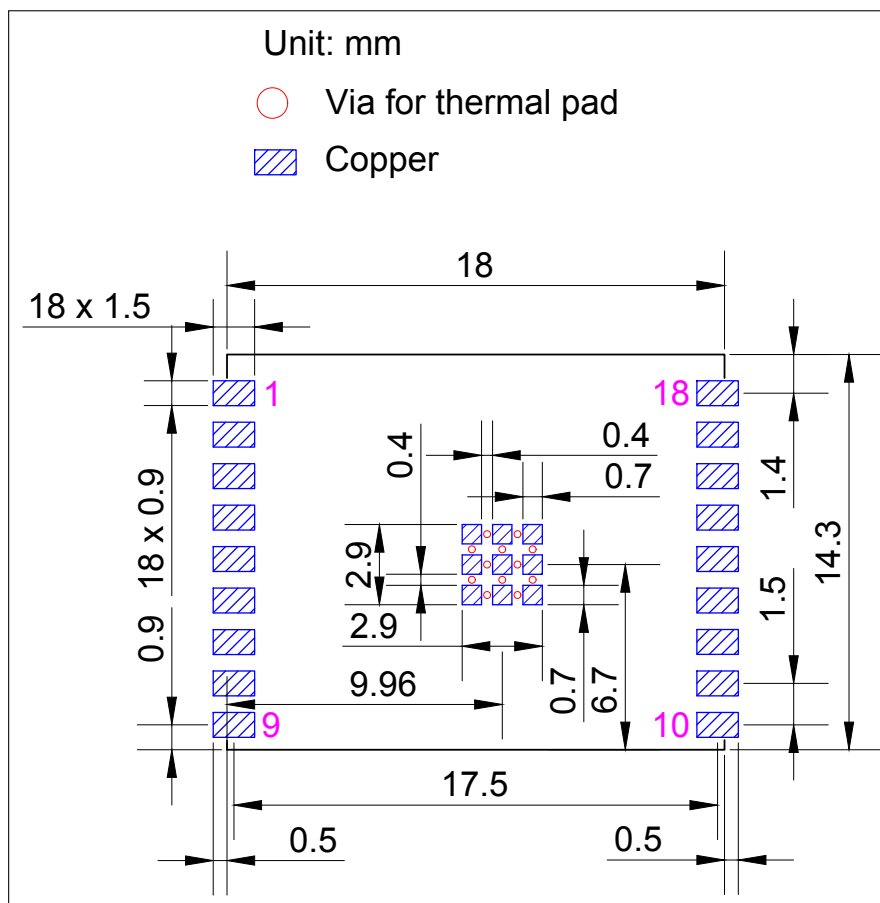
Figure 11: ESP32-C3-WROOM-02U Recommended PCB Land Pattern

11.2 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

For details about module placement for PCB design, please refer to *ESP32-C3 Hardware Design Guidelines* > Section *Positioning a Module on a Base Board*.

12   Product Handling

12.1   Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

12.2   Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

## 12.3   Reflow Profile

Solder the module in a single reflow.
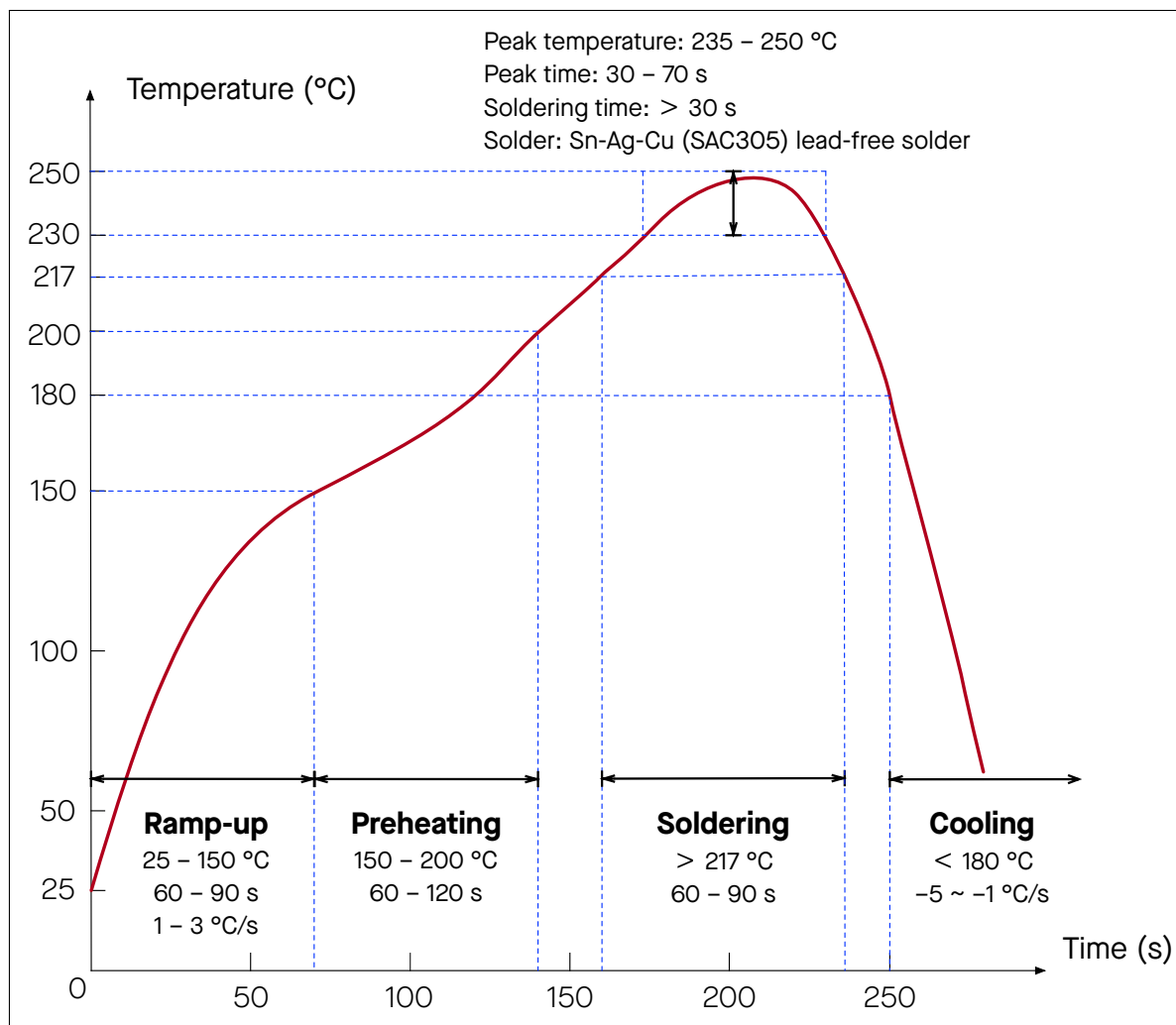
Figure 12: Reflow Profile

12.4   Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

Related Documentation and Resources

Related Documentation

- [ESP32-C3 Series Datasheet](#) – Specifications of the ESP32-C3 hardware.
- [ESP32-C3 Technical Reference Manual](#) – Detailed information on how to use the ESP32-C3 memory and peripherals.
- [ESP32-C3 Hardware Design Guidelines](#) – Guidelines on how to integrate the ESP32-C3 into your hardware product.
- [ESP32-C3 Series SoC Errata](#) – Descriptions of known errors in ESP32-C3 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-C3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C3
- *ESP32-C3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-C3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- [ESP-IDF Programming Guide for ESP32-C3](#) – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C3 Series SoCs* – Browse through all ESP32-C3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C3
- *ESP32-C3 Series Modules* – Browse through all ESP32-C3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-C3
- *ESP32-C3 Series DevKits* – Browse through all ESP32-C3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-C3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release notes
2024-09-19	v1.4	• Deleted the ESP32-C3-WROOM-02-N8 and ESP32-C3-WROOM-02U-N8 variants, updated notes about customizing modules with 8 MB or 16 MB flash, and updated flash program/erase cycles, data retention time (note 4) and maximum clock frequency (note 7) in Table *ESP32-C3-WROOM-02 (ANT) Series Comparison*[1] and Table *ESP32-C3-WROOM-02U (CONN) Series Comparison* • Improved the wording and structure of following sections: – Updated Section "Strapping Pins" and renamed to *4 Boot Configurations* – Added Chapter *5 Peripherals* – Updated Table "Wi-Fi RF Standards" and renamed to "Wi-Fi RF Characteristics" – Added Section *11.2 Module Placement for PCB Design* – Optimized Figure *12 Reflow Profile*
2023-02-01	v1.3	• Added module variants ESP32-C3-WROOM-02-N8 and ESP32-C3-WROOM-02U-N8 • Updated the maximum value of "RF power control range" to 20 dBm in Table *Bluetooth LE RF Characteristics*
2022-11-08	v1.2	• Changed Table *Ordering Information* to Table *ESP32-C3-WROOM-02 (ANT) Series Comparison*[1] and Table *ESP32-C3-WROOM-02U (CONN) Series Comparison* • Updated test condition descriptions and data in Section *6.4 Current Consumption Characteristics* • Updated "RF power control range" in Table *Bluetooth LE RF Characteristics* • Added descriptions in Section *11.1 PCB Land Pattern*
2022-06-13	v1.1	Updated Table *Ordering Information*

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Date	Version	Release notes
2021-08-20	v1.0	- Updated module description on the title page - Deleted Section "About This Document" - Restructured Section 1.1 *Features* - Updated Table 17 *TX EVM Test*[1] - Updated Table 20 *RX Adjacent Channel Rejection* - Updated Chapter 8 *Module Schematics* - Updated ESP32-C3-WROOM-02U *Module Dimensions* - Added descriptions in Section 10.2 *Dimensions of External Antenna Connector* - Updated Section "Learning Resources" and renamed to Related Documentation and Resources - Replaced "chip family" with "chip series" following Espressif's taxonomy
2021-05-17	v0.7	- Updated Section 4 *Boot Configurations* - Updated ESP32-C3-WROOM-02U *Module Dimensions*
2021-04-16	v0.6	Added information about ESP32-C3-WROOM-02U module
2021-03-05	v0.5	Preliminary release

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