R3CAP: Short Range Motion Capture of RFID Tags
Final Project - ECE-395-A

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Abstract

1 Introduction

a. RFID tag localization in industry

b. RFID tag localization in literature

c. Limitations of current literature (2D, AOA only, single tag, RSSI is really not good)

d. State the goal: 3D, localization, no use of RSSI, multi-tag

2 Related Works

2.1 RFID Tracking

2.2 FPGA Beamforming

3 RFID Protocol

4 Proposed Solution

a. Use two antenna arrays to receive phase data at two locations

b. Perform MUSIC algorithm to find angle of arrival from each array, and triangulate positions from these angles

c. Triangulation requires association of RFID transmitters with their respective ID numbers, so simultaneously we must implement the RFID reading protocol

4.1 RF Frontend

a. Two three-by-three square antenna arrays, using chip or patch antennas, as they have fixed positions and are small

b. Receiver chain: low noise amplifiers (LNAs), bandpass filters (BPFs), automatic gain controller (AGC) and serial analog-to-digital converters (ADCs) for each antenna

c. Transmitter chain: digital-to-analog converter (DAC), upconverter consisting of a local oscillator (LO) and mixer, power amplifier (PA), BPF and antenna

d. Auxiliary receiver chain: steals the signal from the output of the transmitter chain to be fed back into FPGA for interference cancellation; power splitter, AGC and ADC

4.2 FPGA Implementation

a. Timing protocol for serial ADC data retrieval

b. Digital downconversion (DDC) and quadrature demodulation, implemented as in paper from related works

c. Antialiasing filters on I and Q data

d. Creation of autocorrelation matrices and implementation of MUSIC algorithm

e. UART serial communication of tag coordinates to host computer

f. Interference cancellation through channel estimation using auxiliary receiver chain for each received signal

g. Implementation of RFID protocol

4.3 Host Computer

a. Graphically display locations of RFID tags in real time

5 Current Progress

5.1 MATLAB Simulations

a. MUSIC algorithm simulations

b. Digital IQ demodulation simulations

5.2 FPGA Designs

a. IQ demodulation and DDC at gate level block diagram and simulations

b. Antialiasing filters optimized for FPGA space, with simulations

c. FPGA receiver processing on pre-synthesized data from front-to-back

5.3 Prototype RF Frontend

a. Full PCB layout for single-antenna-array receiver chain

b. Full schematic for RF frontend, potentially PCB layouts depending on testing results

6 Work for Spring Semester

6.1 RF Frontend

a. Transmitter PCB layout

b. Experimentation with receivers and transmitters to see what is viable before upscaling

c. Upscaling to two three-by-three antenna arrays

6.2 FPGA Designs

a. RFID read and interrogate protocol

b. Interference cancellation

c. Further optimize speed of MUSIC implementation

6.3 Host Computer

a. Using Unity or another similar 3D visualization software, create an interface which uses the UART data from the FPGA to draw the tags at their computed positions in space