ECE 150 Digital Logic Design, Fall 2024

Final Exam, December 4th 2024 Name: ____________________

The exam has 100 pts. Closed book, no calculators. Write all answers and show all work inside your blue book. Show your work for partial/full credit. ***Read carefully.***

Problem 1 (16 pts).
Using several of the 1024x4 RAM chip shown in Figure 1 and any additional combinatorial circuitry (muxes, gates, etc.), implement an equivalent 4096x8 RAM chip. Carefully label your equivalent circuit's write-enable (not), chip-select (not), input/output, and address pins. Indicate MSB and LSB on your address pins.

Problem 2 (4 pts).
Give the truth-table of a tri-state buffer. Describe how tri-state buffers are used internally in RAM chips (such as the chip in Problem 1).

Problem 3 (15pts).
Consider the Mod-N counter in Fig. 2. Assume the circuit starts in the $Q_1Q_0 = 00$ state.

(a) Is this circuit synchronous or asynchronous? Why?

(b) Draw a timing diagram to determine the states of the counter. Include glitch-states from propagation delay (if they exist).

(c) Denote the FF states below your timing diagram in decimal, interpreting Q_1 as the MSB and Q_0 as the LSB.

(d) What Mod is the counter?

Problem 4 (15pts).
A bidirectional shift-register (BSR) is one in which bits are shifted from left to right ($R = 1$) or right to left ($R = 0$) on the edge of a clock pulse, depending on input R.

(a) Design a 4-bit BSR with edge-triggered D flip-flops. Your BSR should have a left Data-input D_L, right Data-input D_R, a direction pin R, and parallel ouput pins $Q_0Q_1Q_2Q_3$. You may use gates and muxes/demuxes in your design.

(b) Briefly describe how you can augment your design to allow for parallel *loading* of data into the register.

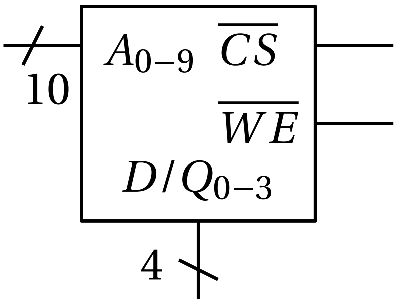

Figure 1: RAM chip.

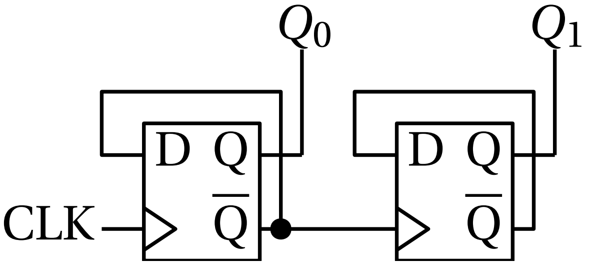

Figure 2: Counter circuit.

Problem 5 (20 pts).
In this problem, you will build a synchronous Mod-4 binary up counter which is *both* "pause-able" and "resetable", i.e. it *pauses counting* when an input signal $\overline{P}$ is low, and *resets to zero* when input signal $\overline{R}$ is low. Otherwise, it continues counting up (with wrap-around). Note that reset should take precedent over pause.

(a) Construct a state transition diagram for your counter.

(b) Convert your state transition digram to a table, labeling current states, inputs, control variables, and next states. Determine values for your control variables to achieve the desired transitions.

(c) Determine simplified boolean expressions for your control variables.

(d) Draw a logic diagram of your circuit. Label the clock, $\overline{P}$, $\overline{R}$, and your state variables clearly.

Problem 6 (10 pts).
Consider the "pause-able"+"resetable" Mod-4 synchronous circuit constructed in Problem 5.

(a) Using a single counter from Problem 5, implement a "chain-able"+resetable Mod-4 up-counter, such that the chain-in ($\mathrm{C_{in}}$) pin of a more significant chainable counter could be connected to the chain-out pin ($\mathrm{C_{out}}$) of a less significant chainable counter.

(b) Implement a Mod-16 synchronous up-counter using your "chain-able"+resetable Mod-4 up-counter(s).

Problem 7 (10 pts).
Consider the "pause-able"+"resetable" Mod-4 synchronous circuit constructed in Problem 5.

(a) Using a single counter from Problem 5, implement a "pause-able"+"programmable" Mod-4 up-counter, such that given an input 2-bit number $B = B_1B_0$, the counter only reaches a maximum value of B before wrapping around.

Problem 8 (10 pts).
Consider the "pause-able"+"resetable" Mod-4 synchronous circuit constructed in Problem 5.

(a) Using a single counter from Problem 5, implement a "chain-able"+"programmable" Mod-4 up-counter (see Problems 7 and 8 for descriptions).

(b) Implement a programmable Mod-16 synchronous up-counter using your "chain-able" + "programmable" Mod-4 up-counter(s), which takes as input a binary number $B = B_3B_2B_1B_0$.