

NILADRISH CHATTERJEE

Computer Architect

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RESEARCH OVERVIEW

My research in computer architecture focuses on advancing the state-of-the-art in memory technology for high-performance platforms and emerging workloads. Improvements in energy-efficiency of DRAM-based main memory systems is imperative for the performance scaling of future systems and my research address this issue through innovations in DRAM microarchitectures, memory controller architectures, and system-level data organization.

PUBLICATIONS

DRAM Microarchitecture

- **MICRO-2017** Fine-Grained DRAM: Energy-Efficient DRAM for Extreme Bandwidth Systems. M. O'Connor, N. Chatterjee, D. Lee, J. Wilson, A. Agrawal, S. W. Keckler, and W. J. Dally.
- **HPCA-2017** Architecting an Energy-Efficient Memory System for GPUs. N. Chatterjee, M. O'Connor, D. Lee, D. R. Johnson, M. Rhu, S. W. Keckler, and W. J. Dally.
- **MEMSYS-2016** CLARA: Circular Linked-List Refresh Architecture. A. Agrawal, M. O'Connor, E. Bolotin, N. Chatterjee, J. Emer, and S. W. Keckler.
- **HPCA-2012** Staged-Reads: Mitigating the Impact of DRAM Writes on DRAM Reads. N. Chatterjee, R. Balasubramonian, N. Muralimanohar, A. Davis, and N. Jouppi.
- **ISCA-2010** Rethinking DRAM Design and Organization for Energy-Constrained Multi-cores. A. Udiipi, N. Muralimanohar, N. Chatterjee, R. Balasubramonian, A. Davis, and N. Jouppi.

Memory Controller & DRAM System Architecture

- **ISPASS-2016** Addressing Service Interruptions in Memory with Thread-to-Rank Assignment. M. Shevgoor, R. Balasubramonian, N. Chatterjee, and J. Kim.
- **MEMSYS-2015** Anatomy of GPU Memory System For Multi-Application Execution. A. Jog, O. Kayiran, E. Bolotin, T. Kesten, A. Pattanayak, N. Chatterjee, S. W. Keckler, M. T. Kandemir, and C. R. Das.
- **SC-2014** Managing DRAM Latency Divergence in Irregular GPGPU Applications. N. Chatterjee, M. O'Connor, G. H. Loh, N. Jayasena, and R. Balasubramonian.
- **MICRO-2013** Quantifying the Relationship between the Power Delivery Network and Architectural Policies in 3D-Stacked Memory Devices. M. Shevgoor, J.-S. Kim, N. Chatterjee, R. Balasubramonian, A. Davis, and A. N. Udiipi.
- **UUCS-TR-12-002** USIMM: the Utah Simulated Memory Module. A Simulation Infrastructure for the JWAC Memory Scheduling Competition. N. Chatterjee, R. Balasubramonian, M. Shevgoor, S. H. Pugsley, A. N. Udiipi, A. Shaifei, M. Awasthi, K. Sudan, and Z. Chishti
- **MICRO-2012** Leveraging Heterogeneity in DRAM Main Memories to Accelerate Critical Word Access. N. Chatterjee, M. Shevgoor, R. Balasubramonian, A. Davis, Z. Fang, R. Illikkal, and R. Iyer.
- **ASPLOS-2010** Micro-pages: Increasing DRAM Efficiency with Locality-Aware Data Placement. K. Sudan, N. Chatterjee, M. Awasthi, D. Nellans, R. Balasubramonian, and A. Davis.

EDUCATION

Ph.D. in Computer Engineering

University of Utah

2008 – 2013

Thesis title: Designing Efficient Memory Schedulers For Future Systems

Advisor: Dr. Rajeev Balasubramonian

B.E. in Computer Science

Jadavpur University

2003 – 2007

EXPERIENCE

NVIDIA

Sr. Research Scientist

2013 – Ongoing Redmond, WA

- Researching fundamental advances to HPC and AI platforms with emphasis on memory system performance and energy-efficiency.

HP Labs

Intern

Fall 2012 SLC, UT

- Enhancing disaggregated memory systems for datacenters.

AMD Research

Intern

Spring 2012 Sunnyvale, CA

- Memory scheduler enhancement to provide latency guarantees while serving high bandwidth clients.

PATENTS

9,910,605 Page migration in a hybrid memory device

9,846,550 Memory access methods and apparatus (divisional of 9,361,955)

9,535,831 Page migration in a 3D stacked hybrid memory

9,489,321 Scheduling memory accesses using an efficient row burst value

9,361,955 Memory Access Methods and Apparatus

Near-Memory Data Processing

- **SC-2017** Toward Standardized Near-Data Processing with Unrestricted Data Placement for GPUs. G. Kim, N. Chatterjee, M. O'Connor, and K. Hsieh.
- **ISCA-2016** Transparent Offloading and Mapping (TOM): Enabling Programmer-Transparent Near-Data Processing in GPU Systems. K. Hsieh, E. Ebrahimi, G. Kim, N. Chatterjee, M. O'Connor, N. Vijaykumar, O. Mutlu, and S. W. Keckler.

Data Transfer Acceleration

- **HPCA-2018** Reducing Data Transfer Energy by Exploiting Similarity within a Data Transaction. D. Lee, M. O'Connor, and N. Chatterjee.
- **HPCA-2018** Compressing DMA Engine: Leveraging Activation Sparsity for Training Deep Neural Networks. M. Rhu, M. O'Connor, N. Chatterjee, J. Pool, Y. Kwon, and S. W. Keckler.

DRAM System Measurements

- **SIGMETRICS-2018** What Your DRAM Power Models are Not Telling You: Lessons from a Detailed Experimental Study . S. Ghose, A. G. Yaglicki, R. Gupta, D. Lee, K. Kudrolli, W. X. Liu, H. Hassan, K. K. Chang, N. Chatterjee, A. Agrawal, M. O'Connor, and O. Mutlu .
- **SIGMETRICS-2017** Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms. K. K. Chang, A. G. Yaglicki, S. Ghose, A. Agrawal, N. Chatterjee, A. Kashyap, D. Lee, M. O'Connor, H. Hassan, and O. Mutlu.

HONORS



Best Paper Award
ISPASS 2016



Best Paper Nominee
HPCA 2018



Best Poster Awards
HiPC 2009. School of Computing
Graduate Research Competition 2010
and 2013



School of Computing Fellowship
University of Utah teaching fellowship
2008. Awarded to outstanding incoming
graduate students.



Media Coverage
HPCA 2017 work on GPU DRAM microarchitecture covered on The
Next Platform

SERVICE

Conference Program Committee Member
HPCA 2019, HPCA 2018, IPDPS 2017, ICS
2016

External Review Committee Member
MICRO 2019, HPG 2017, ISCA 2015, HPCA
2015, ISCA 2014, MICRO 2012, HPCA 2012

Journal Reviewer
ACM TACO

Co-organizer
3rd JILP Workshop on Computer Architecture
Competitions (Memory Scheduling
Championship). Held with ISCA-2012.