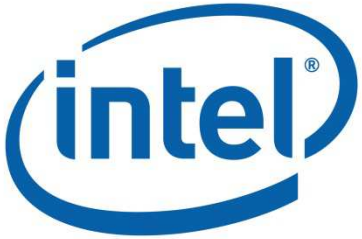
Leveraging Heterogeneity in DRAM Main Memories to Accelerate Critical Word Access



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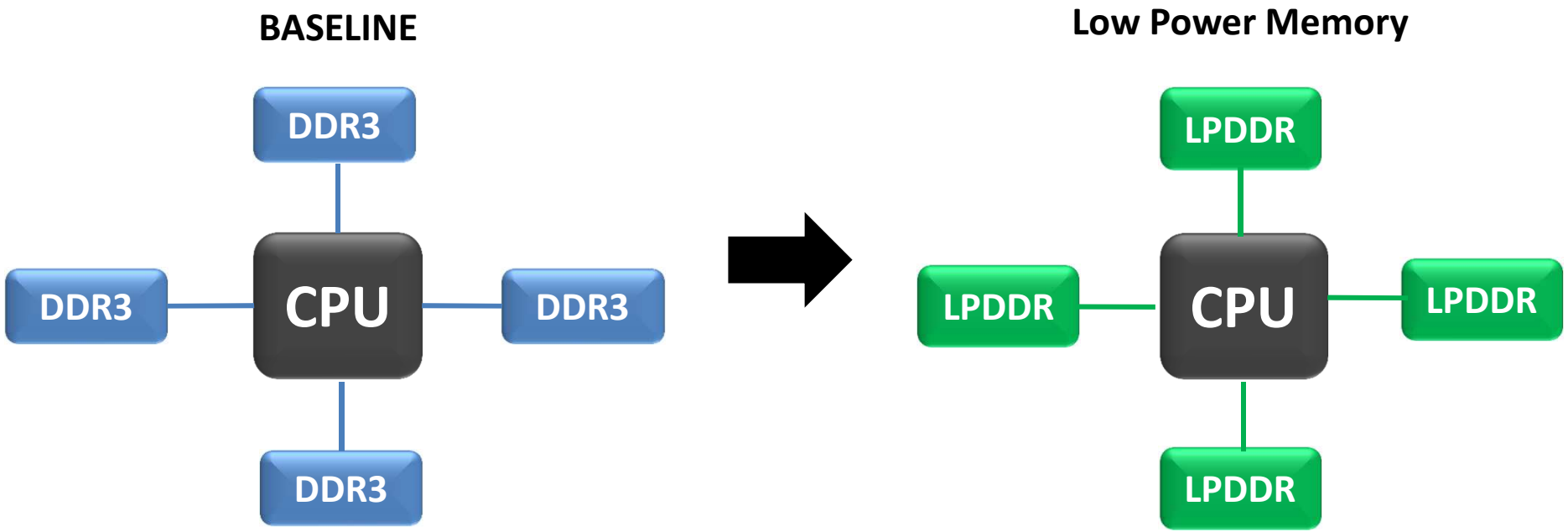
Memory Bottleneck

- High DRAM power consumption
- Recent proposals for Low-Power DRAM instead of DDR3



- The use of LPDRAM does not address the latency wall problem that continues to grow

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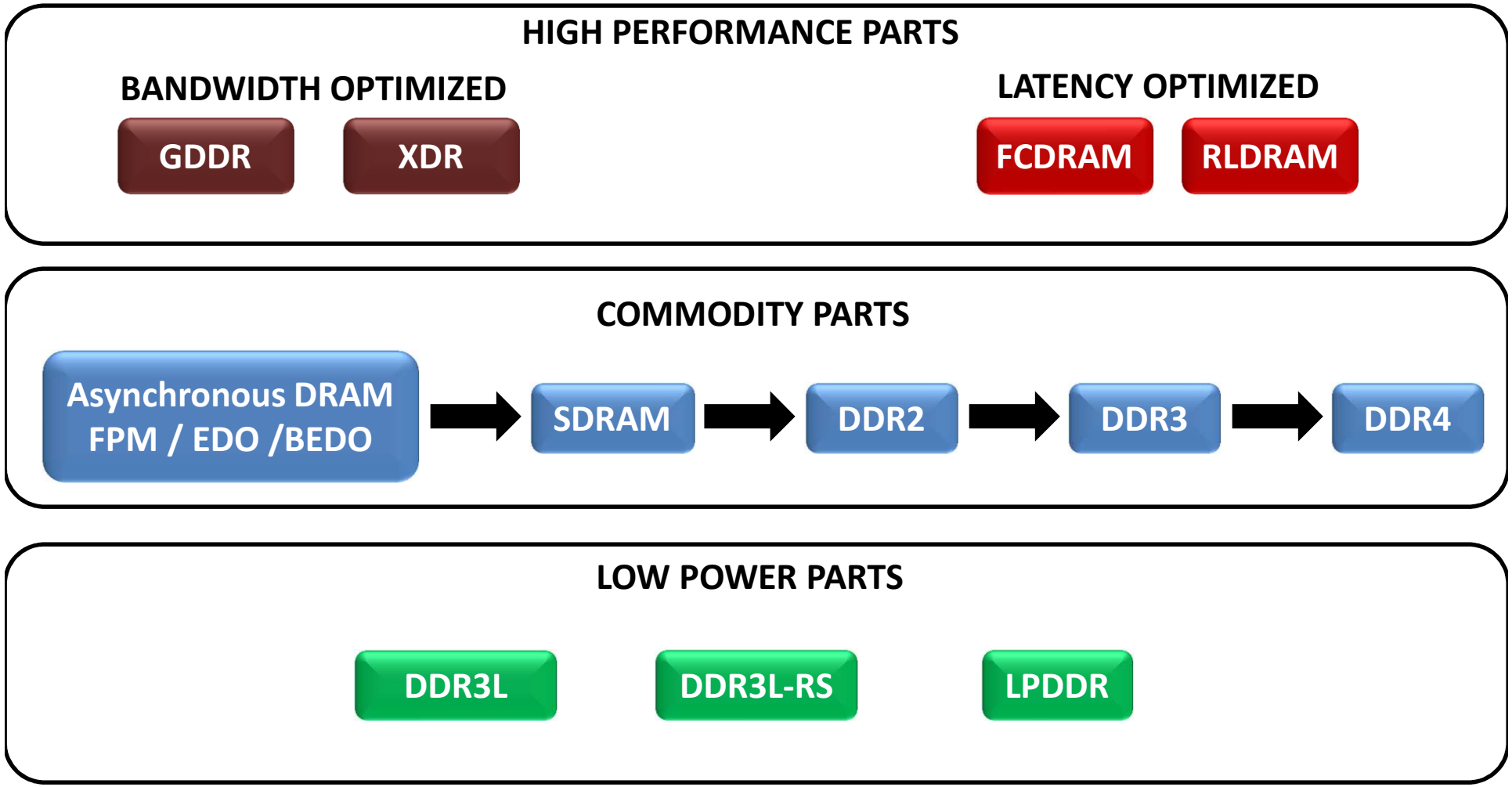
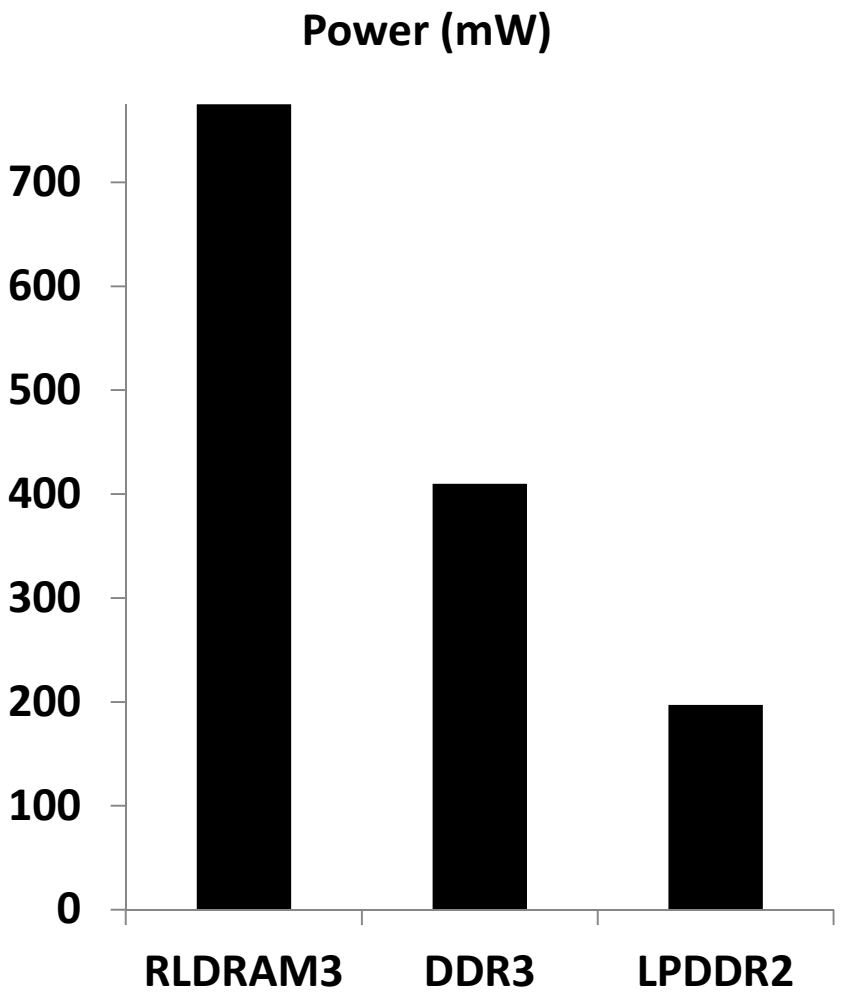
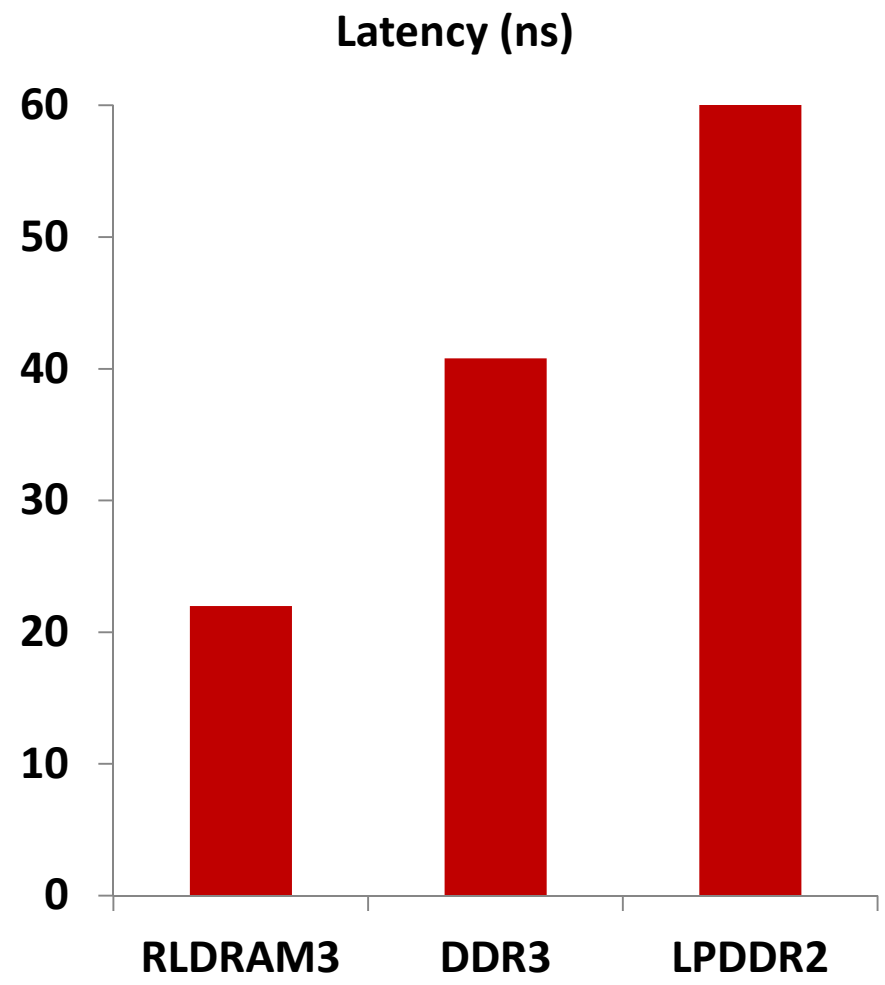
DRAM Variants



No one memory works best





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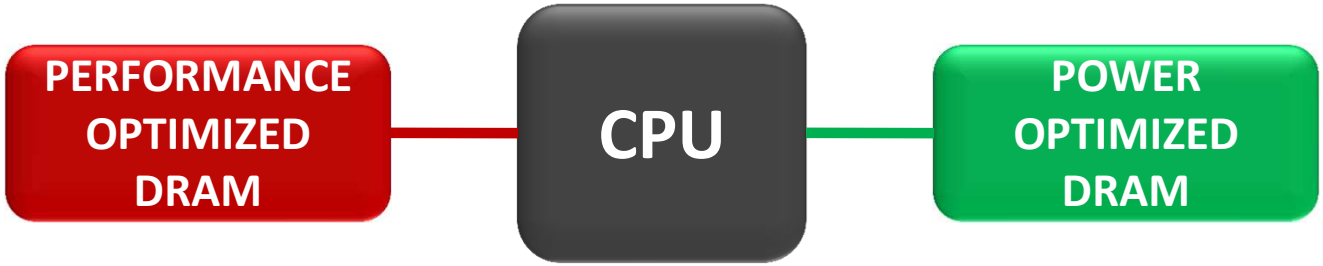
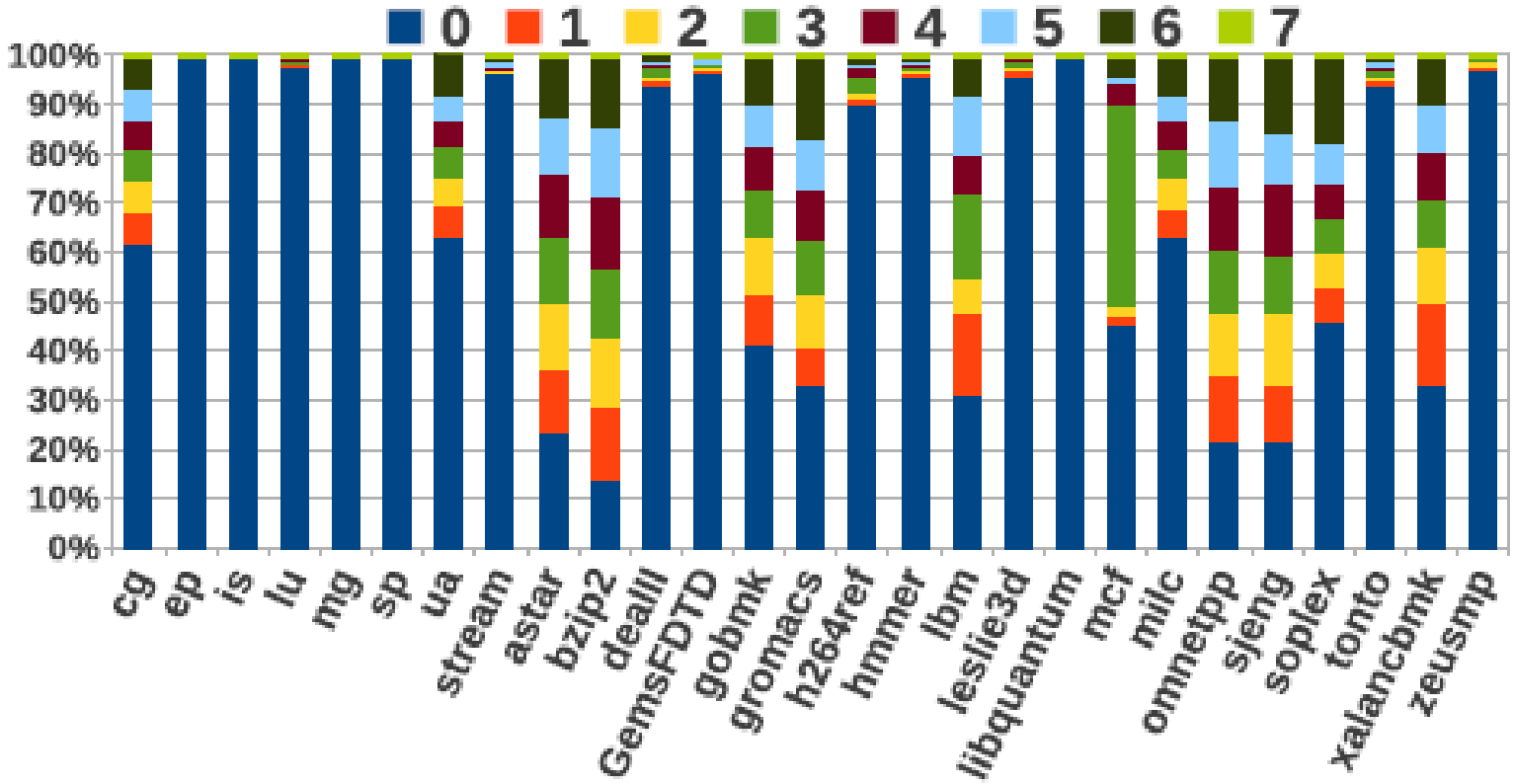
Heterogeneous Memory



- Combine high-performance and low-power dram to outperform DDR3 at a lower energy cost
- Many design options

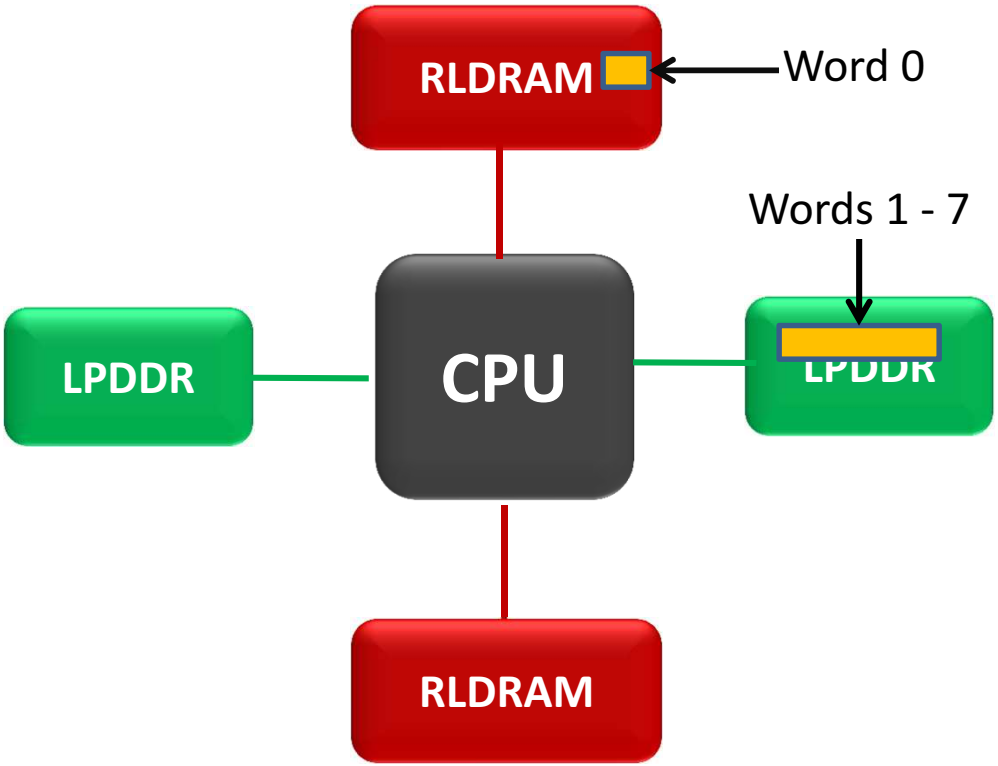
Critical Word Regularity



Frequency of accesses to individual words of a cache-line

- Most DRAM requests are for word-0 of the cache-line

Critical Word Acceleration



- Critical Word from RLDRAM
- Rest of cache-line from LPDRAM
- Improves both system throughput (13%) and energy (6%)

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