A biomedical SoC architecture for predicting ventricular arrhythmia

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Summary

- **Electrocardiography**, method of graphic tracing of the electric current generated by the heart muscle during a heartbeat. The tracing is recorded with an electrocardiograph, and it provides information on the condition and performance of the heart. This paper provides low power solution to predict ventricular arrythmia. This algorithm does ECG feature extraction with ultra-low power requirements. The architecture is based on Curve Length Transform (CLT) for the detection of QRS complex. QRS complex has the highest slope and CLT further enhances it and suppresses the TP waves making it easier to detect the QRS complex.

Brief

- The code has been divided into a test bench: 'test_clt.v' and the main module: 'CLT.v'.
- We've generated the testbench inputs using an actual ECG signal of 500 samples.
- The code has been well commented to give the reader understanding of the algorithm and has been implemented using an approximate version of CLT given in research paper(Ultra-Low Power QRS Detection and ECG Compression Architecture for IoT Healthcare Devices)

Algorithm

- Using the first 200 samples, we compute the threshold of CLT value on a batch size of 32 to qualify as a QRS section.
- After getting the threshold, we perform real time computation on the incoming signals and compare the CLT value for every batch of size 32 with the above computed threshold using a sliding window approach.
- Now we implement an FSM as given in the paper as follows:

➢ If the CLT value is less than the threshold, it is not a QRS section and ignored.

➢ Else, the FSM enters the next state where it checks if this CLT value is greater than the previous one. If yes, the process is continued, else this current value is the CLT maxima.

Algorithm

- Now we enter the third state of the FSM.
- After getting the CLT maxima and the corresponding sample number, we traverse back 15 values of the stored ECG signals and compute the maxima. This maxima corresponds to the R-peak.
- After getting the R-peak, we move 15 values backward and forward of the stored ECG signals to get the minima in both cases. These minimas correspond to the Q-peak and S-peak respectively.
- The sample and window sizes(15, 32 ,etc) used have been carefully decided in the research paper.

Simulation Output & Analysis

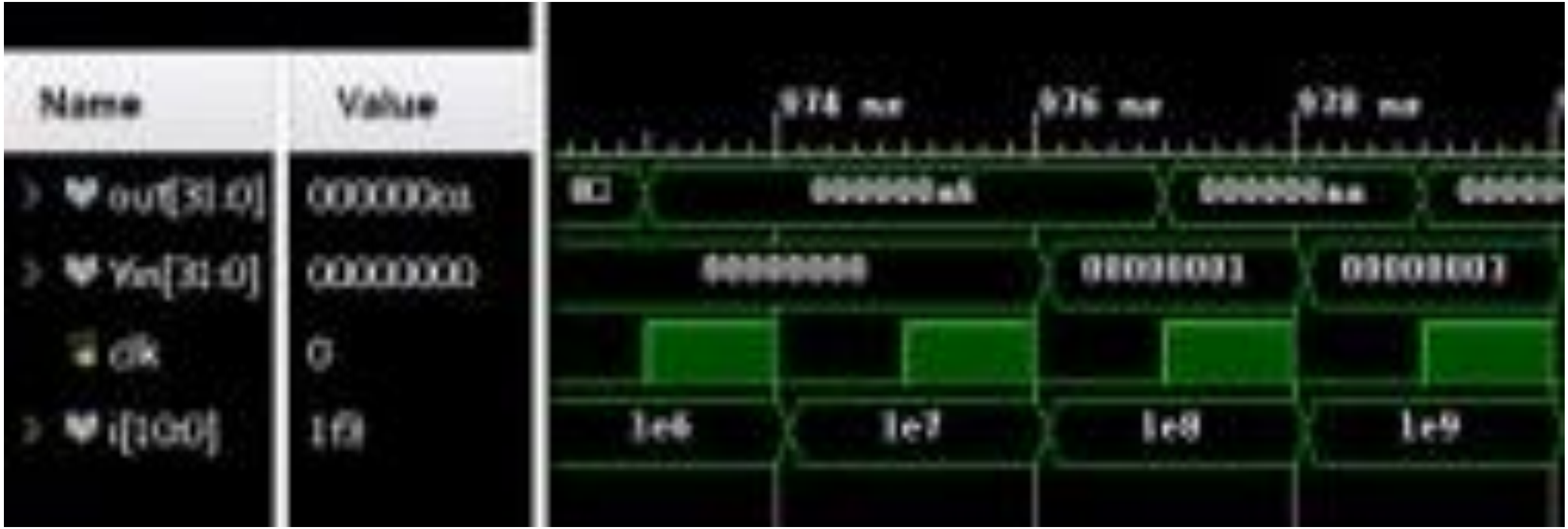
- The above code when simulated displays the Q,R and S peak value and their sample numbers in the output display area.
- The simulation window shows the inputs being stored in the array, the clock pulse, the calculated CLT value on 32 batch-sized inputs and sample number.
- The time delay has been experimentally chosen to provide sufficient time for calculations before the next input. Since this algorithm uses a causal system, future values are not needed.
- The inputs are provided after every 2000 ps and the clock switches at 1000 ps. Since calculations take place at the positive edge of the clock, inputs are synchronized.

Space & Time Complexity

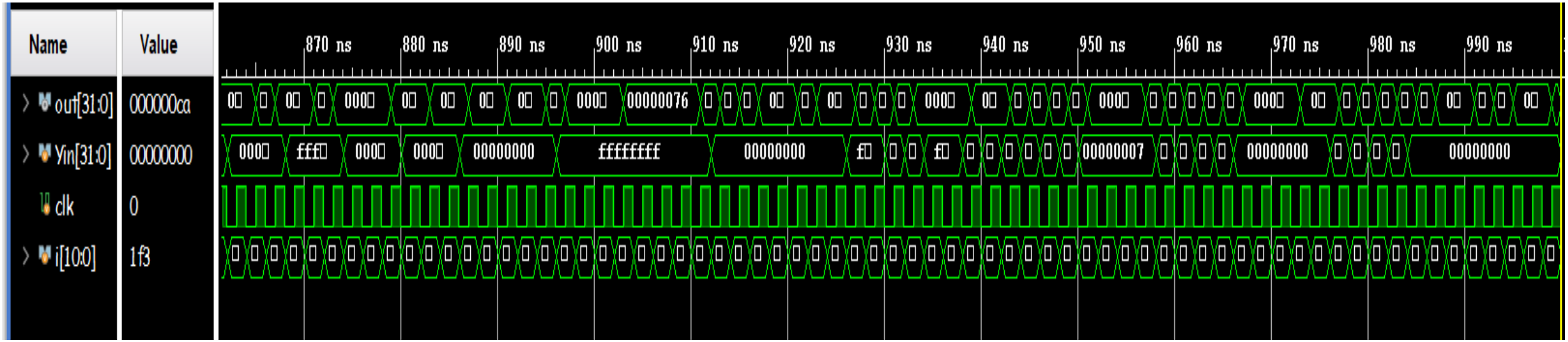
- The array(mem) is a 32-cell storage and each cell stores a 32-bit binary number in 2's complement form.
- The sample number is given as an 11-bit binary number.
- The simulation result is also a 32-bit value in 2's complement form which gives the value of CLT performed on the signal.
- Hence, the space complexity is constant and thus O(1).
- Since we use a sliding window approach and a memory to store the last 31 input signal values, the time complexity is O(1). Hence the given delay of 2000 ps between the input signals always gives accurate results.

Output :

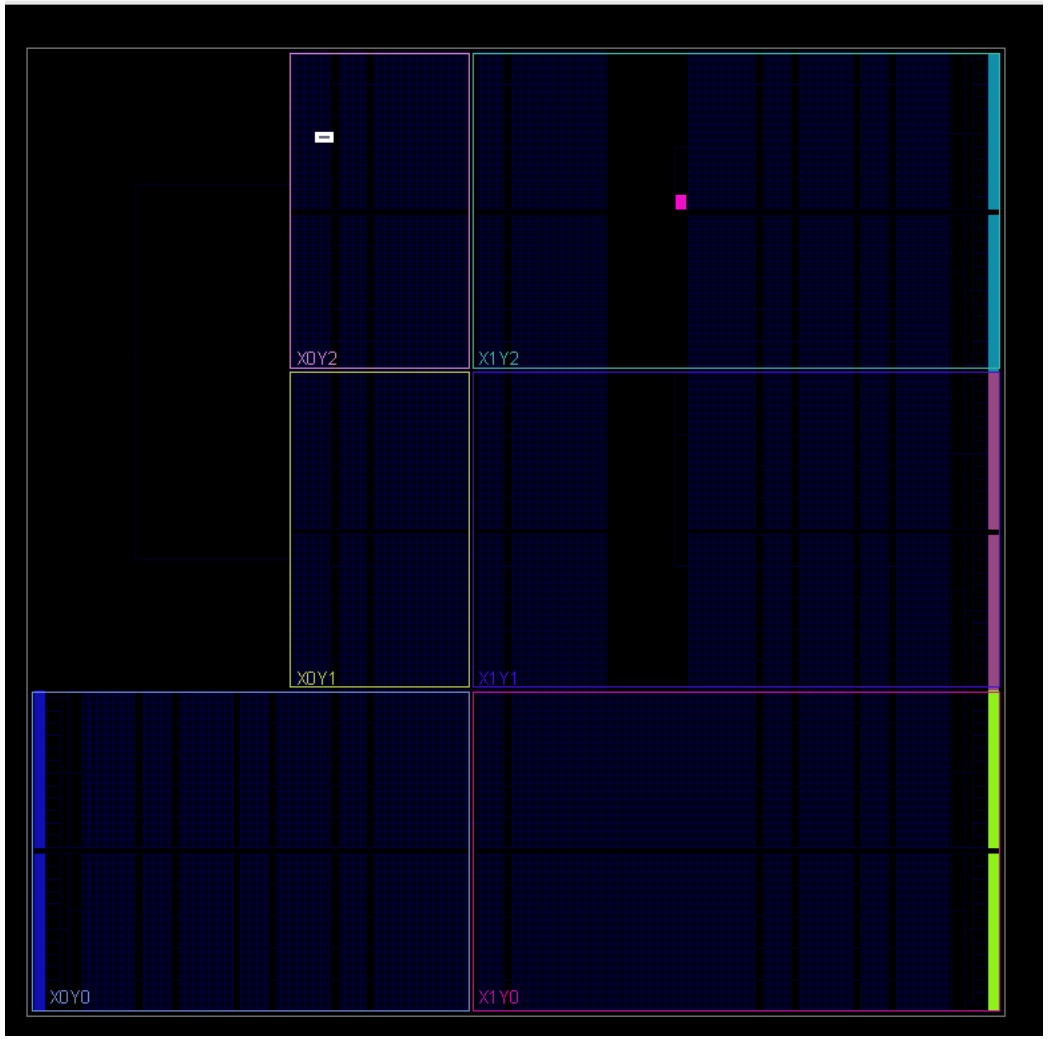
```
# run 1000ns
 R peak value is          13  and sample number is         322
 Q peak value is          -3  and sample number is         306
 S peak value is         -36  and sample number is         337
```



An overall view of simulation:



Floorplanning of the device:



(Zoomed version)

Power estimation from synthesized netlist:

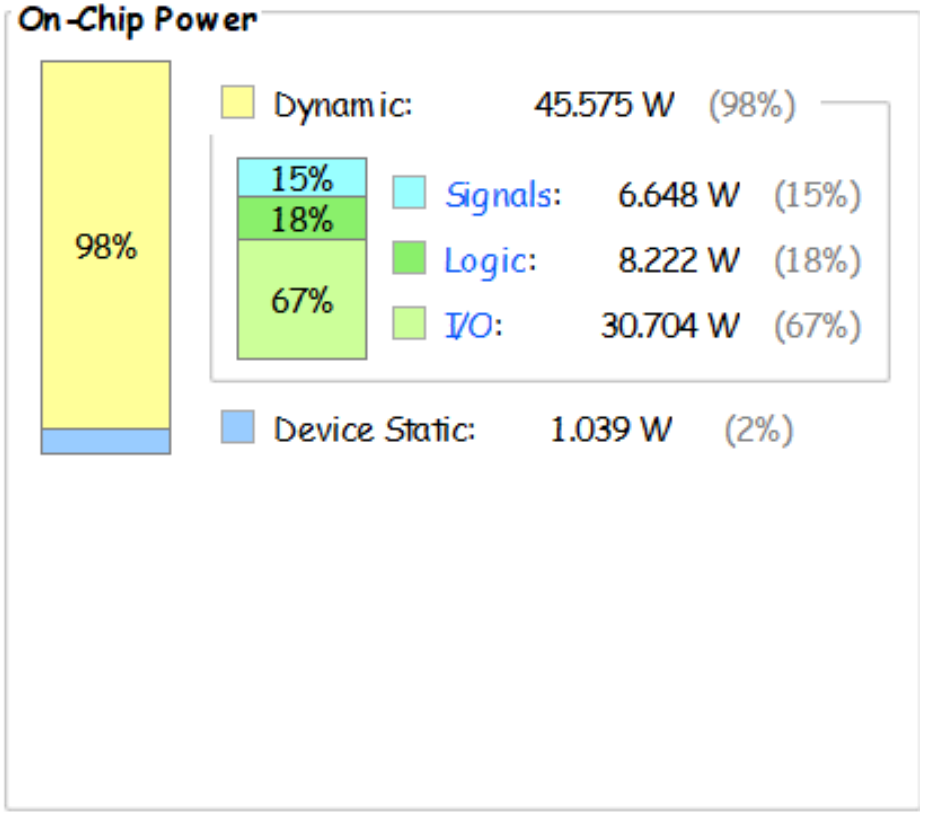
Reports | Design Runs | Power ×

Summary

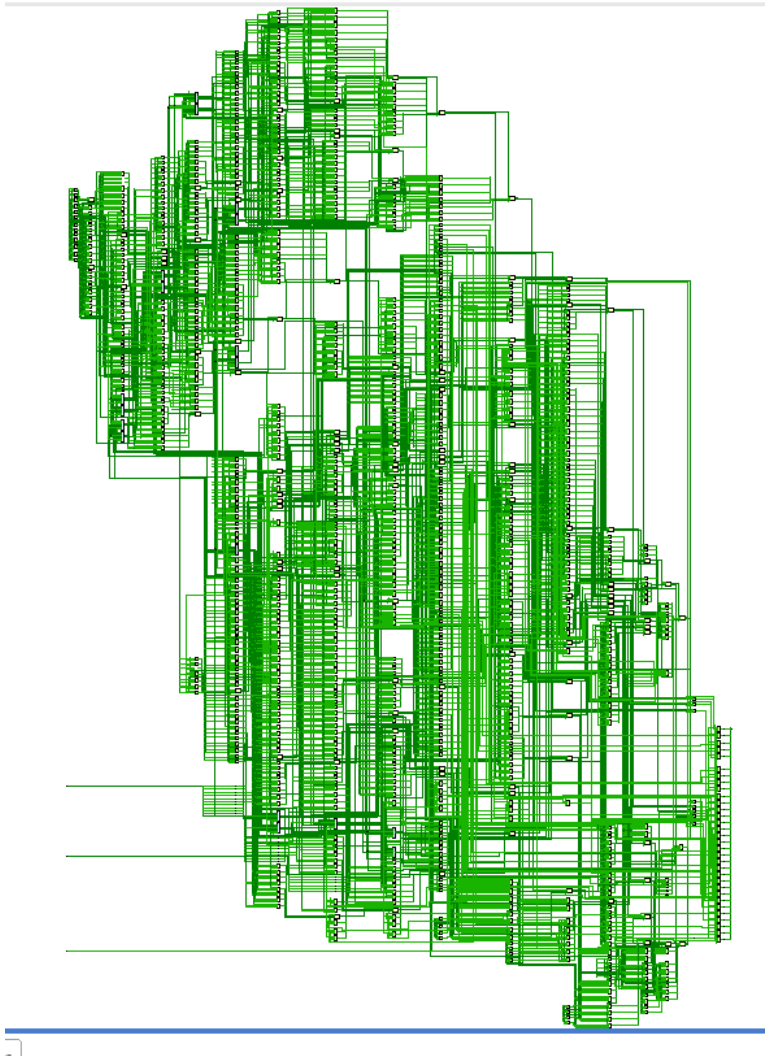
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**46.614 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**125.0°C**
Thermal Margin:	-477.6°C (-40.6 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

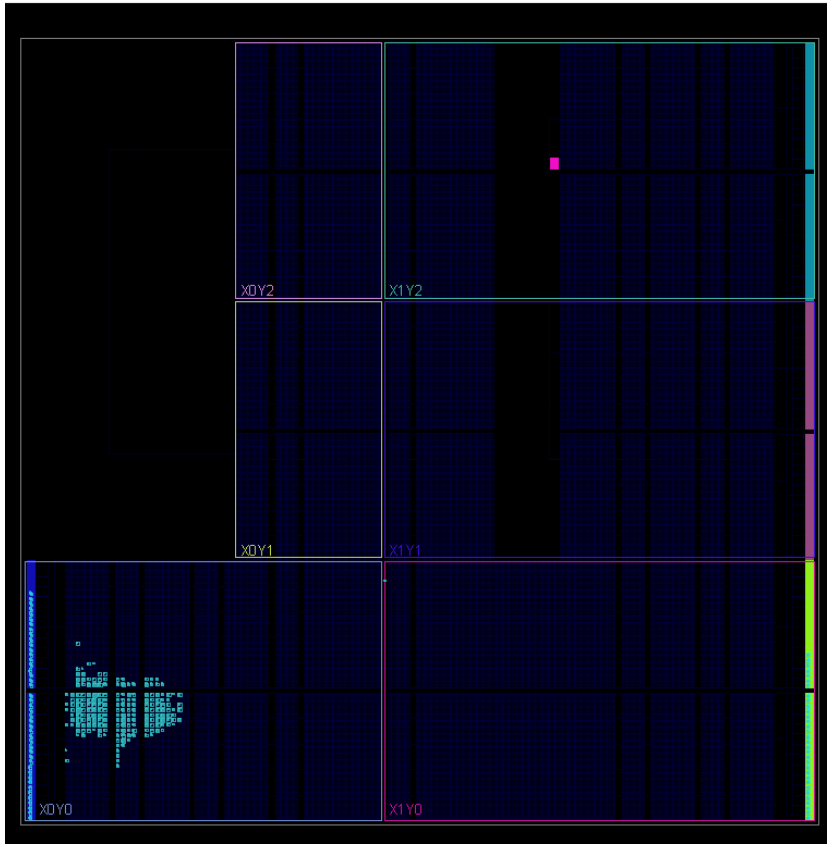


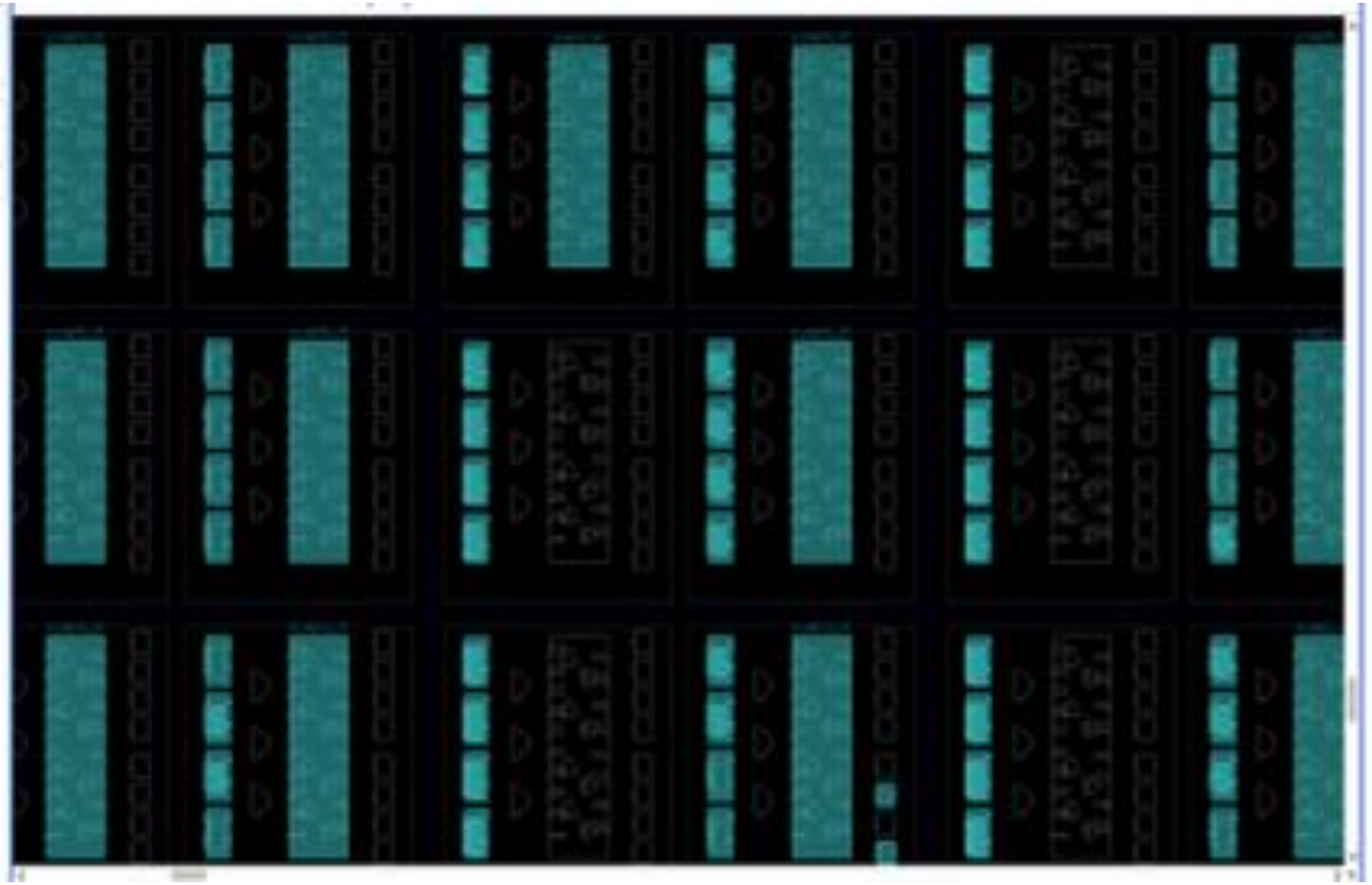
Schematic:



(Zoomed view)

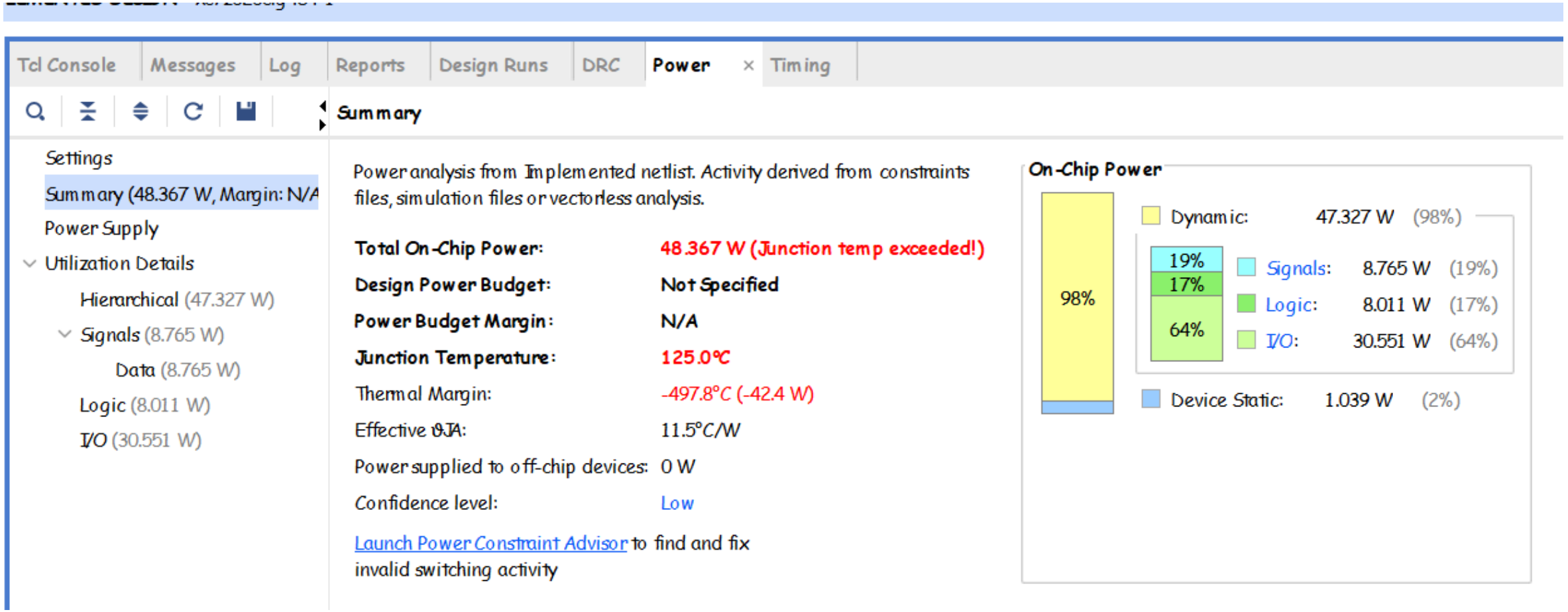
Default layout of the device:



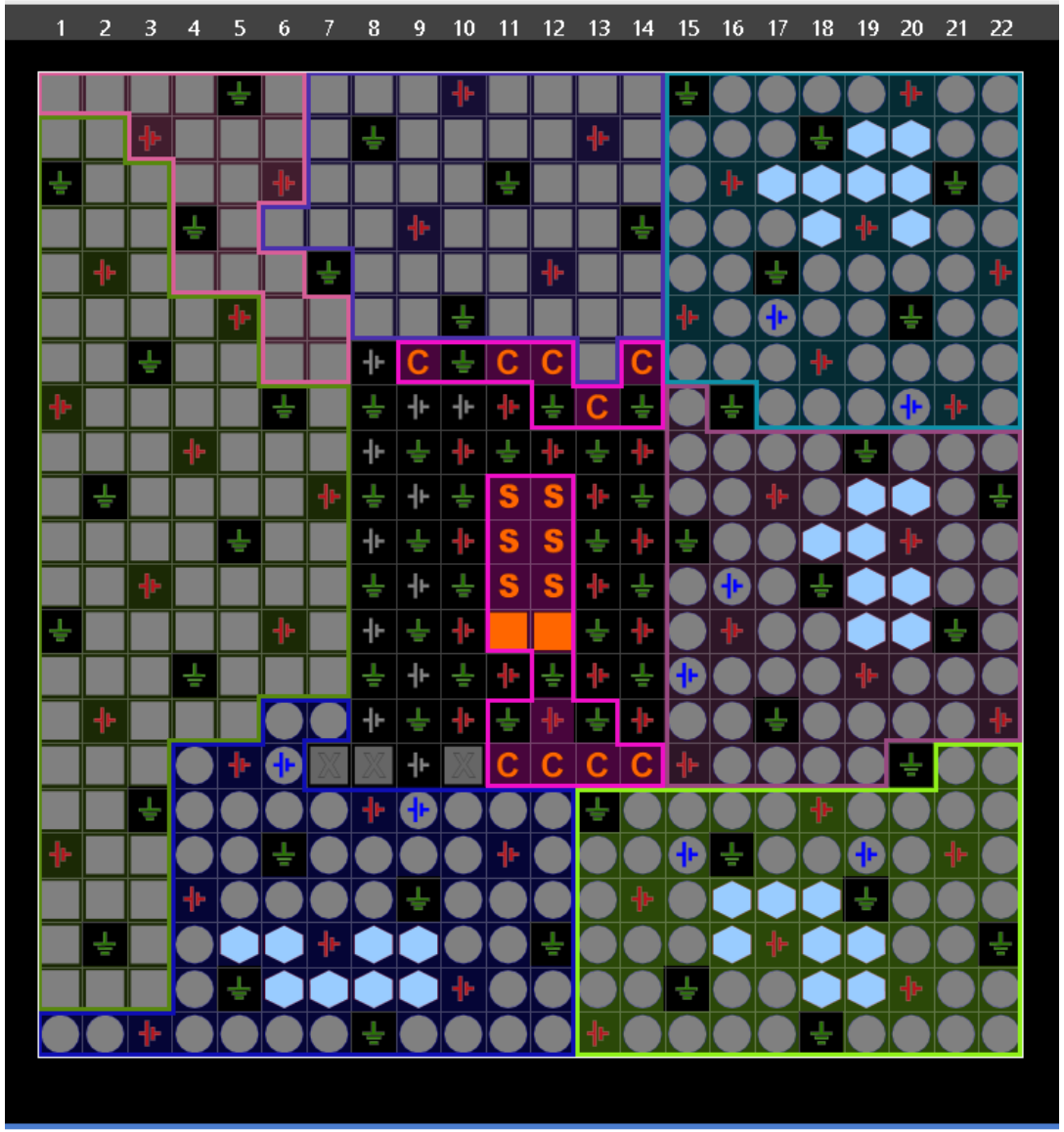


(Zoomed view)

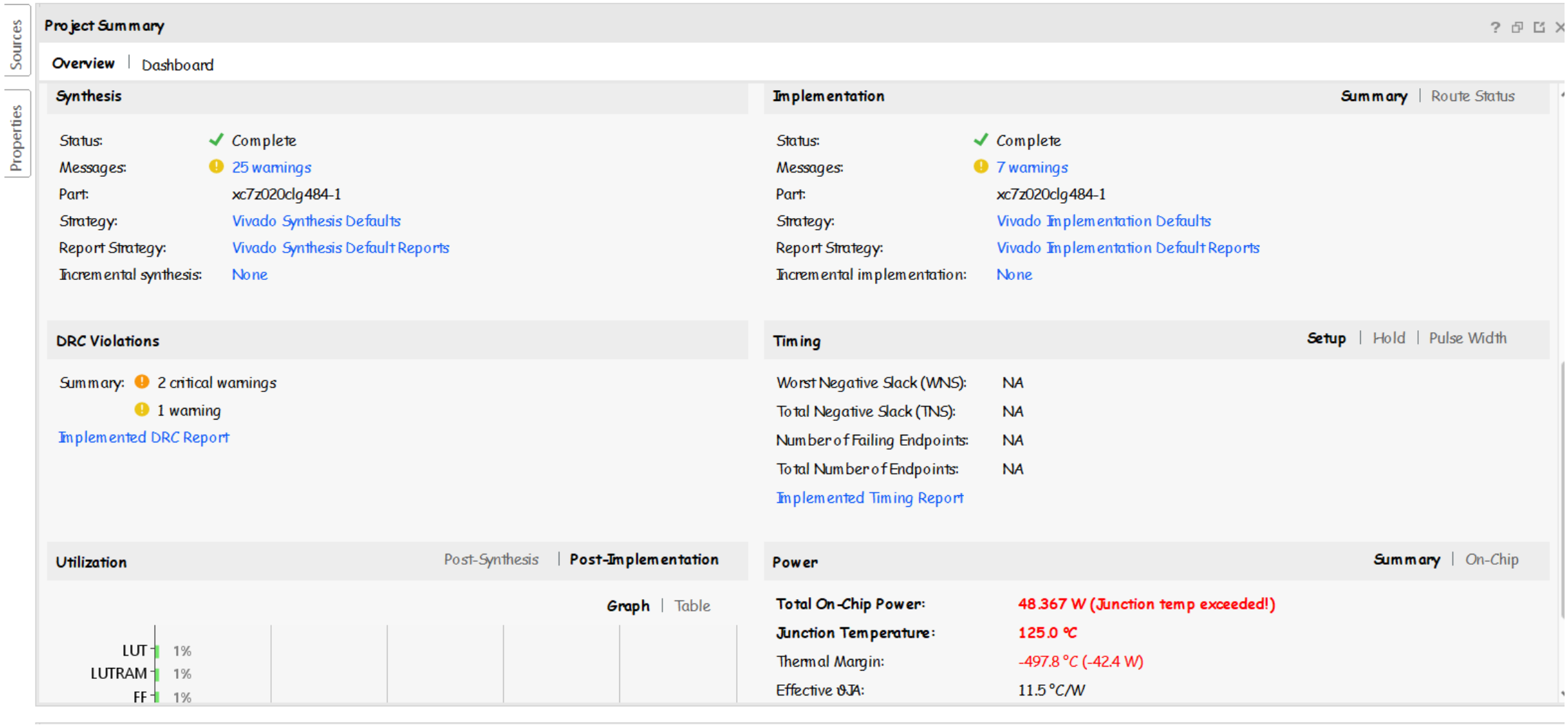
Power estimation from implemented netlist:



Package I/O Planning:



Project summary:



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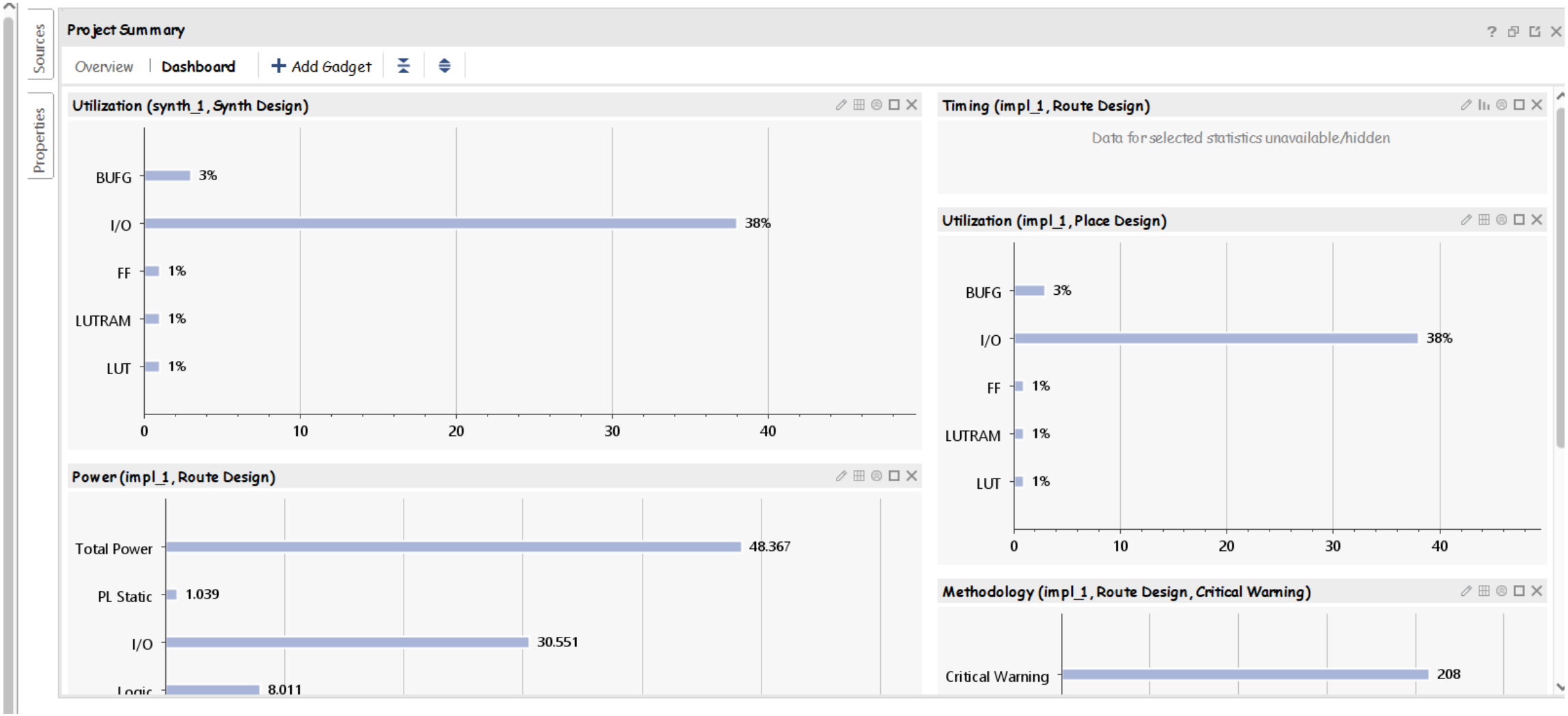
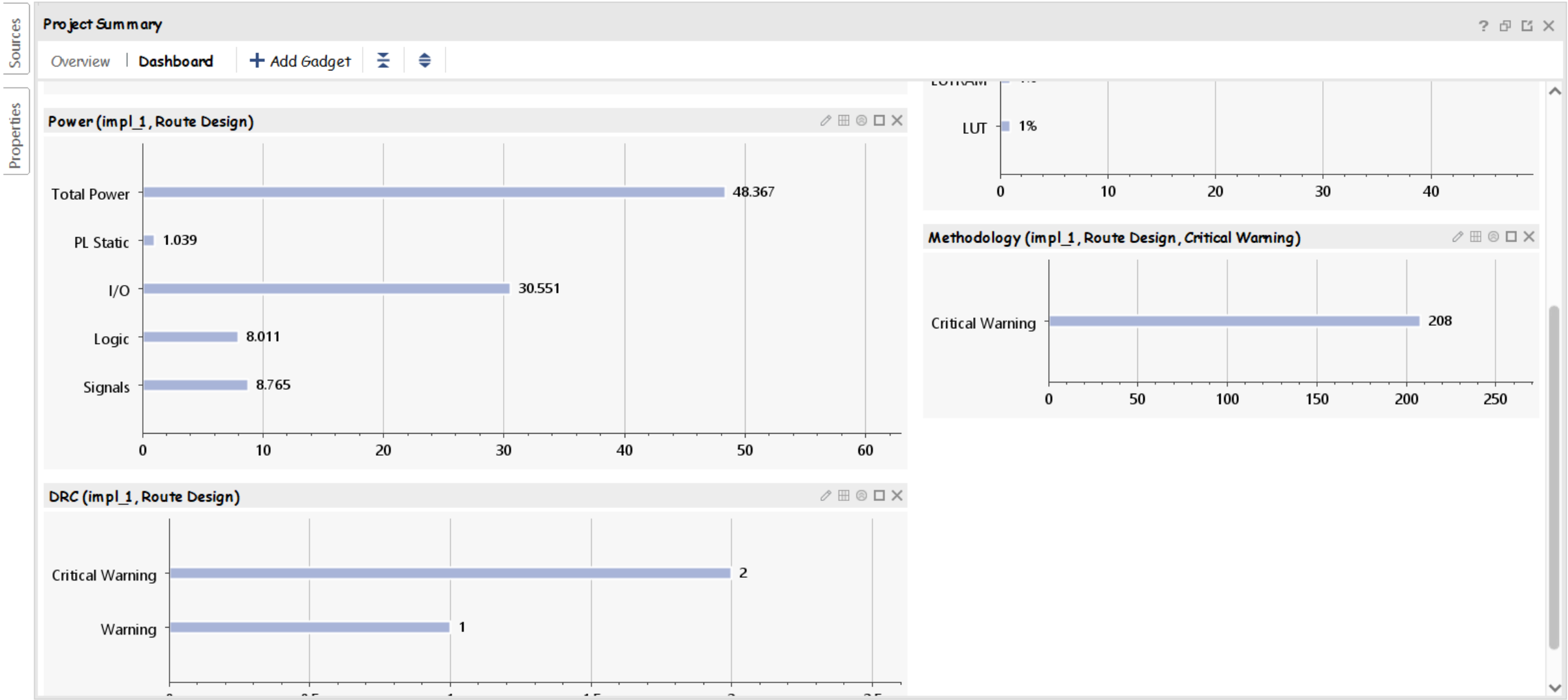
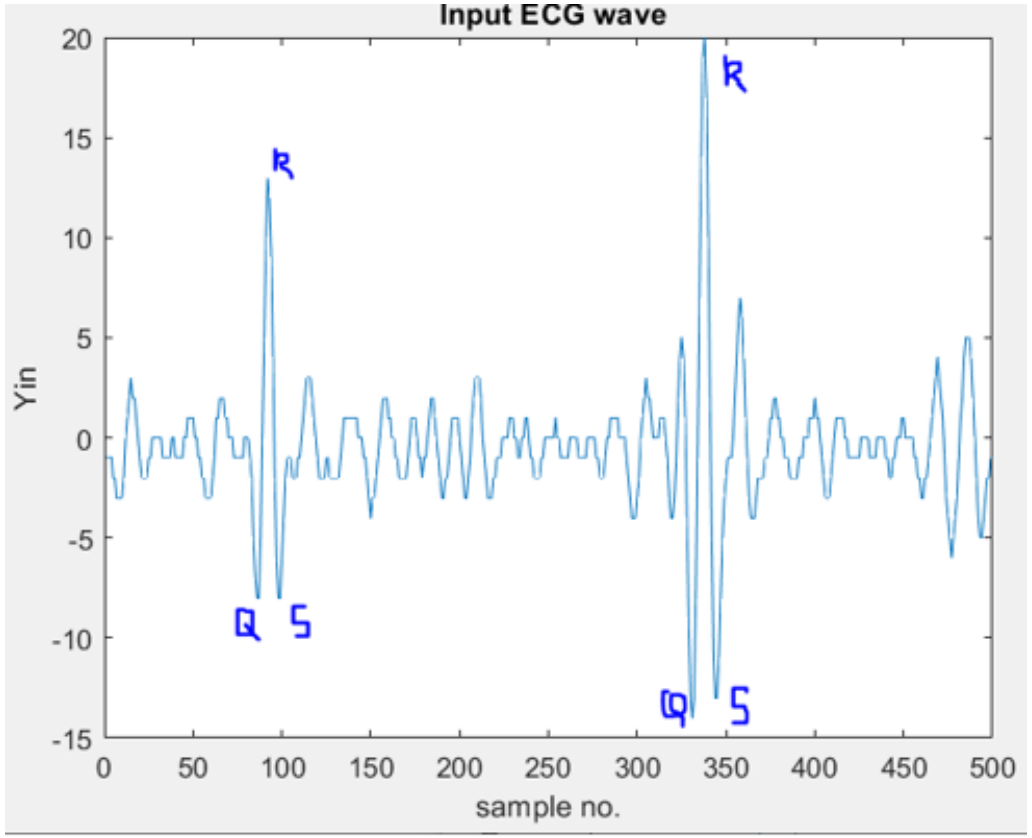


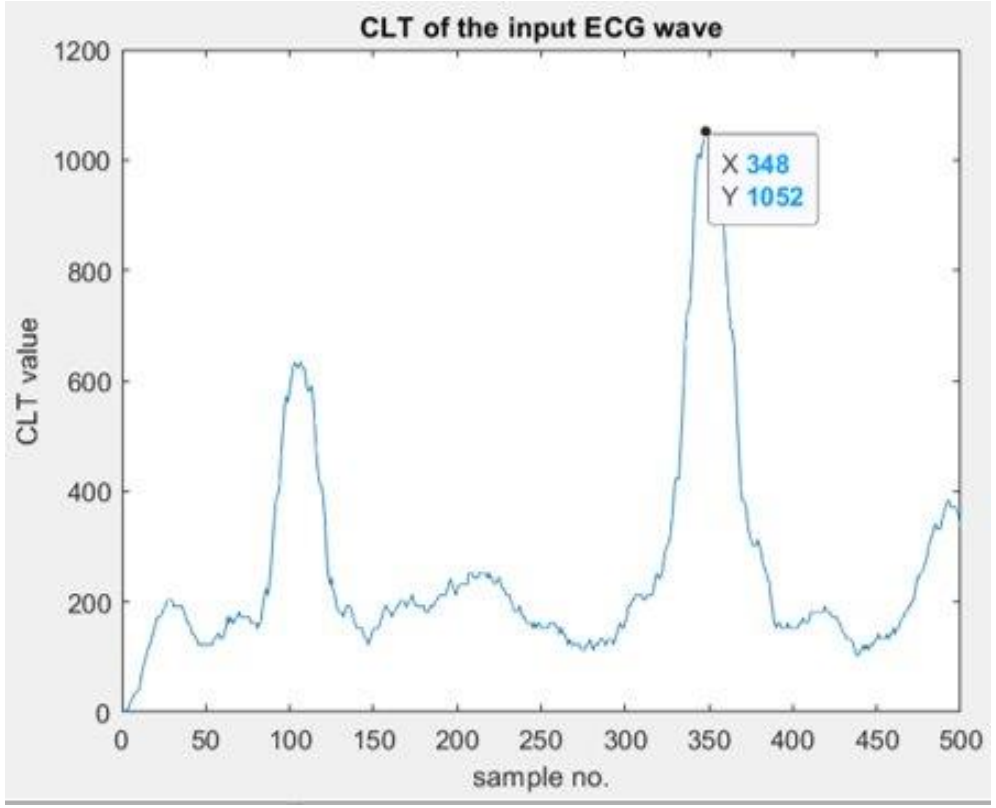
Project summary:

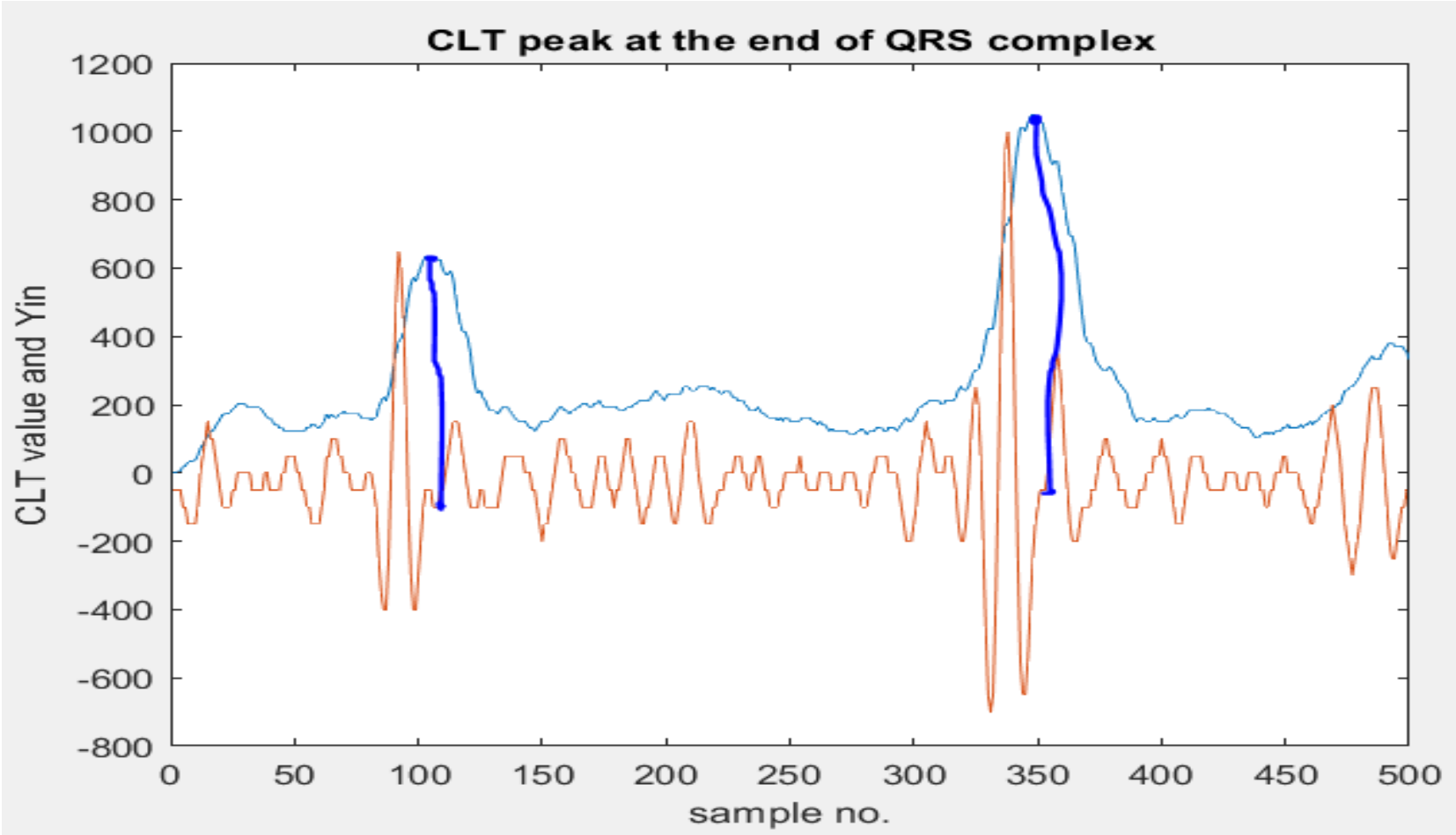


Conclusion:

- Our results match with the theoretical(expected) results as has been verified by plotting the waveform on MATLAB.







As evident from the graph, the CLT peak is at sample 348 which matches the experimental results. As expected, we found that the Q-peak is at sample 306, R-peak at sample 322 and S-peak at sample 337 which are graphically verified from the previous slide.The threshold for CLT peak is calculated from the first 200 samples as shown.