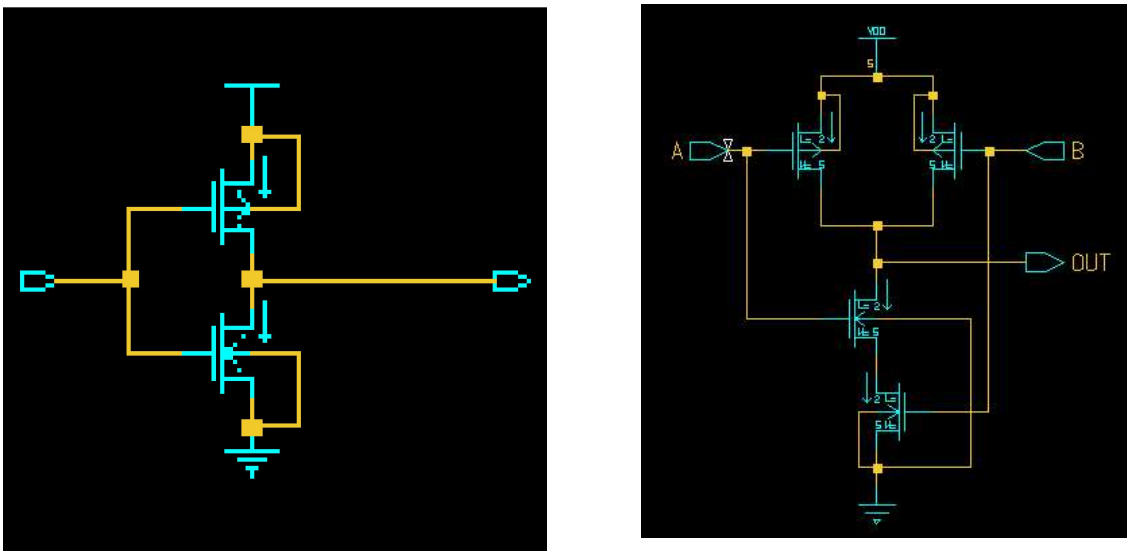
CIRCUIT DIAGRAM



CMOS Inverter

Theory:

Inverter Static Characteristics (VTC)

Digital inverter quality is often measured using the Voltage Transfer Curve (VTC), which is a plot of input vs. output voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained.

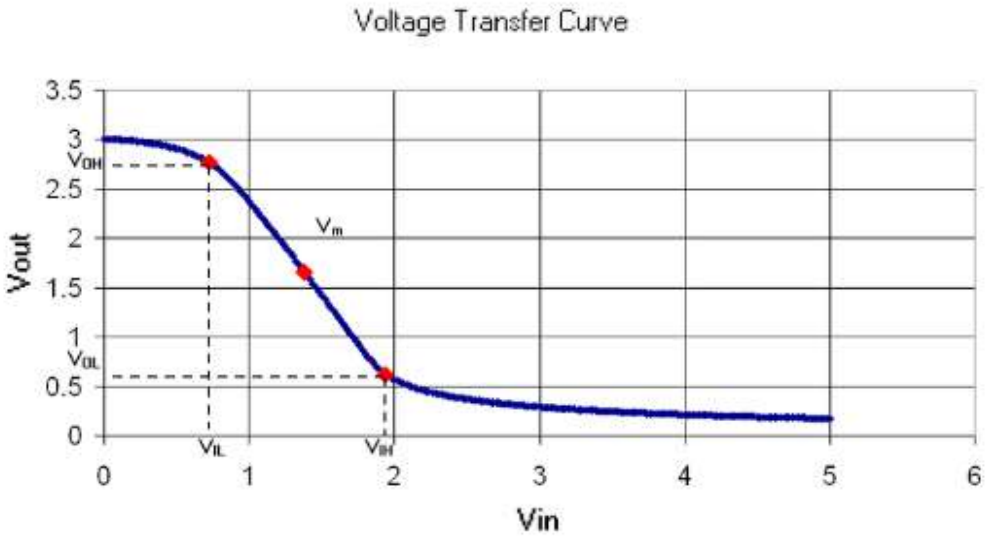


Fig.2: Voltage Transfer Curve for a typical 20 µm Inverter

Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between on and off - but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts. The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching. The tolerance to noise can be measured by comparing the minimum input to the maximum output for each region of operation (on / off). This is more explicitly shown in the fig.3.

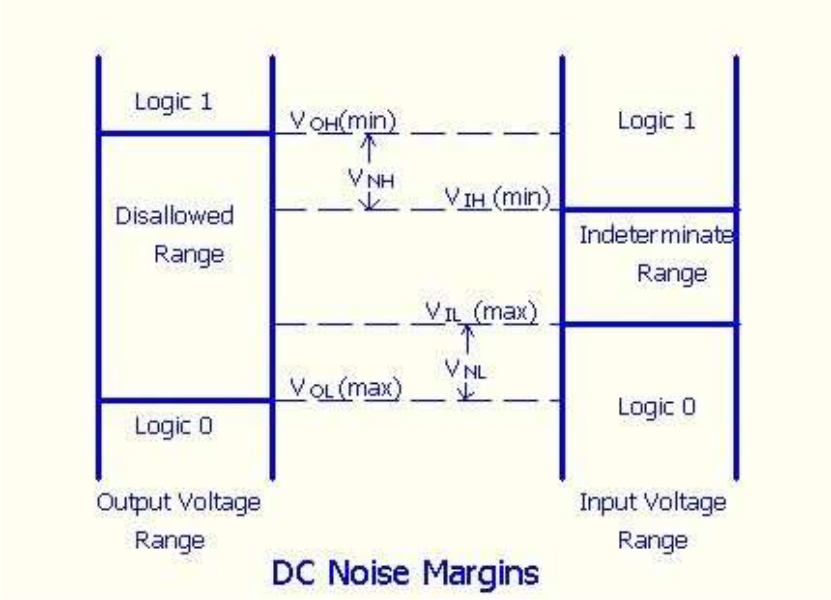


Fig.3: Definition of noise margin

Noise margin : is a parameter intimately related to the transfer characteristics. It allows one to estimate the allowable noise voltage on the input of a gate so that the output will not be affected. Noise margin (also called noise immunity) is specified in terms of two parameters - the low noise margin NL, and the high noise margin NH . Referring to above figure, NL is defined as the difference in magnitude between the maximum LOW input voltage recognized by the driven gate and the maximum LOW output voltage of the driving gate. That is, NL =|

VIL - VOL|. Similarly, the value of NH is the difference in magnitude between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognizable by the driven gate. That is, NMH =|VOH - VIH|. Where VIH: minimum HIGH input voltage, VIL: maximum LOW input voltage, VOH: minimum HIGH output voltage, VOL: maximum LOW output voltage.

Inverter Dynamic Characteristics

Fig.4 shows the dynamic characteristics of a CMOS inverter. The following are some formal definitions of temporal parameters of digital circuits. All percentages are of the steady state values.

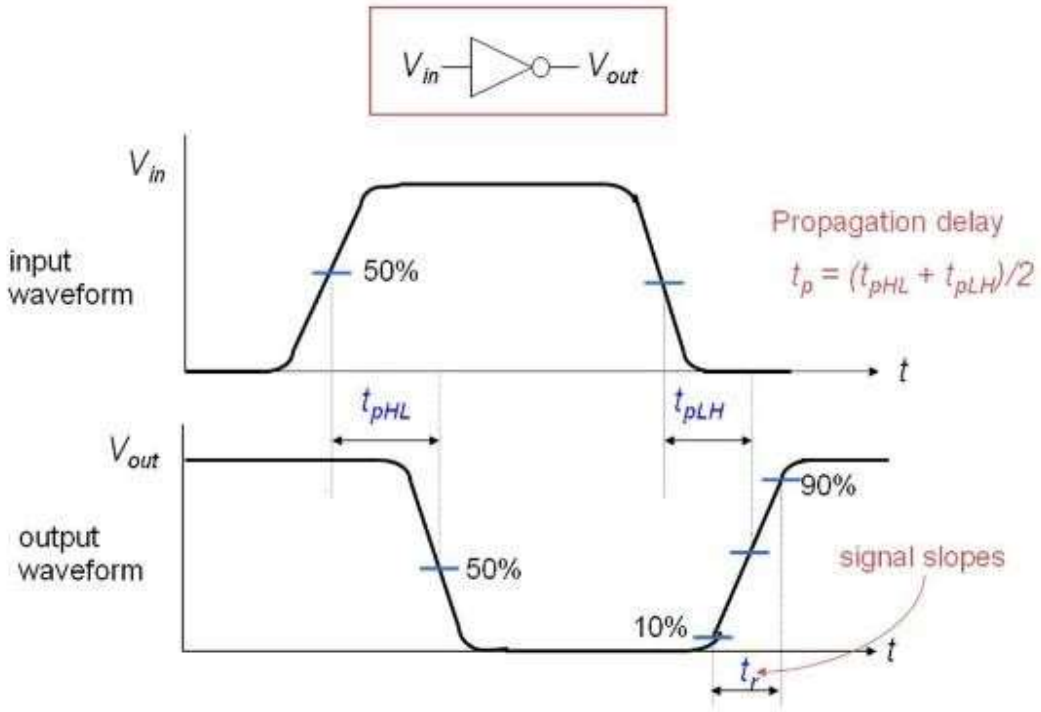
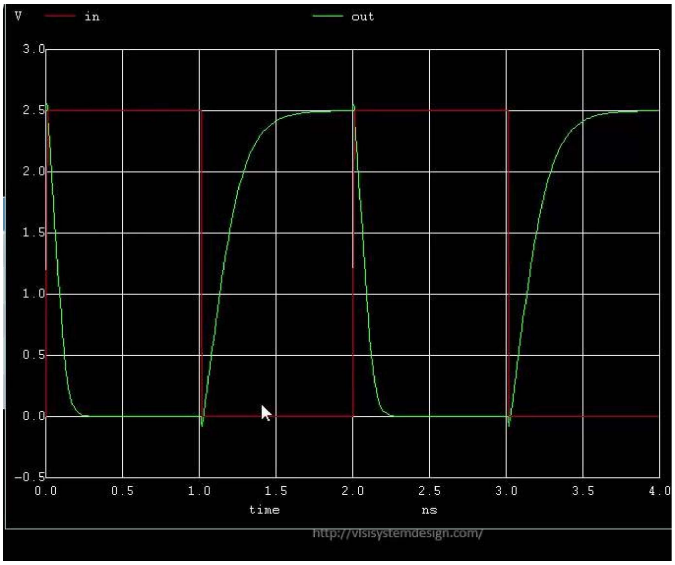


Fig.4: Dynamic characteristics of CMOS inverter

Rise Time (tr) : Time taken to rise from 10% to 90%.
Fall Time (tf): Time taken to fall from 90% to 10%.
Edge Rate (trf): (tr + tf)/2.
High-to-Low propagation delay (tpHL): Time taken to fall from VOH to 50%.
Low-to-High propagation delay (tpLH): Time taken to rise from 50% to VOL.
Propagation Delay (tp): (tpHL + tpLH)/2.
Contamination Delay (tcd): Minimum time from the input crossing 50% to the output crossing 50%

Output:



Characteristics of Inverter

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