ECE 510: Pre-Silicon Validation
Laboratory 1

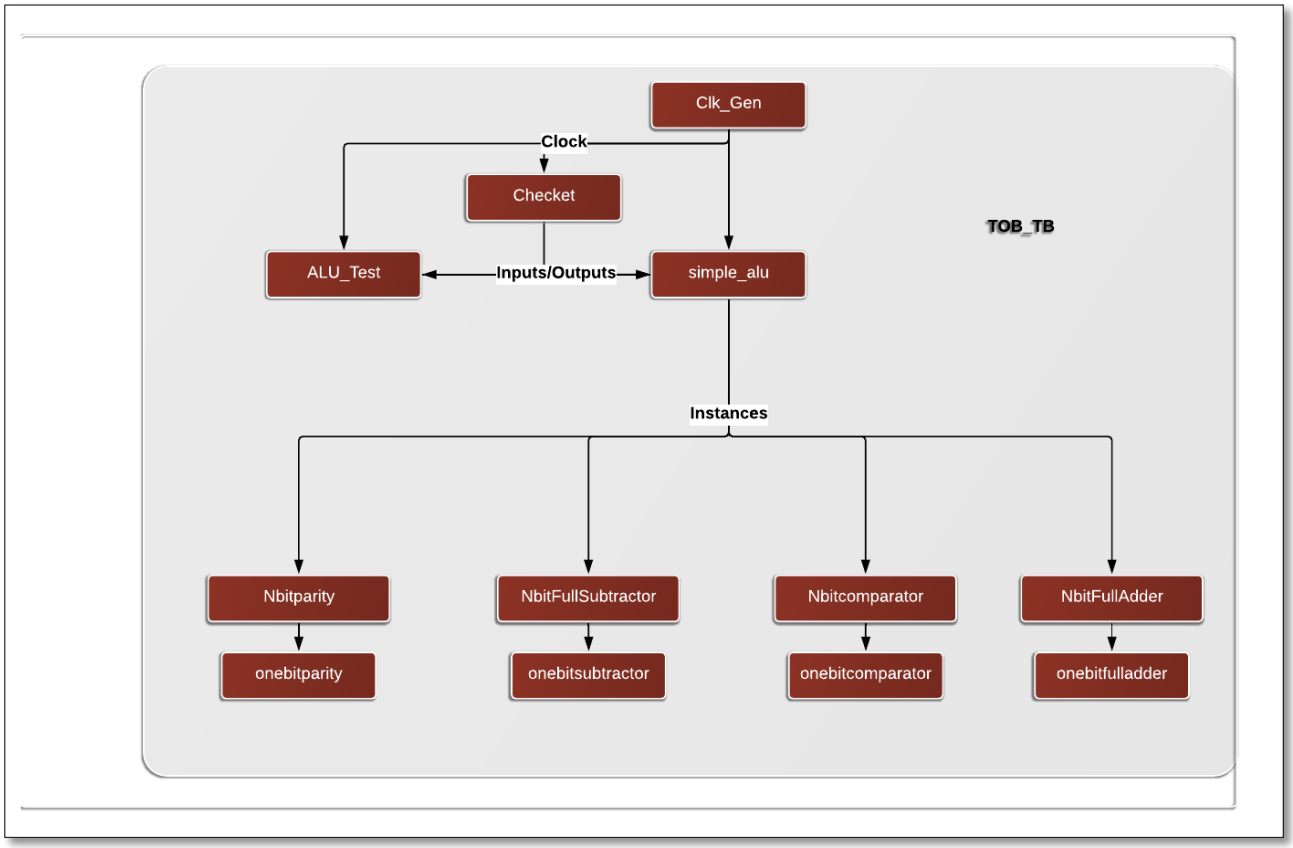
Nilesh Dattani

PSU ID: 958880624

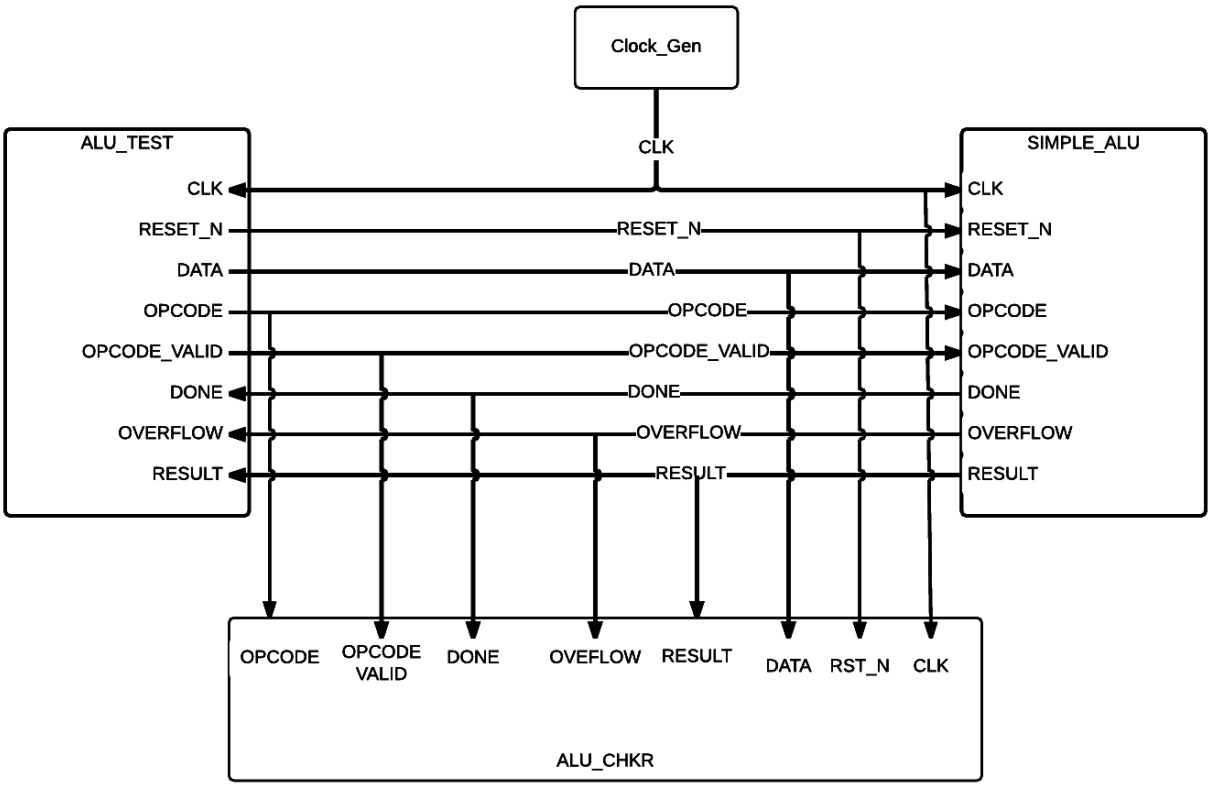
Portland State UNIVERSITY

High Level Block Diagram

```
clkgen_driver clkgen(.clk(clk));
alu_test_new   i1(.clk(clk),.reset_n(reset_n),.opcode_valid(opcode_valid),.opcode(opcode),.data(data),.done(done),.overflow(overflow),.result(result),.simulation_end(simulation_end));
simple_alu i2(.clk(clk),.reset_n(reset_n),.opcode_valid(opcode_valid),.opcode(opcode),.data(data),.done(done),.overflow(overflow),.result(result));
alu_chkr chkr1(.clk(clk),.reset_n(reset_n),.opcode_valid(opcode_valid),.opcode(opcode),.data(data),.done(done),.overflow(overflow),.result(result),.simulation_end(simulation_end));
```



Block Diagram with connections at high level



Assumptions:

- FSM State IDLE should clear the done bit and should not change any other outputs, i.e. hold their values
- Logical Operators are the lowest level of code writing expected
- Delay were not accounted for the simulation
- Race conditions could be ignored
- Arithmetic operations are unsigned operations.

Observations and Results

- The code was simulated and verified with the tester code provided
- Transcript and the source codes are provided with the report in the submission folder
- Files were arranged as required and submitted to d2l.pdx.edu

```
#
# ----------------------------------------SUMMARY-----------------------------------------
#
# DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
# DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992             FAILED = 0
# DATTANI : DONE TEST           (RULE_3):PASSED = 1048544             FAILED = 131068
# DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544             FAILED = 0
# DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544             FAILED = 0
# ----------------------------------------------------------------------------------------
```

Figure 1: No additional bug introduced

Individual Bug Checking

Add separate bugs in the DUT and show the transcript that your checker flags errors for rule#1, 4 & 5. Document where you introduced your bugs in the DUT.

1. Bug introduced for rule 1.

```
always@(state) begin

case(state)
RESET    : begin
           result = {ALU_SIZE{1'b0}};
           done = FALSE;
           overflow = TRUE;
           end
```

Result Observed:

```
----------------------------------------SUMMARY-----------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 0             FAILED = 131069
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992             FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544             FAILED = 131068
DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544             FAILED = 0
DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544             FAILED = 0
----------------------------------------------------------------------------------------
```

Result Observed when RULE_1 disabled:

```
# ----------------------------------------SUMMARY-----------------------------------------------------
#
# DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992              FAILED = 0
# DATTANI : DONE TEST           (RULE_3):PASSED = 1048544              FAILED = 131068
# DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544              FAILED = 0
# DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544              FAILED = 0
# ----------------------------------------------------------------------------------------------------
```

2. Bug Introduced for rule 4

```
module onebitparity(a,b,parity);
input a,b;
output parity;

assign parity = !a^b;

endmodule
```

Result Observed:

```
----------------------------------------SUMMARY-----------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069               FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992              FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544              FAILED = 131068
DATTANI : RESULT CHECK        (RULE_4):PASSED = 786408               FAILED = 262136
DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544              FAILED = 0
----------------------------------------------------------------------------------------------------
```

Result Observed when RULE_4 disabled

```
----------------------------------------SUMMARY-----------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069               FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992              FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544              FAILED = 131068
DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544              FAILED = 0
----------------------------------------------------------------------------------------------------
```

3. Bug introduced for rule 5

```
module NbitFullAdder(a,b,cin,sum,cout);
parameter width = 8;
input [width :1] a,b;
input cin;
output [width:1] sum;
output cout;
wire [width:0]c;

genvar i;
assign c[0]=cin;
generate
for (i=1;i<=width;i=i+1)
onebitfulladder A(.a(a[i]),.b(b[i]),.cin(c[i-1]),.sum(sum[i]),.cout(c[i]));
endgenerate
assign cout = 'x;


endmodule
```

Result Observed:

```
----------------------------------------SUMMARY-------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992             FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544             FAILED = 131068
DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544             FAILED = 0
DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 786408              FAILED = 262136
-----------------------------------------------------------------------------------------------
```

Result Observed when RULE_5 disabled

```
----------------------------------------SUMMARY-------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5766992             FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544             FAILED = 131068
DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544             FAILED = 0
-----------------------------------------------------------------------------------------------
```

Add a bug in the test generator and show the transcript that your checker flags errors for rule#2. Document where you introduced your bug in the test generator

Bug Introduced:

```
// Test sequence 2
int_opcode_valid = 1;
int_opcode = full_opcode[0];
//int_data = ({$random} % 8'hff);
int_data = 8'b00xx_0000;
repeat (CYCLE_TO_LATCH_FIRST_DATA) @(posedge clk);
int_opcode = full_opcode[1];
int_data = ({$random} % 8'hff);
while (done == 0) @(posedge clk);
int_opcode_valid = 0;
delay = ({$random} % 4'hf);
repeat (delay+2)  @(posedge clk);
```

Result Observed:

```
----------------------------------------SUMMARY-------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 5504856             FAILED = 262136
```

Result Observed when RULE_2 disabled:

```
----------------------------------------SUMMARY-------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 1048544             FAILED = 131068
DATTANI : RESULT CHECK        (RULE_4):PASSED = 1048544             FAILED = 0
DATTANI : OVERFLOW CHECK      (RULE_5):PASSED = 1048544             FAILED = 0
----------------------------------------------------------------------------------------------------
```

Bonus: Introduce a bug in the DUT and see if you can get your checker to flag an error for rule#3.

Bug Introduced:

```
COMP    : begin
          result = result_comp;
          overflow = FALSE;
          done=done;
          end

DONE    : begin
          result = result;
          overflow = overflow;
          done = FALSE;
          end
```

```
IDLE    : begin
          result = result;
          done = TRUE;
          overflow = overflow;
          end
```

Result Observed:

```
----------------------------------------SUMMARY-------------------------------------------------

DATTANI : RESET TEST          (RULE_1):PASSED = 131069              FAILED = 0
DATTANI : VALIDITY TEST       (RULE_2):PASSED = 2621360             FAILED = 0
DATTANI : DONE TEST           (RULE_3):PASSED = 0           FAILED = 131068
```