ECE 510: Pre-Silicon Validation

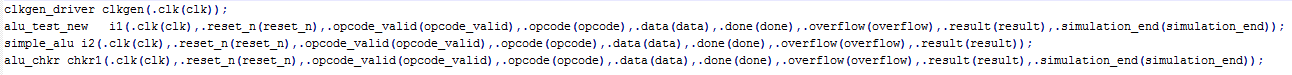
Laboratory 1

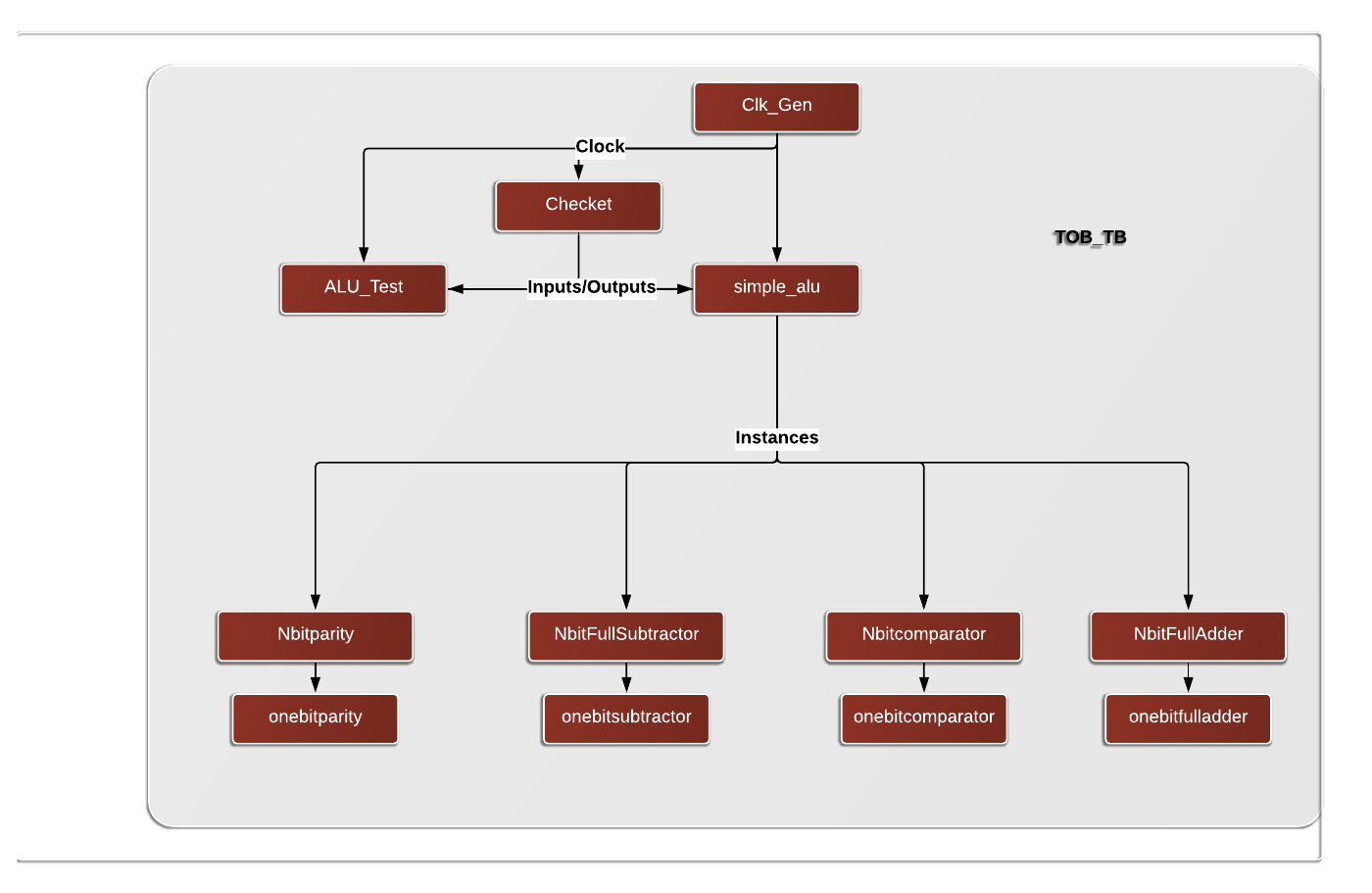


Nilesh Dattani

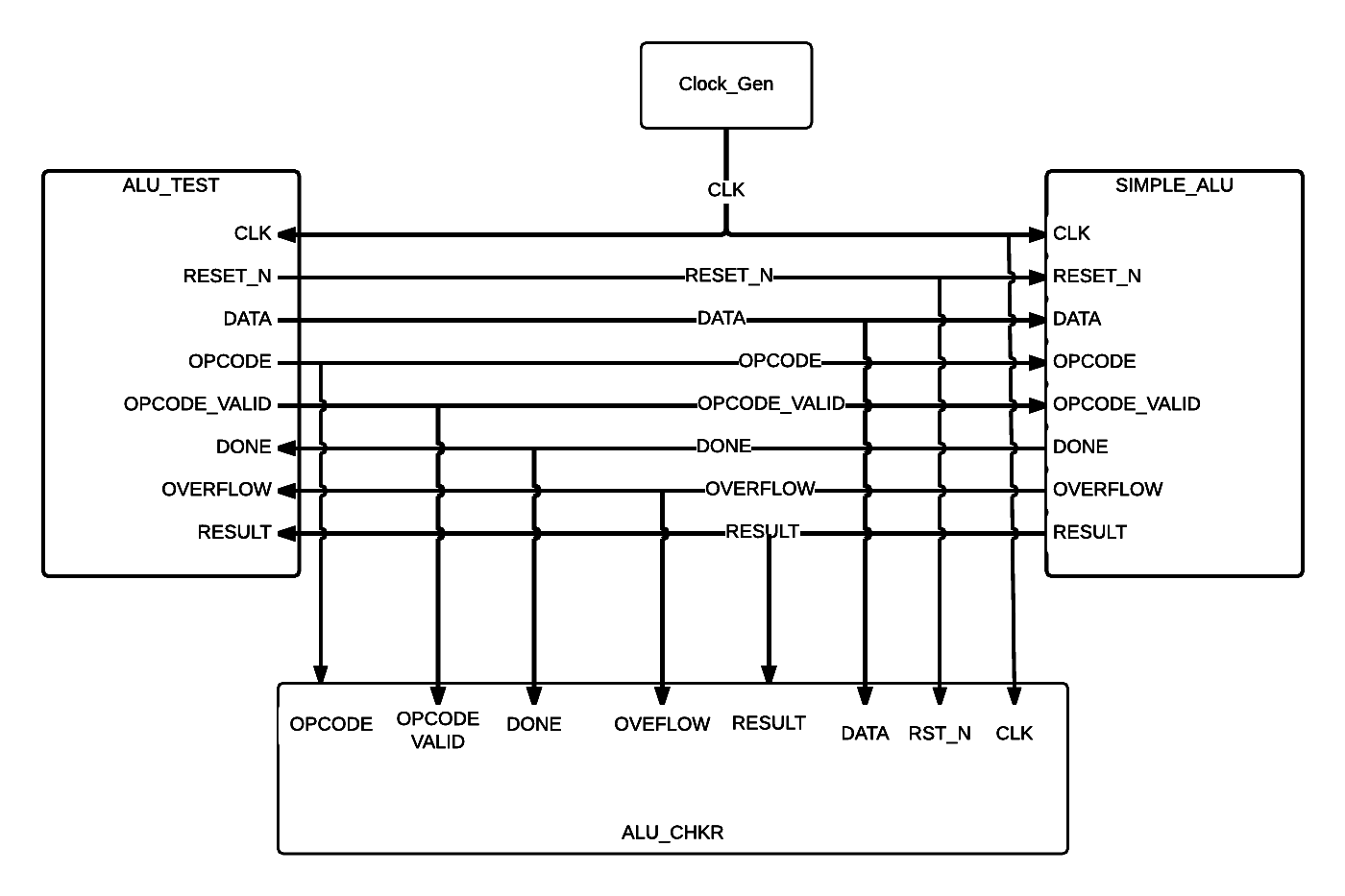
PSU ID: 958880624

High Level Block Diagram





Block Diagram with connections at high level



# Assumptions:

* FSM State IDLE should clear the done bit and should not change any other outputs, i.e. hold their values
* Logical Operators are the lowest level of code writing expected
* Delay were not accounted for the simulation
* Race conditions could be ignored
* Arithmetic operations are unsigned operations.

# Observations and Results

* The code was simulated and verified with the tester code provided
* Transcript and the source codes are provided with the report in the submission folder
* Files were arranged as required and submitted to d2l.pdx.edu

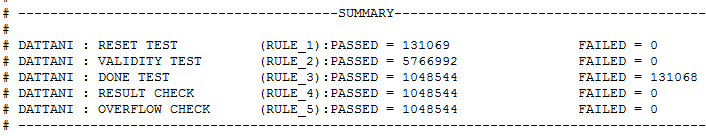
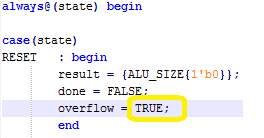


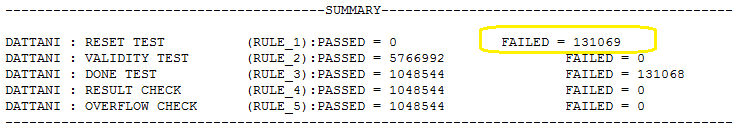
Figure 1: No additional bug introduced

# Individual Bug Checking

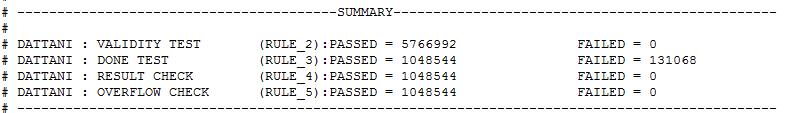
# Add separate bugs in the DUT and show the transcript that your checker flags errors for rule#1, 4 & 5. Document where you introduced your bugs in the DUT.

1. Bug introduced for rule 1.

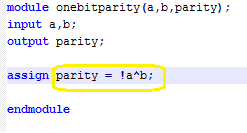


Result Observed:

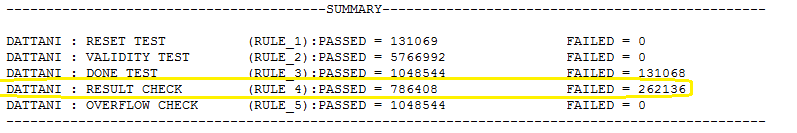
Result Observed when RULE\_1 disabled:



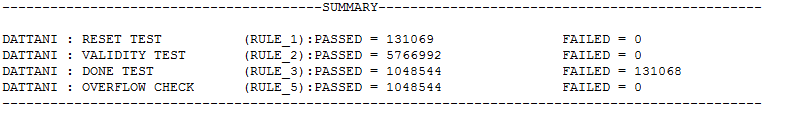
1. Bug Introduced for rule 4



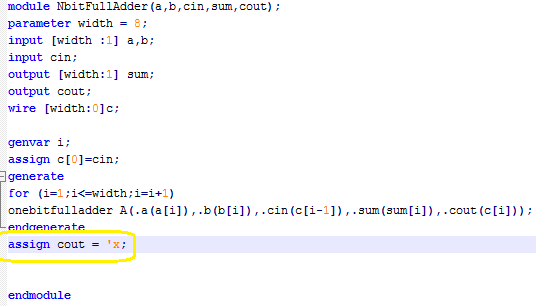
Result Observed:



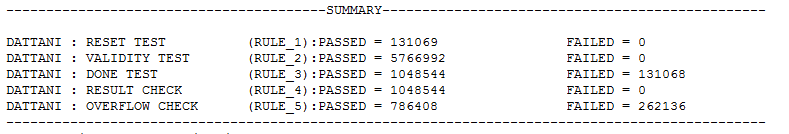
Result Observed when RULE\_4 disabled



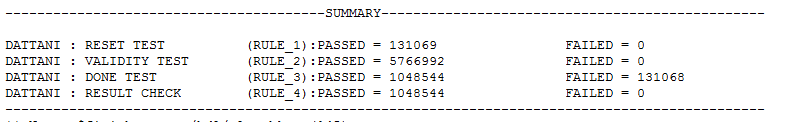
1. Bug introduced for rule 5



Result Observed:

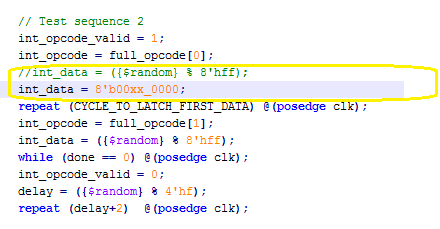


Result Observed when RULE\_5 disabled

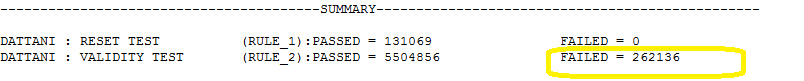


# Add a bug in the test generator and show the transcript that your checker flags errors for rule#2. Document where you introduced your bug in the test generator

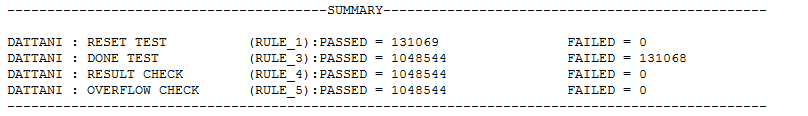
Bug Introduced:



Result Observed:

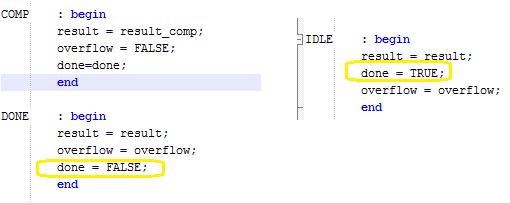


Result Observed when RULE\_2 disabled:



# Bonus: Introduce a bug in the DUT and see if you can get your checker to flag an error for rule#3.

Bug Introduced:



Result Observed:

